

# SN54ABT16825, SN74ABT16825 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS218D – JUNE 1992 – REVISED OCTOBER 2000

- Members of Texas Instruments' Widebus™ Family
- Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD 17
- Typical  $V_{OLP}$  (Output Ground Bounce) <1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ( $-32\text{-mA } I_{OH}$ ,  $64\text{-mA } I_{OL}$ )

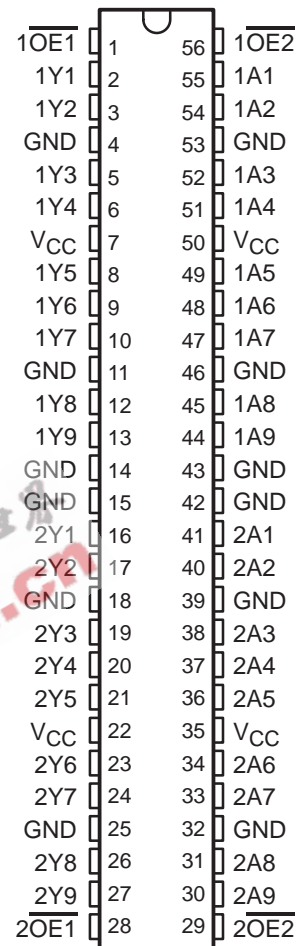
## description

The 'ABT16825 devices are 18-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as two 9-bit buffers or one 18-bit buffer. They provide true data.

The 3-state control gate is a 2-input AND gate with active-low inputs so that, if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all nine affected outputs are in the high-impedance state.

When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

SN54ABT16825 . . . WD PACKAGE  
SN74ABT16825 . . . DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ABT16825DL	ABT16825
		Tape and reel	SN74ABT16825DLR	
-55°C to 125°C	CFP–WD	Tube	SNJ54ABT16825WD	SNJ54ABT16825WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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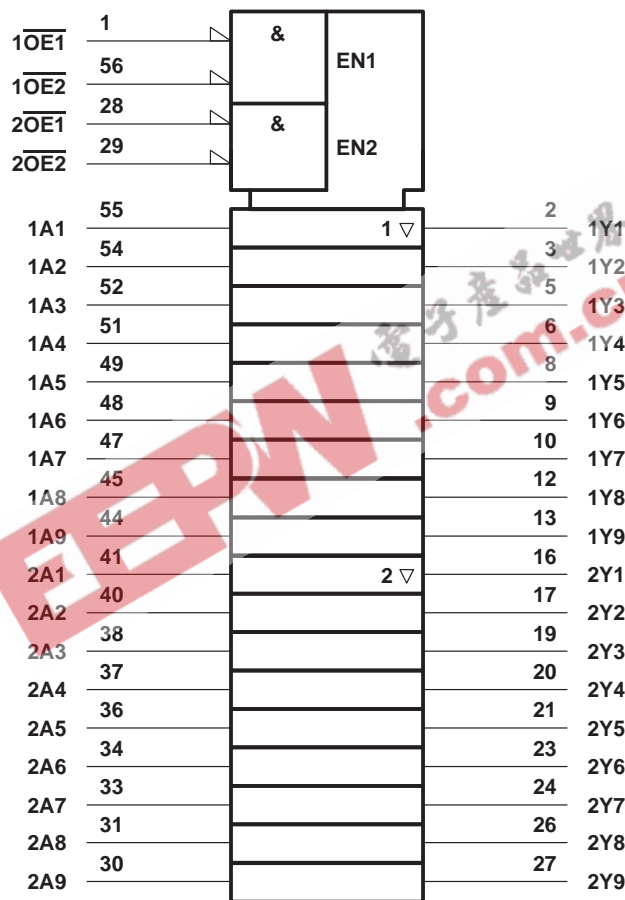
# SN54ABT16825, SN74ABT16825 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each 9-bit section)

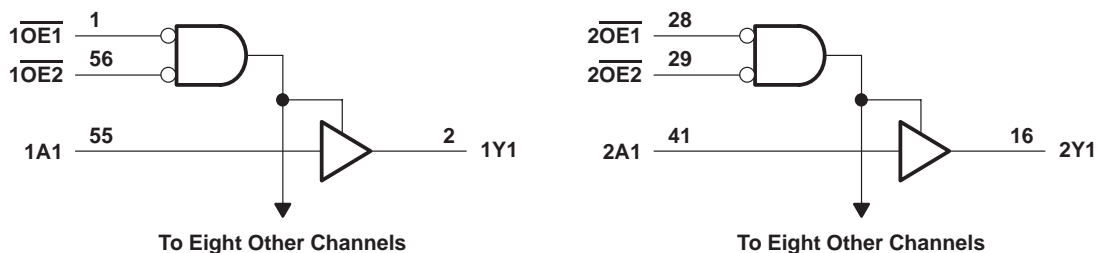
INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



# SN54ABT16825, SN74ABT16825 18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABT16825 .....	96 mA
SN74ABT16825 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2) .....	56°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

		SN54ABT16825		SN74ABT16825		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Control pins		4		ns/V
		Data pins		10		
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu$ s/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54ABT16825, SN74ABT16825

## 18-BIT BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$T_A = 25^\circ\text{C}$			SN54ABT16825		SN74ABT16825		UNIT		
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
$V_{IK}$	$V_{CC} = 4.5\text{ V}$ , $I_I = -18\text{ mA}$			-1.2		-1.2		-1.2	V		
$V_{OH}$	$V_{CC} = 4.5\text{ V}$ , $I_{OH} = -3\text{ mA}$			2.5		2.5		2.5	V		
	$V_{CC} = 5\text{ V}$ , $I_{OH} = -3\text{ mA}$			3		3		3			
	$V_{CC} = 4.5\text{ V}$	$I_{OH} = -24\text{ mA}$			2		2				
$V_{OL}$	$V_{CC} = 4.5\text{ V}$	$I_{OL} = 48\text{ mA}$				0.55		0.55	V		
		$I_{OL} = 64\text{ mA}$				0.55*		0.55			
$V_{hys}$				100					mV		
$I_I$	$V_{CC} = 0\text{ to }5.5\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$		$\pm 1$		$\pm 1$	$\mu\text{A}$		
$I_{OZPU}$	$V_{CC} = 0\text{ to }2.1\text{ V}$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$		$\pm 50$		$\pm 50$	$\mu\text{A}$		
$I_{OZPD}$	$V_{CC} = 2.1\text{ V to }0$ , $V_O = 0.5\text{ V to }2.7\text{ V}$ , $\overline{OE} = X$			$\pm 50$		$\pm 50$		$\pm 50$	$\mu\text{A}$		
$I_{OZH}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 2.7\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			10		10		10	$\mu\text{A}$		
$I_{OZL}$	$V_{CC} = 2.1\text{ V to }5.5\text{ V}$ , $V_O = 0.5\text{ V}$ , $\overline{OE} \geq 2\text{ V}$			-10		-10		-10	$\mu\text{A}$		
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O \leq 4.5\text{ V}$			$\pm 100$				$\pm 100$	$\mu\text{A}$		
$I_{CEX}$	Outputs high $V_{CC} = 5.5\text{ V}$ , $V_O = 5.5\text{ V}$			50		50		50	$\mu\text{A}$		
$I_{O\ddagger}$	$V_{CC} = 5.5\text{ V}$ , $V_O = 2.5\text{ V}$			-50	-100	-180	-50	-180	-50	-180	mA
$I_{CC}$	Outputs high	$V_{CC} = 5.5\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$			2		2		2	mA	
	Outputs low				32		32		32		
	Outputs disabled				2		2		2		
$\Delta I_{CC}\S$	$V_{CC} = 5.5\text{ V}$ , One input at 3.4 V, Other inputs at $V_{CC}\text{ or GND}$			1.5		1.5		1.5	mA		
$C_i$	$V_I = 2.5\text{ V or }0.5\text{ V}$			3					pF		
$C_o$	$V_O = 2.5\text{ V or }0.5\text{ V}$			7.5					pF		

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at  $V_{CC} = 5\text{ V}$ .

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$			SN54ABT16825		SN74ABT16825		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	1	1.9	3.6	1	4.1	1	3.9	ns
$t_{PHL}$			1	2.1	3.9	1	4.7	1	4.4	
$t_{PZH}$	$\overline{OE}$	Y	1	2.8	5.5	1	6.4	1	6.1	ns
$t_{PZL}$			1	2.8	5.4	1	6.3	1	6	
$t_{PHZ}$	$\overline{OE}$	Y	2.4	4.5	6.8	2.4	7.1	2.4	6.9	ns
$t_{PLZ}$			1.6	3.7	6.2	1.6	7.6	1.6	6.6	

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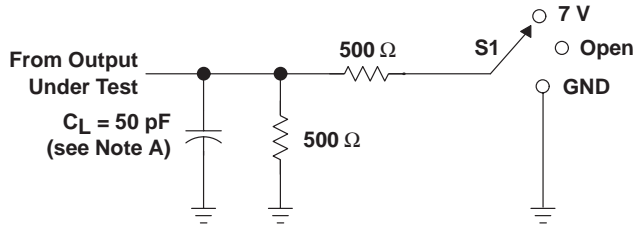


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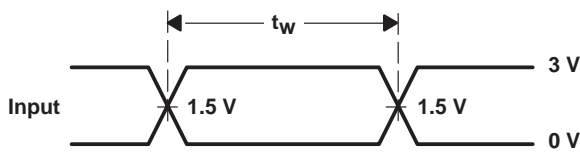
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PARAMETER MEASUREMENT INFORMATION

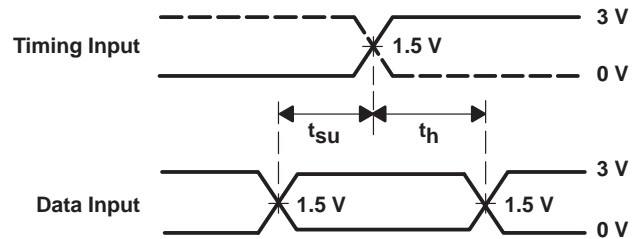


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

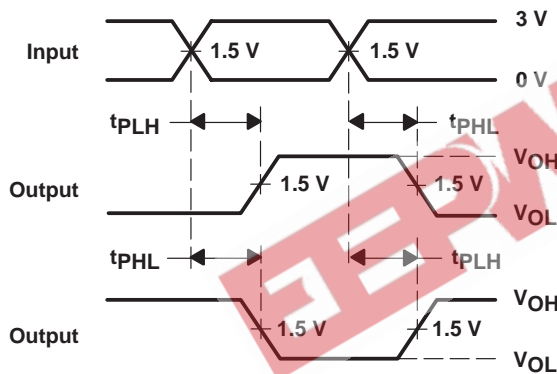
LOAD CIRCUIT



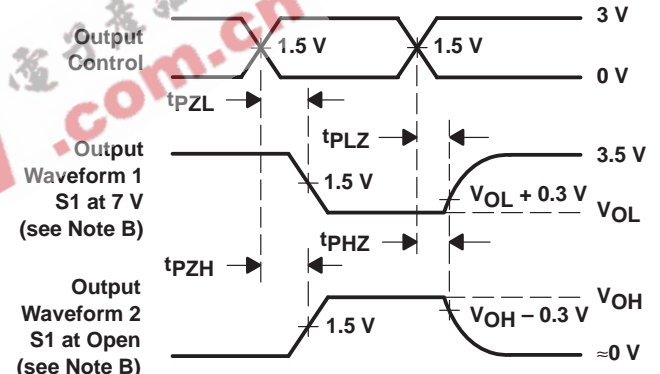
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ABT16825DL	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16825DLG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16825DLR	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ABT16825DLRG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

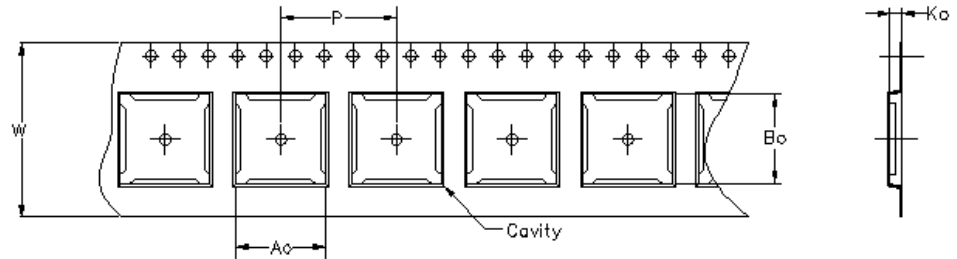
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

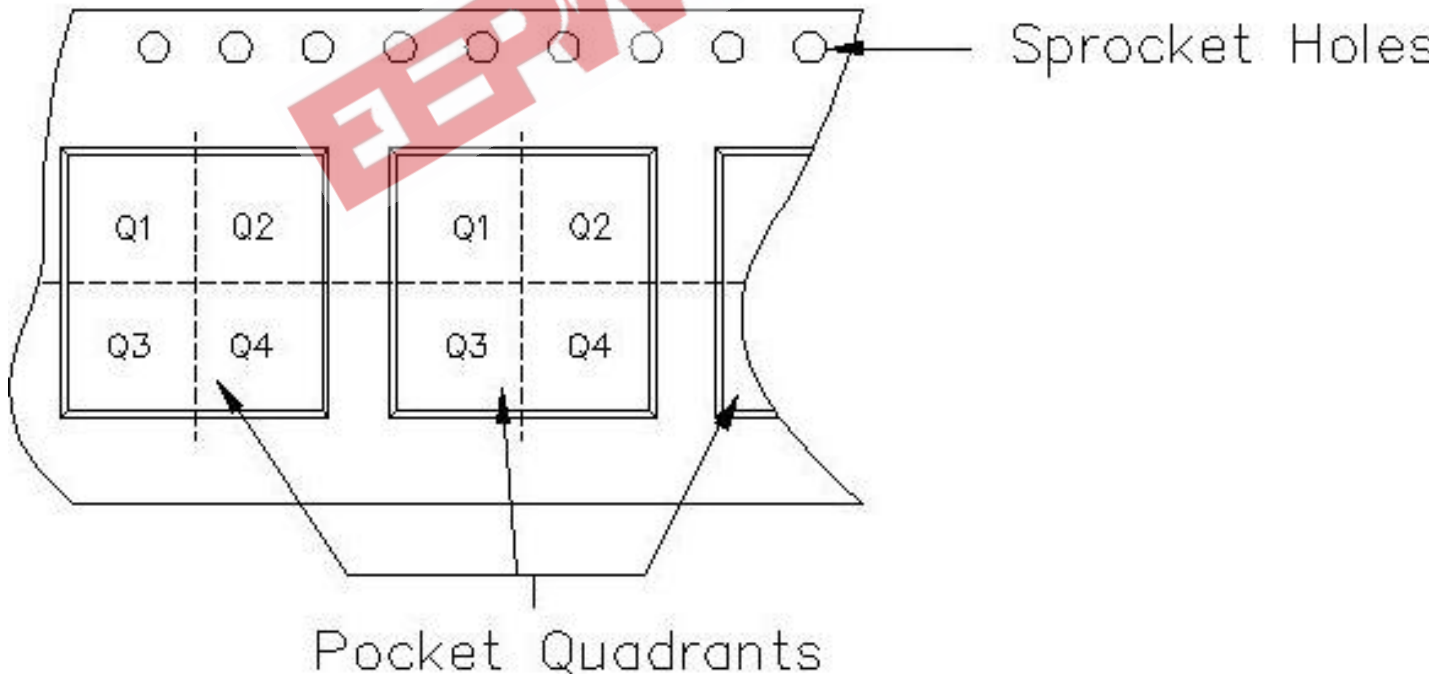
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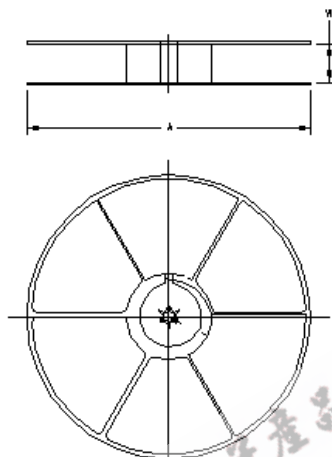
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



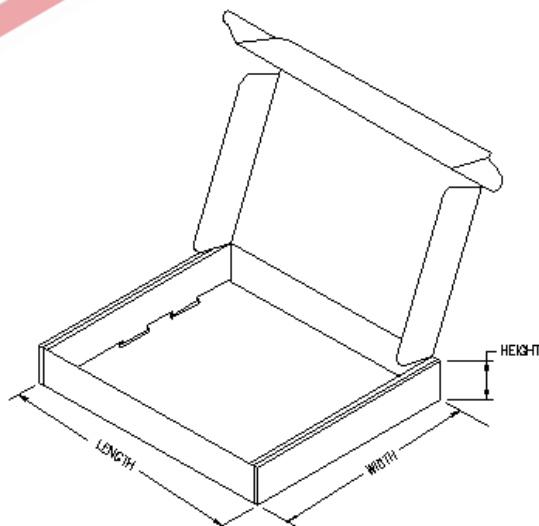
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT16825DLR	DL	56	MLA	330	32	11.35	18.67	3.1	16	32	Q1



**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74ABT16825DLR	DL	56	MLA	336.6	342.9	41.3





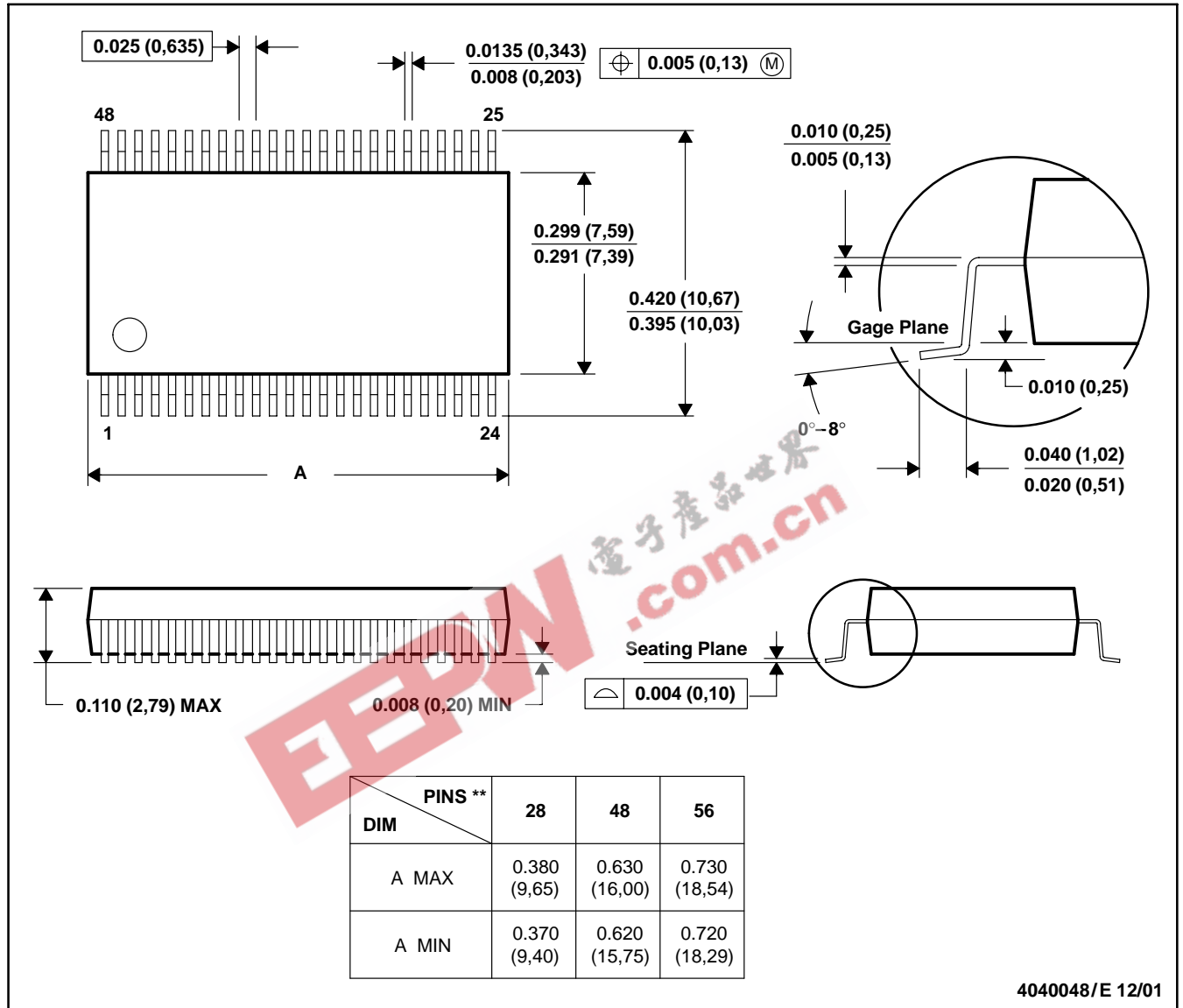
# MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

## DL (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

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