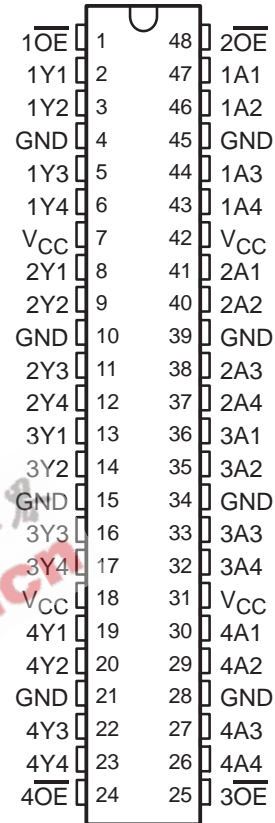


SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS238E – JUNE 1992 – REVISED JUNE 2004

- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- I_{off} and Power-Up 3-State Support Hot Insertion
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD-17

SN54ABT162244 . . . WD PACKAGE
SN74ABT162244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description/ordering information

The 'ABT162244 devices are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide noninverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

The outputs, which are designed to source or sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ABT162244DL	ABT162244
		Tape and reel	SN74ABT162244DLR	
	TSSOP – DGG	Tape and reel	SN74ABT162244DGGR	ABT162244
-55°C to 125°C	TVSOP – DGV	Tape and reel	SN74ABT162244DGV	AH2244
	CFP – WD	Tube	SNJ54ABT162244WD	SNJ54ABT162244WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS238E – JUNE 1992 – REVISED JUNE 2004

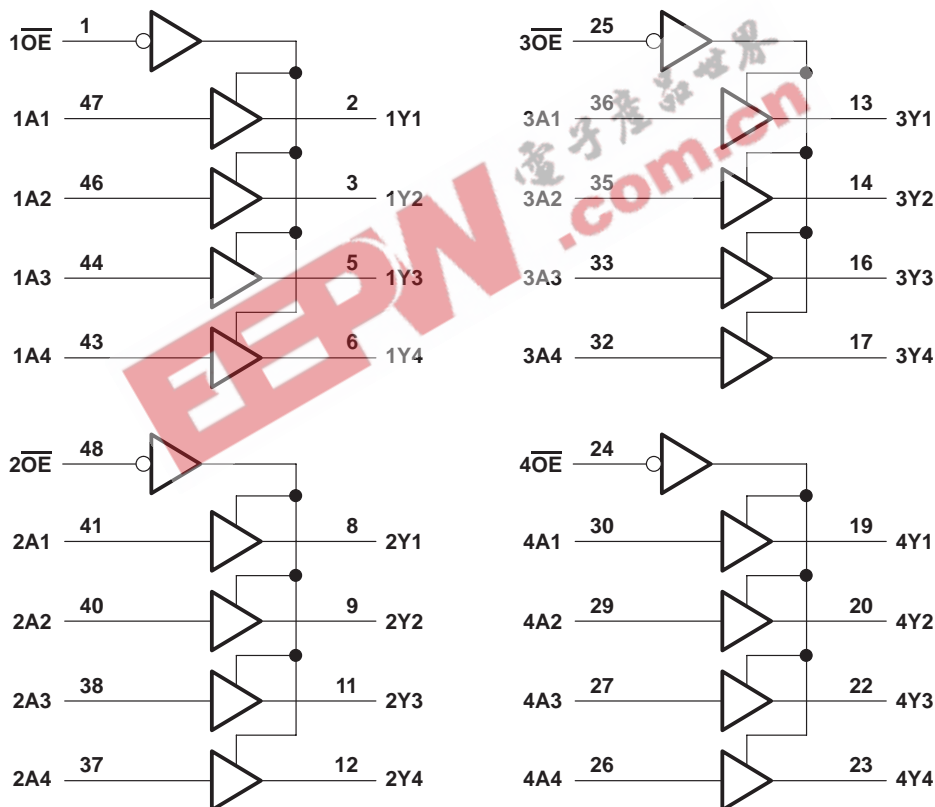
description/ordering information (continued)

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS238E – JUNE 1992 – REVISED JUNE 2004

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	–0.5 V to 7 V	
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V	
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V	
Current into any output in the low state, I_O	30 mA	
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA	
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA	
Package thermal impedance, θ_{JA} (see Note 2):	DGG package	70°C/W
	DGV package	58°C/W
	DL package	63°C/W
Storage temperature range, T_{stg}	–65°C to 150°C	

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		SN54ABT162244		SN74ABT162244		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V_{IH}	High-level input voltage	2		2		V
V_{IL}	Low-level input voltage		0.8		0.8	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current		–3		–12	mA
I_{OL}	Low-level output current		8		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10	10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
T_A	Operating free-air temperature	–55	125	–40	85	°C

- NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS238E – JUNE 1992 – REVISED JUNE 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT162244		SN74ABT162244		UNIT
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2		-1.2		-1.2	V
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -1 mA	3.35			3.35		3.35		V
	V _{CC} = 5 V, I _{OH} = -1 mA	3.85			3.85		3.85		
	V _{CC} = 4.5 V, I _{OH} = -3 mA	3.1			3.1		3.1		
V _{OL}	V _{CC} = 4.5 V, I _{OL} = 8 mA		0.4			0.8		0.65	V
		I _{OL} = 12 mA		0.8*				0.8	
V _{hys}			100						mV
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, $\overline{OE} = X$			±50		±50		±50	μA
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, $\overline{OE} \geq 2$ V			10		10		10	μA
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, $\overline{OE} \geq 2$ V			-10		-10		-10	μA
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V, Outputs high			50		50		50	μA
I _O	V _{CC} = 5.5 V, V _O = 2.5 V	-25	-55	-100	-25	-100	-25	-100	mA
I _{CC} ‡	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high		2		2		2	mA
		Outputs low		30		30		30	
		Outputs disabled		2		2		2	
ΔI _{CC} §	Data inputs V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled		50		50		50	μA
		Outputs disabled		50		50		50	
	Control inputs V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			50		50		50	
C _i	V _I = 2.5 V or 0.5 V			3					pF
C _o	V _O = 2.5 V or 0.5 V			8					pF

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

SN54ABT162244, SN74ABT162244
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS238E – JUNE 1992 – REVISED JUNE 2004

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT162244				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.5	3.6	1	4.1	ns
t_{PHL}			1	3.1	4.7	1	5.3	
t_{PZH}	\overline{OE}	Y	1	3.2	4.8	1	5.6	ns
t_{PZL}			1	3.2	4.7	1	5.5	
t_{PHZ}	\overline{OE}	Y	1	3.2	5.3	1	6.3	ns
t_{PLZ}			1	3.1	4.6	1	4.9	

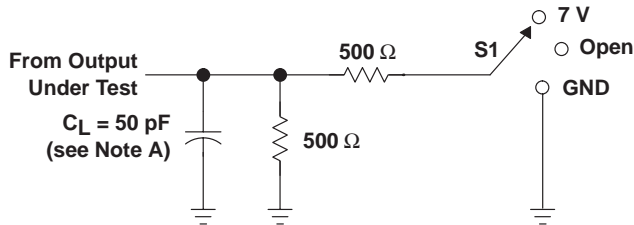
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT162244				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
t_{PLH}	A	Y	1	2.5	3.2	1	3.9	ns
t_{PHL}			1	3.1	4	1	4.8	
t_{PZH}	\overline{OE}	Y	1	3.2	4.2	1	5.4	ns
t_{PZL}			1	3.2	4.1	1	5.1	
t_{PHZ}	\overline{OE}	Y	1	3.2	4	1	4.6	ns
t_{PLZ}			1	3.1	3.9	1	4.5	

SN54ABT162244, SN74ABT162244 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

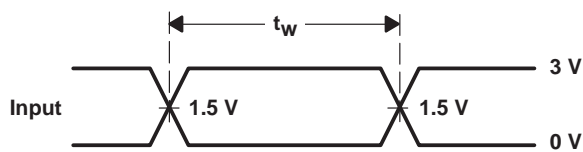
SCBS238E – JUNE 1992 – REVISED JUNE 2004

PARAMETER MEASUREMENT INFORMATION

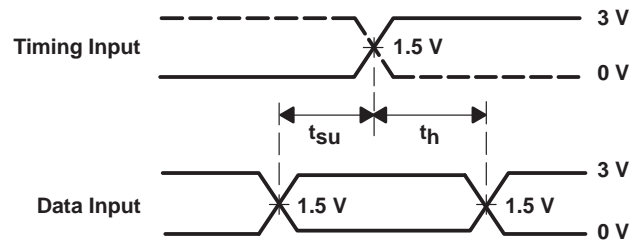


LOAD CIRCUIT

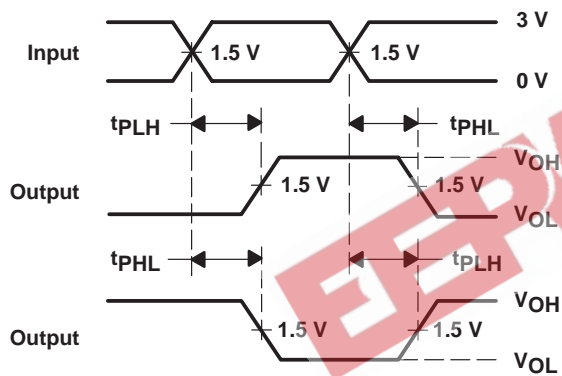
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



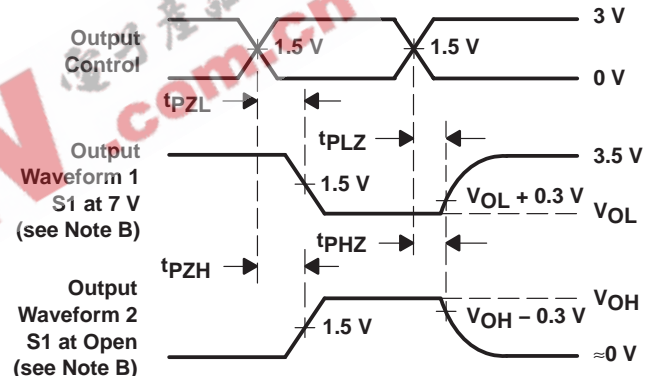
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9458701QXA	ACTIVE	CFP	WD	48	1	None	Call TI	Level-NC-NC-NC
SN74ABT162244DGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ABT162244DGVR	ACTIVE	TVSOP	DGV	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74ABT162244DL	ACTIVE	SSOP	DL	48	25	None	CU NIPDAU	Level-1-235C-UNLIM
SN74ABT162244DLR	ACTIVE	SSOP	DL	48	1000	None	CU NIPDAU	Level-1-235C-UNLIM
SNJ54ABT162244WD	ACTIVE	CFP	WD	48	1	None	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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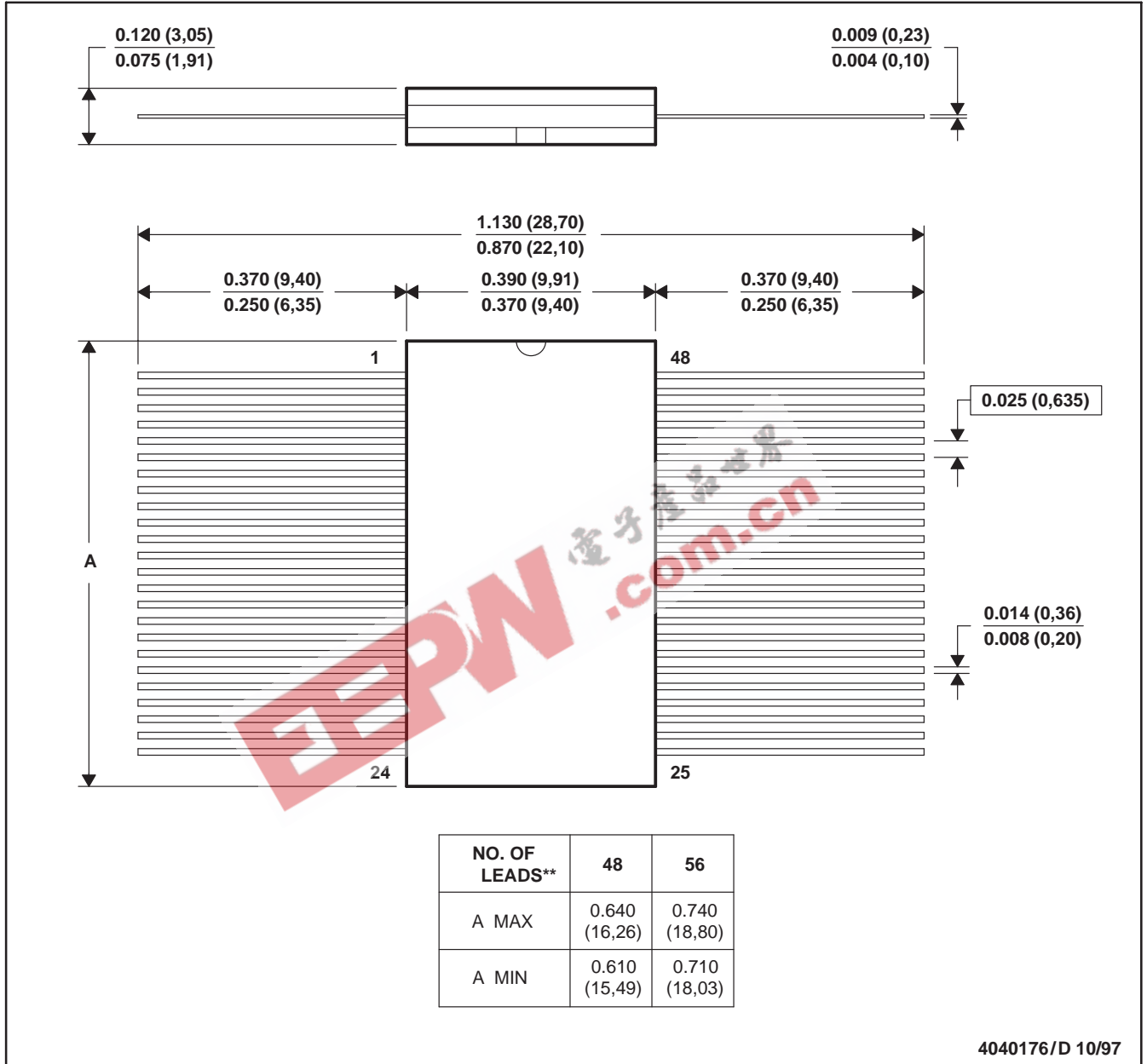
MECHANICAL DATA

MCFP010B – JANUARY 1995 – REVISED NOVEMBER 1997

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

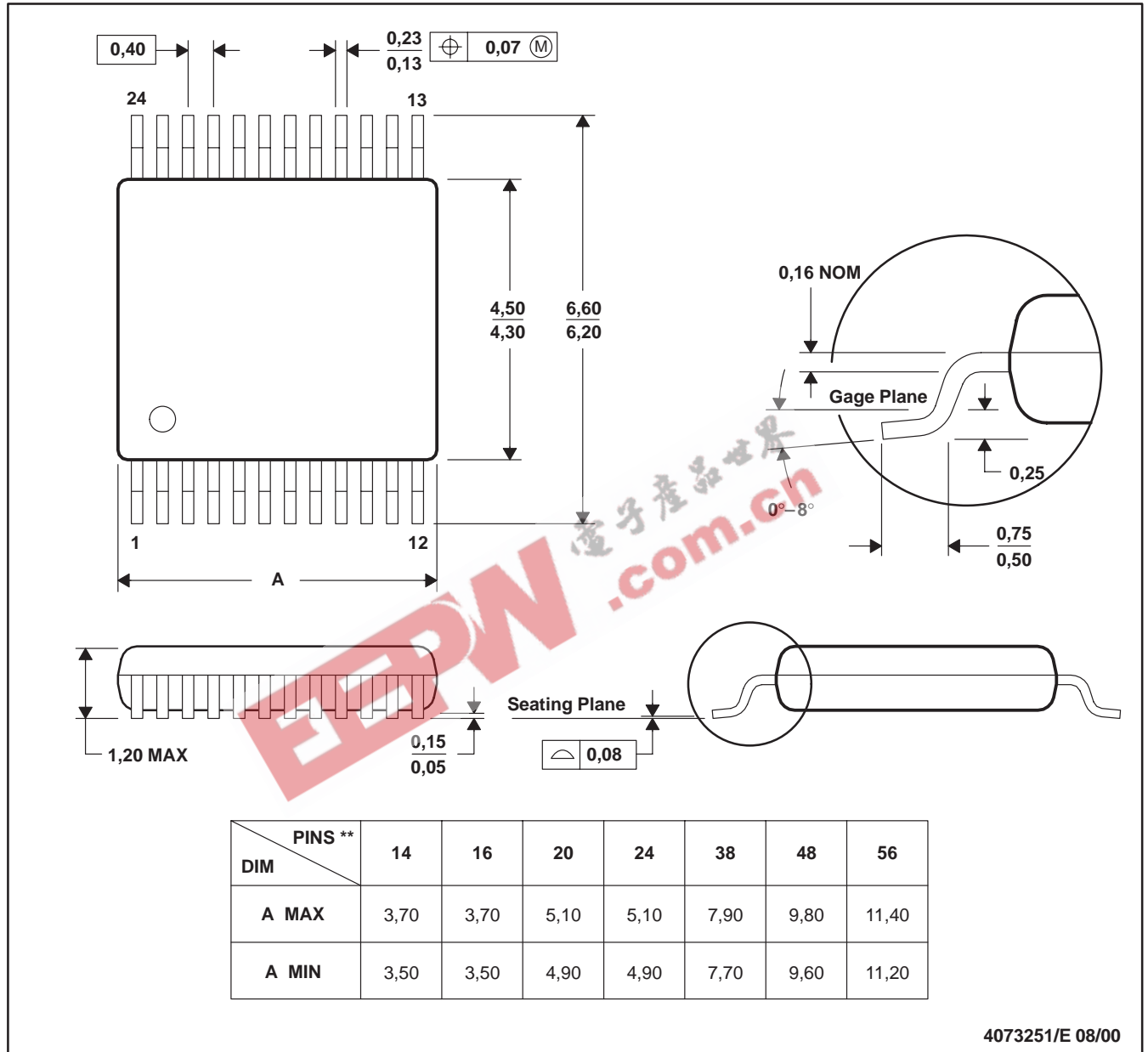
MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G)**

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

4040078/F 12/97

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265