# **SPICE I/O MODEL**

## SN74ABT16241 **16-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS

SCBS347 - MAY 1994

<ul> <li>Member of the Texas Instruments</li></ul>	D	L PACKAG	iE
Widebus™ Family		(TOP VIEW	)
<ul> <li>State-of-the-Art EPIC-IIB<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation</li> </ul>		$1 \qquad 48$	20E
<ul> <li>Typical V<sub>OLP</sub> (Output Ground Bounce)</li> <li>&lt; 1 V at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C</li> </ul>		2 47 3 46 4 45	
<ul> <li>Distributed V<sub>CC</sub> and GND Pin Configuration</li></ul>	1Y3	5 44	1A3
Minimizes High-Speed Switching Noise	1Y4	6 43	
<ul> <li>Flow-Through Architecture Optimizes</li></ul>	V <sub>CC</sub>	7 42	V <sub>CC</sub>
PCB Layout	2Y1	8 41	2A1
<ul> <li>High-Drive Outputs (-32-mA I<sub>OH</sub>,</li></ul>	2Y2	9 40	2A2
64-mA I <sub>OL</sub> )	GND	10 39	GND
<ul> <li>Packaged in Plastic 300-mil Shrink</li></ul>	2Y3	11 38	2A3
Small-Outline (SSOP) Packages	2Y4	12 37	2A4
description	311 3Y2	13 30 14 35 15 34	3A1 3A2
The SN74ABT16241 is a 16-bit buffer and line driver designed specifically to improve both the	3Y3	16 33	3A3
	3Y4	17 32	3A4
performance and density of 3-state memory	x x Vec	18 31	V <sub>CC</sub>
address drivers, clock drivers, and bus-oriented		19 30	4A1
receivers and transmitters. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs	4Y2 GND	20 29 21 28	4A2 GND
and complementary output-enable (OE and $\overline{OE}$ ) inputs.	4Y3 4Y4 4OF	22 27 23 26	4A3 4A4

To ensure the high-impedance state during power up or power down, OE should be tied to V<sub>CC</sub>

through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

4<u>OE</u> 24

25 30E

The SN74ABT16241 is available in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ABT16241 is characterized for operation from -40°C to 85°C.

INPUTS		OUTPUTS	INPU	OUTPUTS		
10E, 40E	1A, 4A	1Y, 4Y	20E, 30E	2A, 3A	2Y, 3Y	
L	Н	Н	Н	Н	Н	
L	L	L	Н	L	L	
Н	Х	Z	L	Х	Z	

#### **FUNCTION TABLE**

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## SN74ABT16241 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS SCBS347 - MAY 1994

### logic diagram (positive logic)



110				NODE	ODEDATION	
1	2	OPERATION	4	5	6	OPERATION
L	Н	Input	L	Н	L	Output
Н	L	Input	Н	L	L	Output
			Х	Ζ	Н	Hi-Z



## **SPICE I/O MODEL**

### SPICE netlist

\*

ABT16241 SPICE I/O MODEL SUBCIRCUIT ADVANCED BUS INTERFACE \* \* ADVANCED SYSTEM LOGIC, TEXAS INSTRUMENTS \* SUBCIRCUITS: ABT16241IN, ABT162410UT \* \* \* PACKAGE PARASITICS .LIB 'PKGS.LIB' SSOP48 \* PROCESS MODELS .LIB 'EPIC2B.LIB' NOMINAL L13 .LIB 'EPIC2B.LIB' STRONG L13 .LIB 'EPIC2B.LIB' WEAK L13 \* \* \* ABT16241 INPUT SUBCIRCUIT NODES : INPUT NODE INTERNAL OUTPUT NODE VCC \* \* GND .SUBCKT ABT16241IN 199 100 1 2 SSOP48\_47 SSOP48\_07 SSOP48\_04 1001 X\_PKGIN 1 X\_PKGVCC 199 1199 IN Х PKGGND 100 1100 XABT16241IN ABT16241 1001 2 1199 1100 .ENDS ABT16241IN m-\* ABT16241 OUTPUT SUBCIRCUIT \* NODES: INTERNAL INPUT NODE OUTPUT NODE \* INTERNAL OE NODE \* VCC \* GND \* .SUBCKT ABT162410UT 199 100 5 4 6 X\_PKGOUT 1005 SSOP48 02 SSOP48\_07 X\_PKGVCC 199 1199 X PKGGND 100 1100 SSOP4804 XABT162410UT 4 1005 6 1199 1100 ABT16241 OUT .ENDS ABT162410UT .SUBCKT ABT16241 501 502 599 500 IN XP1 502 504 506 599 ΡM WP=200U LP=0.8U XP2 509 502 599 599 ΡM WP=20U LP=0.8U XP3 506 509 599 599 ΡM WP=85U LP=0.8U 508 500 599 599 WP=50U LP=0.8U XP4 ΡМ 500 500 WN=220U XN1 502 504 NΜ LN=0.8U XN2 509 502 500 500 ΝM WN=20U LN=0.8U XN4 599 500 508 500 NM WN=20U LN=0.8U Q2 NPN QA 599 508 507 10 Q5\_NPN Q7\_NPN Q5\_NPN 599 507 506 OB 60 Q\_ESD1 501 500 500 200 Q ESD 504 505 500 46 XR1 506 507 507 507 RMOS WR=4U RES=6K RESD1 501 504 50 RESD2 505 500 1K CBP 501 500 0.3P CL 502 500 0.2P .ENDS ABT16241\_\_IN .SUBCKT ABT16241 OUT 601 602 603 699 600 WP=200II LP=0.8U XP1 605 603 699 699 РM XP4 601 603 621 699 РM WP = 40ULP=0.8U XP5 613 601 605 699 ΡM WP=30U LP=0.8U 699 XP10 618 603 699 ΡM WP=50U LP=0.8U XP11 607 612 605 699 ΡM WP=60U LP=0.8U XN1 607 608 600 NΜ WN = 100U $T_{\rm N}=0.8U$ 601



# SN74ABT16241 **16-BIT BUFFER/DRIVER** WITH 3-STATE OUTPUTS SCBS347 - MAY 1994

### **SPICE** netlist (continued)

XN2 XN3 XN4 XN6 XN7 XN8 XN9 XN10 XN11 XN12 QM1 QM2 QM1 QM2 QM3 QD4 QDR1 D1 D2	606 608 613 602 621 601 619 620 613 616 602 614 615 613 699	619 609 603 621 603 622 619 604 601 615 608 613 614 615 614 617	607 600 600 600 600 621 620 602 600 602 600 615 616 613	600 600 600 600 600 600 600 600 600	NM NM NM NM NM NM NM NM NM Q9_NPN Q11_NPN Q11_NPN Q4_NPN Q2_NPN Q2_NPN D1_GDS D9_GSD	WN=50U WN=25U WN=25U WN=100U WN=20U WN=20U WN=25U WN=25U WN=25U WN=40U 200 600 15 8 8 8 156 4700	LN=0.8U LN=0.8U LN=0.8U LN=0.8U LN=0.8U LN=0.8U LN=0.8U LN=0.8U LN=0.8U LN=0.8U
XR1	606	605	605	605	RMOS	WR=6U	RES=1K
XR2	607	606	606	606	RMOS	WR=4U	RES=3K
XR3	614	605	605	605	RMOS	WR=6U	RES=1K
R4	616	617				10	
XR10	619	618	618	618	RMOS	WR=3U	RES=20K
XPVREF	670	603	699	699	PM	WP=50U	LP=0.8U
XNVREF	671	671	600	600	NM	WN=30U	LN=0.8U
XRVREF1	604	670	670	670	RMOS	WR=3U	RES=20K
XRVREF2	671	604	604	604	RMOS 🥠	WR=3U	RES=1.5K
XNCLAMP	673	612	674	600	NM 🧼 🔊	WN=250U	LN=0.8U
DCLAMP1	608	673			D6 GSD	800	
DCLAMP2	674	602			D6_GSD	800	
XPNOR1	675	609	699	699	PM	WP=30U	LP=0.8U
XPNOR2	612	611	675	699	PM	WP=30U	LP=0.8U
XNNOR1	612	611	600	600	NM	WN=6U	LN=0.8U
XNNOR2	612	609	600	600	NM	WN=6U	LN=0.8U
XP_INV1	609	601	699	699	PM	WP=20U	LP=0.8U
XN_INV1	609	601	600	600	NM	WN=10U	LN=0.8U
XP_INV2	622	603	699	699	PM	WP=15U	LP=0.8U
XN_INV2	622	603	600	600	NM	WN=5U	LN=0.8U
XP_INV3	610	603	699	699	PM	WP=4U	LP=0.8U
XN_INV3	610	603	600	600	NM	WN=4U	LN=0.8U
XP_INV4	611	610	699	699	PM	WP=4U	LP=0.8U
XN_INV4	611	610	600	600	NM	WN=4U	LN=0.8U
CBP	602	600				0.3P	

.ENDS ABT16241\_\_OUT \*



30-Mar-2005

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ABT16241DGGR	OBSOLETE	TSSOP	DGG	48	TBD	Call TI	Call TI
SN74ABT16241DL	OBSOLETE	SSOP	DL	48	TBD	Call TI	Call TI
SN74ABT16241DLR	OBSOLETE	SSOP	DL	48	TBD	Call TI	Call TI

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## **MECHANICAL DATA**

MTSS003D - JANUARY 1995 - REVISED JANUARY 1998

### PLASTIC SMALL-OUTLINE PACKAGE

DGG (R-PDSO-G\*\*) 48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153



## **MECHANICAL DATA**

MSSO001C - JANUARY 1995 - REVISED DECEMBER 2001

### PLASTIC SMALL-OUTLINE PACKAGE

DL (R-PDSO-G\*\*) 48 PINS SHOWN



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

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