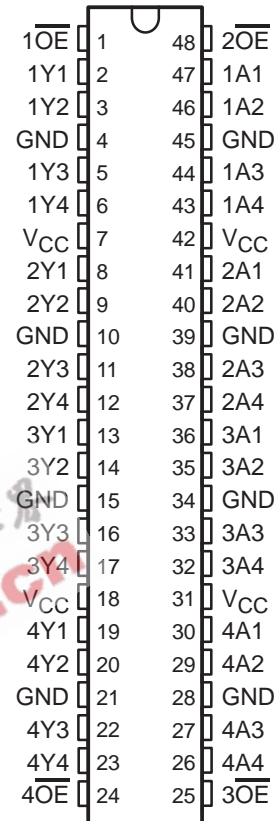


SN54ABT16240A, SN74ABT16240A 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS095G – DECEMBER 1991 – REVISED OCTOBER 1998

- Members of the Texas Instruments *Widebus™* Family
- State-of-the-Art *EPIC-II B™* BiCMOS Design Significantly Reduces Power Dissipation
- Typical V_{OLP} (Output Ground Bounce) < 1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)
- Package Options Include Plastic Shrink Small-Outline (DL), Thin Shrink Small-Outline (DGG), and Thin Very Small-Outline (DGV) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

SN54ABT16240A . . . WD PACKAGE
SN74ABT16240A . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



description

The 'ABT16240A devices are 16-bit buffers and line drivers designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. These devices provide inverting outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT16240A is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ABT16240A is characterized for operation from -40°C to 85°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

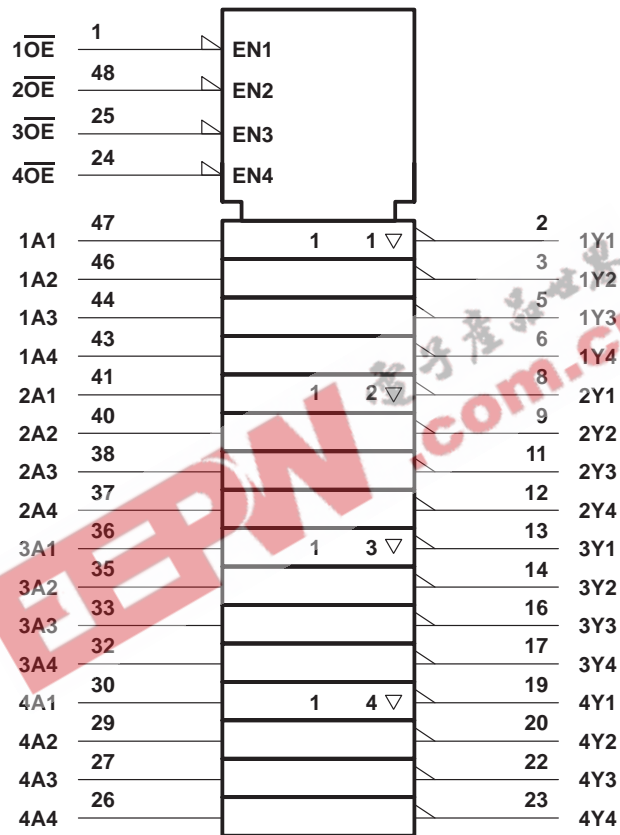
SN54ABT16240A, SN74ABT16240A 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS095G – DECEMBER 1991 – REVISED OCTOBER 1998

FUNCTION TABLE
(each 4-bit buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

logic symbol†

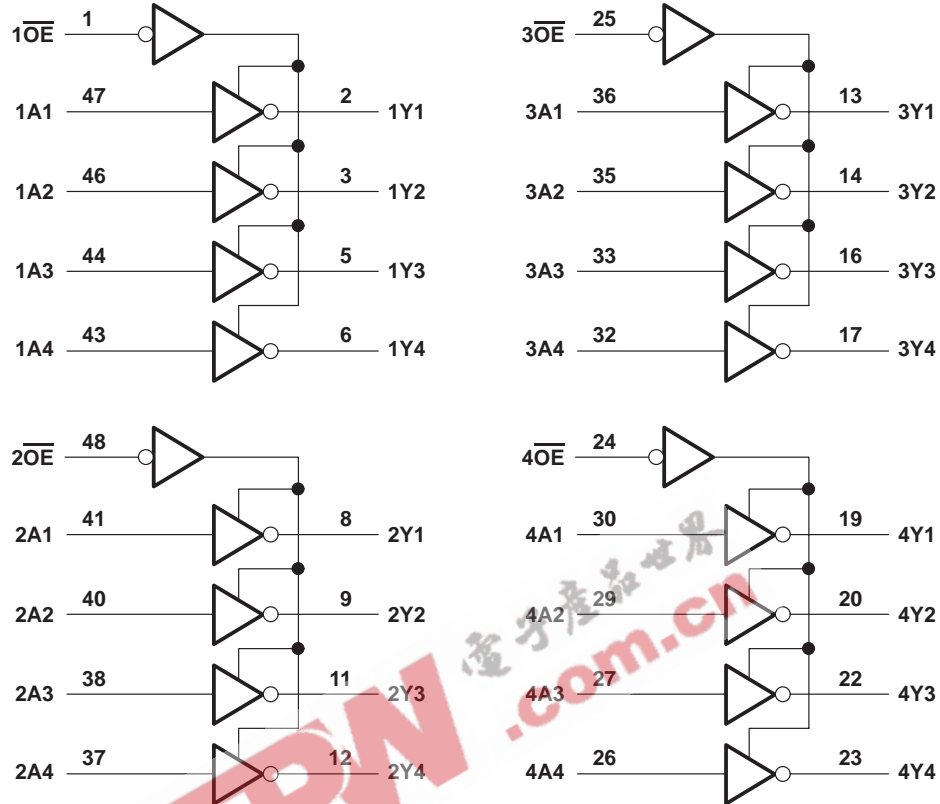


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN54ABT16240A, SN74ABT16240A 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS095G – DECEMBER 1991 – REVISED OCTOBER 1998

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|-----------------|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_{OL} : SN54ABT16240A | 96 mA |
| SN74ABT16240A | 128 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Package thermal impedance, θ_{JA} (see Note 2): DGG package | 89°C/W |
| DGV package | 93°C/W |
| DL package | 94°C/W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JEDEC 51.

SN54ABT16240A, SN74ABT16240A

16-BIT BUFFERS/DRIVERS

WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 3)

| | | SN54ABT16240A | | SN74ABT16240A | | UNIT |
|---------------------|------------------------------------|-----------------|----------|---------------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 4.5 | 5.5 | 4.5 | 5.5 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | -24 | | -32 | mA |
| I_{OL} | Low-level output current | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | | 10 | ns/V |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $T_A = 25^\circ\text{C}$ | | | SN54ABT16240A | | SN74ABT16240A | | UNIT |
|-------------------|---|--------------------------|------|-----------|---------------|---------|---------------|-----------|---------------|
| | | MIN | TYP† | MAX | MIN | MAX | MIN | MAX | |
| V_{IK} | $V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$ | | | -1.2 | | -1.2 | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$ | 2.5 | | | 2.5 | | 2.5 | | V |
| | $V_{CC} = 5\text{ V}$, $I_{OH} = -3\text{ mA}$ | 3 | | | 3 | | 3 | | |
| | $V_{CC} = 4.5\text{ V}$ | | | | 2 | | | 2 | |
| V_{OL} | $V_{CC} = 4.5\text{ V}$ | | | 0.55 | | 0.55 | | | V |
| | | | | 0.55* | | | | 0.55 | |
| V_{hys} | | | 100 | | | | | | mV |
| I_I | $V_{CC} = 5.5\text{ V}$, $V_I = V_{CC}$ or GND | | | ± 1 | | ± 1 | | ± 1 | μA |
| I_{OZH} | $V_{CC} = 5.5\text{ V}$, $V_O = 2.7\text{ V}$ | | | 10 | | 10 | | 10 | μA |
| I_{OZL} | $V_{CC} = 5.5\text{ V}$, $V_O = 0.5\text{ V}$ | | | -10 | | -10 | | -10 | μA |
| I_{off} | $V_{CC} = 0$, V_I or $V_O \leq 4.5\text{ V}$ | | | ± 100 | | | | ± 100 | μA |
| I_{CEX} | $V_{CC} = 5.5\text{ V}$, $V_O = 5.5\text{ V}$ | | | 50 | | 50 | | 50 | μA |
| $I_{O\ddagger}$ | $V_{CC} = 5.5\text{ V}$, $V_O = 2.5\text{ V}$ | -50 | -100 | -180 | -50 | -180 | -50 | -180 | mA |
| I_{CC} | $V_{CC} = 5.5\text{ V}$, $I_O = 0$, $V_I = V_{CC}$ or GND | | | 3 | | 3 | | 3 | mA |
| | | | | 34 | | 34 | | 34 | |
| | | | | 3 | | 3 | | 3 | |
| $\Delta I_{CC}\S$ | Data inputs $V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND | Outputs enabled | | 1 | | 1.5 | | 1 | mA |
| | | Outputs disabled | | 0.05 | | 1 | | 0.05 | |
| | Control inputs $V_{CC} = 5.5\text{ V}$, One input at 3.4 V, Other inputs at V_{CC} or GND | | 1.5 | | 1.5 | | 1.5 | | |
| C_i | $V_I = 2.5\text{ V}$ or 0.5 V | | 3.5 | | | | | | pF |
| C_o | $V_O = 2.5\text{ V}$ or 0.5 V | | 7.5 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at $V_{CC} = 5\text{ V}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

SN54ABT16240A, SN74ABT16240A
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

SCBS095G – DECEMBER 1991 – REVISED OCTOBER 1998

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54ABT16240A | | | | | UNIT |
|-----------|-----------------|-------------|---|-----|-----|-----|-----|------|
| | | | $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| t_{PLH} | A | Y | 0.8 | 2.7 | 3.8 | 0.8 | 4.8 | ns |
| t_{PHL} | | | 1.1 | 3.1 | 4.3 | 1.1 | 4.9 | |
| t_{PZH} | \overline{OE} | Y | 1.3 | 3.3 | 4.3 | 1.3 | 5.4 | ns |
| t_{PZL} | | | 1.4 | 3.4 | 6.2 | 1.4 | 7.2 | |
| t_{PHZ} | \overline{OE} | Y | 1.6 | 3.6 | 6.2 | 1.6 | 7.2 | ns |
| t_{PLZ} | | | 1.4 | 3 | 5.1 | 1.4 | 5.7 | |

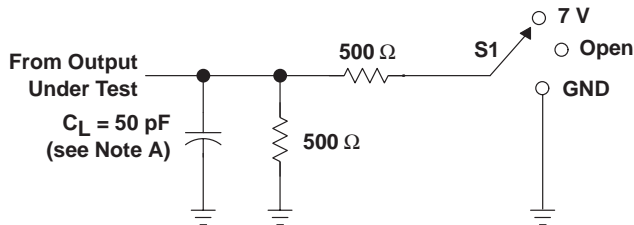
switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74ABT16240A | | | | | UNIT |
|-----------|-----------------|-------------|---|-----|-----|-----|-----|------|
| | | | $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$ | | | MIN | MAX | |
| | | | MIN | TYP | MAX | | | |
| t_{PLH} | A | Y | 1 | 2.7 | 3.8 | 1 | 4.7 | ns |
| t_{PHL} | | | 1.1 | 3.1 | 4.3 | 1.1 | 4.8 | |
| t_{PZH} | \overline{OE} | Y | 1.3 | 3.3 | 4.3 | 1.3 | 5.3 | ns |
| t_{PZL} | | | 1.4 | 3.4 | 6.2 | 1.4 | 7.1 | |
| t_{PHZ} | \overline{OE} | Y | 1.6 | 3.6 | 4.8 | 1.6 | 6.1 | ns |
| t_{PLZ} | | | 1.4 | 3 | 5.1 | 1.4 | 5.6 | |

SN54ABT16240A, SN74ABT16240A 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

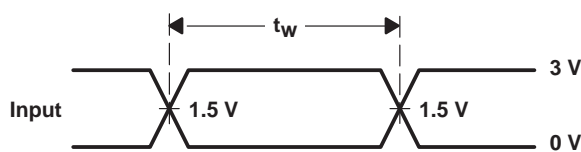
SCBS095G – DECEMBER 1991 – REVISED OCTOBER 1998

PARAMETER MEASUREMENT INFORMATION

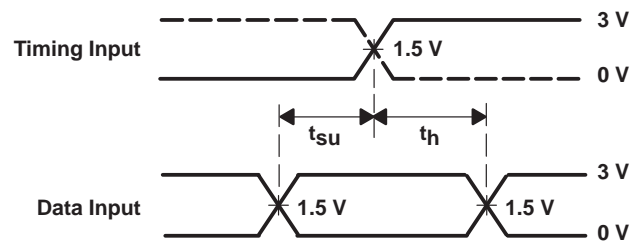


LOAD CIRCUIT

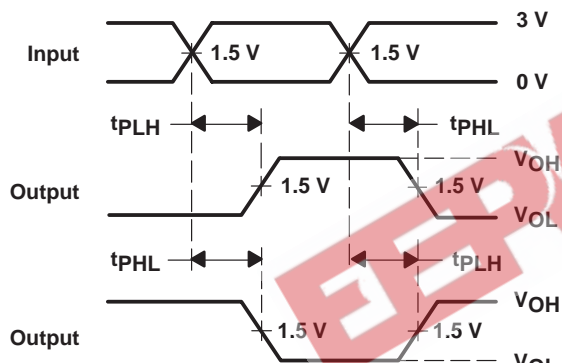
| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 7 V |
| t_{PHZ}/t_{PZH} | Open |



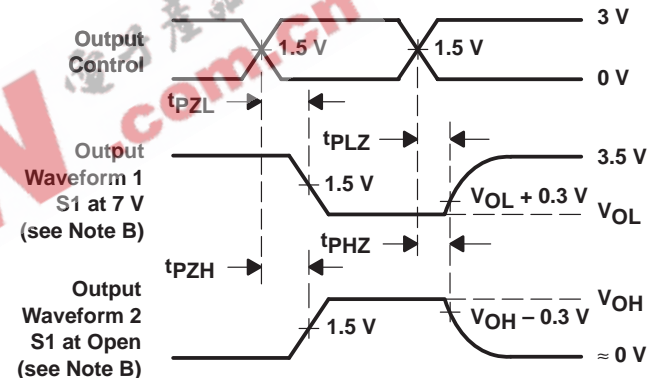
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9319901MXA | ACTIVE | CFP | WD | 48 | 1 | TBD | A42 SNPB | N / A for Pkg Type |
| 74ABT16240ADGGRE4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ABT16240ADGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ABT16240ADGVRE4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74ABT16240ADGVRG4 | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT16240ADGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT16240ADGGRG | ACTIVE | TSSOP | DGG | 48 | | TBD | Call TI | Call TI |
| SN74ABT16240ADGVR | ACTIVE | TVSOP | DGV | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT16240ADL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT16240ADLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT16240ADLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74ABT16240ADLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SNJ54ABT16240AWD | ACTIVE | CFP | WD | 48 | 1 | TBD | A42 SNPB | N / A for Pkg Type |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

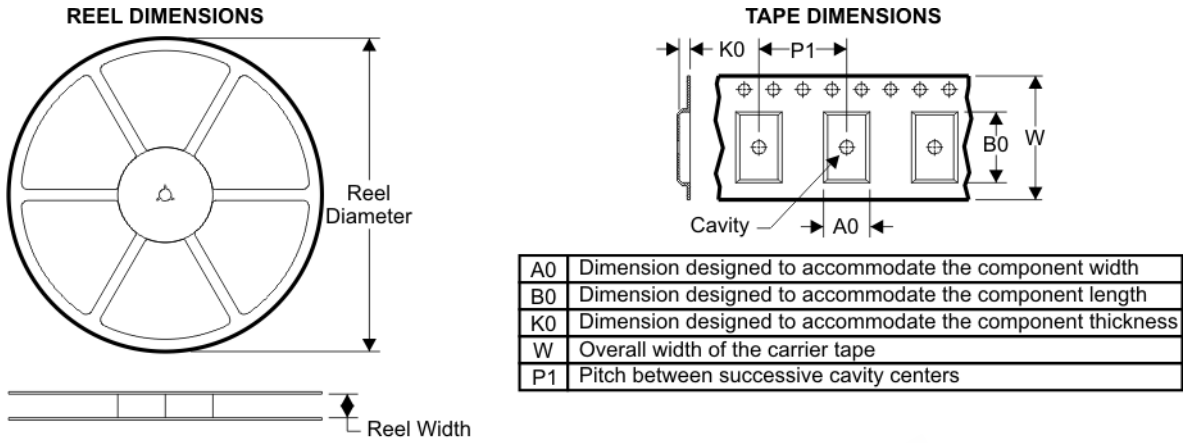
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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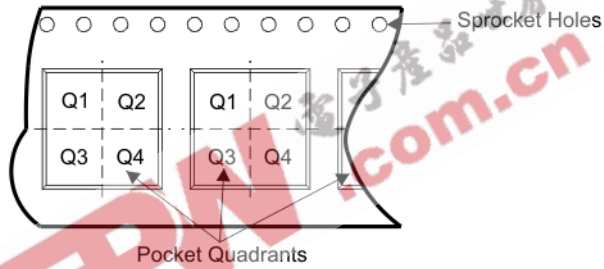
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TAPE AND REEL BOX INFORMATION

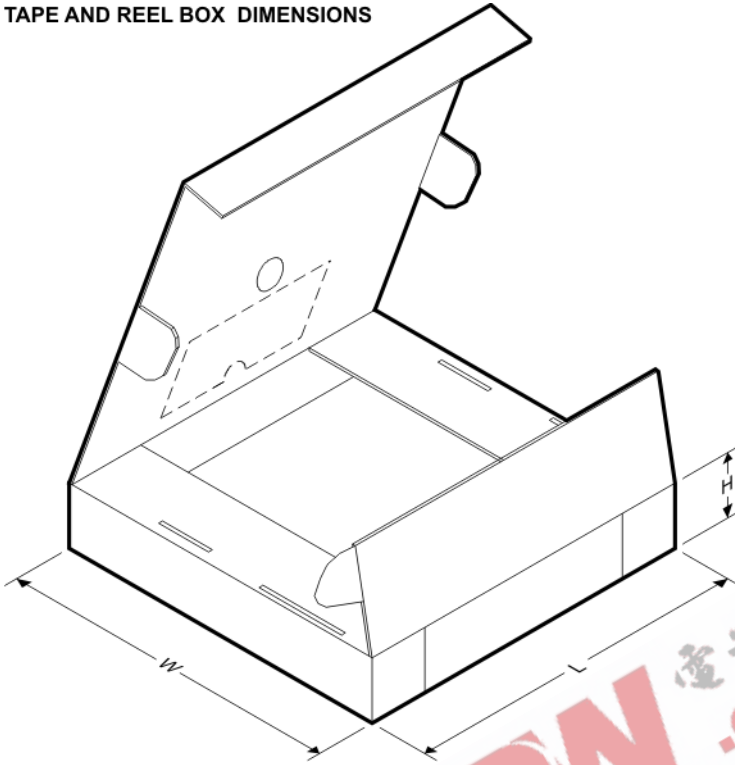


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|---------|------|---------|--------------------|-----------------|---------|---------|---------|---------|--------|---------------|
| SN74ABT16240ADGGR | DGG | 48 | SITE 41 | 330 | 24 | 8.6 | 15.8 | 1.8 | 12 | 24 | Q1 |
| SN74ABT16240ADGVR | DGV | 48 | SITE 41 | 330 | 24 | 6.8 | 10.1 | 1.6 | 12 | 24 | Q1 |
| SN74ABT16240ADLR | DL | 48 | SITE 41 | 330 | 32 | 11.35 | 16.2 | 3.1 | 16 | 32 | Q1 |

TAPE AND REEL BOX DIMENSIONS



| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|-------------------|---------|------|---------|-------------|------------|-------------|
| SN74ABT16240ADGGR | DGG | 48 | SITE 41 | 346.0 | 346.0 | 41.0 |
| SN74ABT16240ADGVR | DGV | 48 | SITE 41 | 346.0 | 346.0 | 41.0 |
| SN74ABT16240ADLR | DL | 48 | SITE 41 | 346.0 | 346.0 | 49.0 |

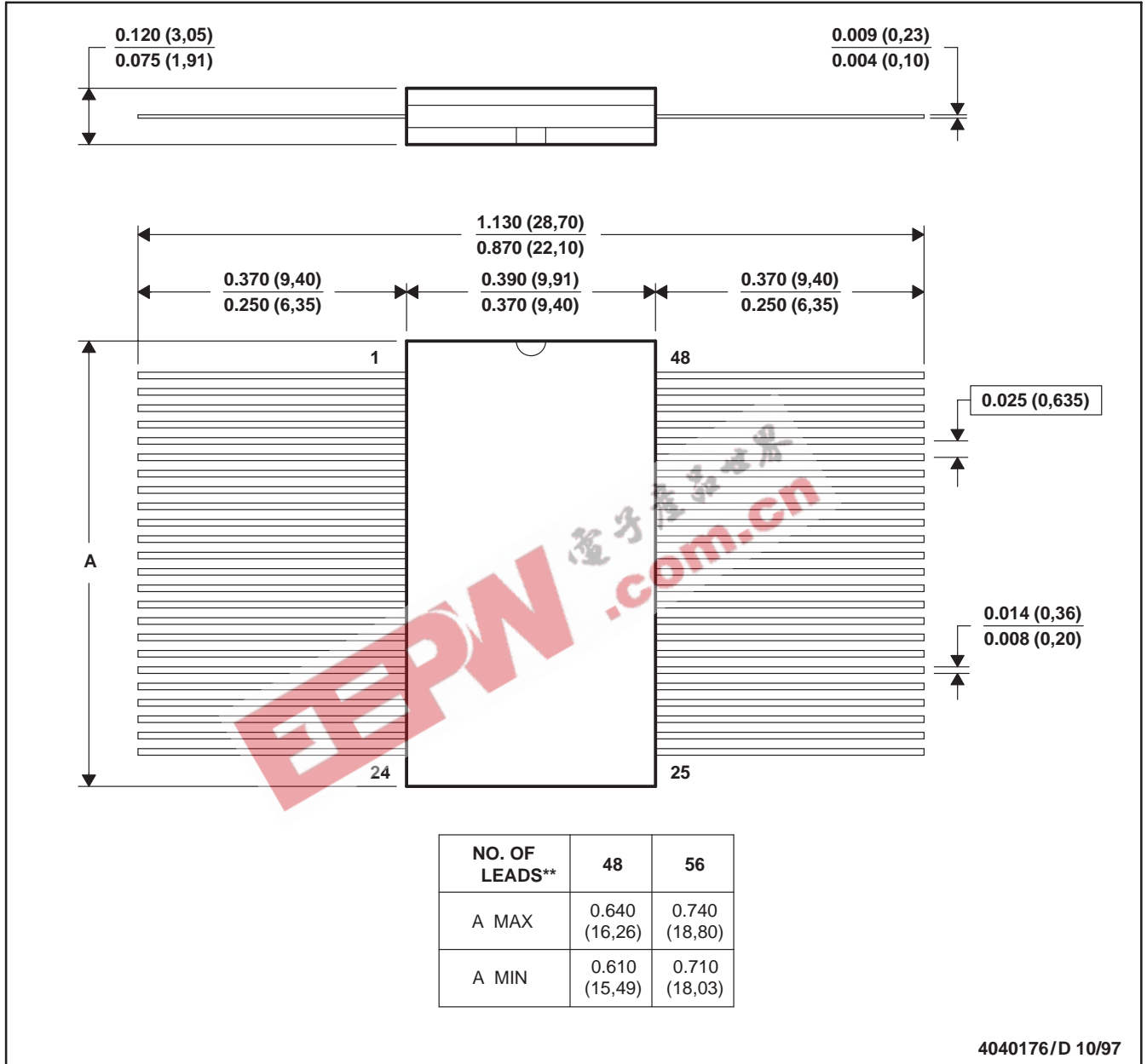
MECHANICAL DATA

MCFP010B – JANUARY 1995 – REVISED NOVEMBER 1997

WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only
 - E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
GDFP1-F56 and JEDEC MO-146AB

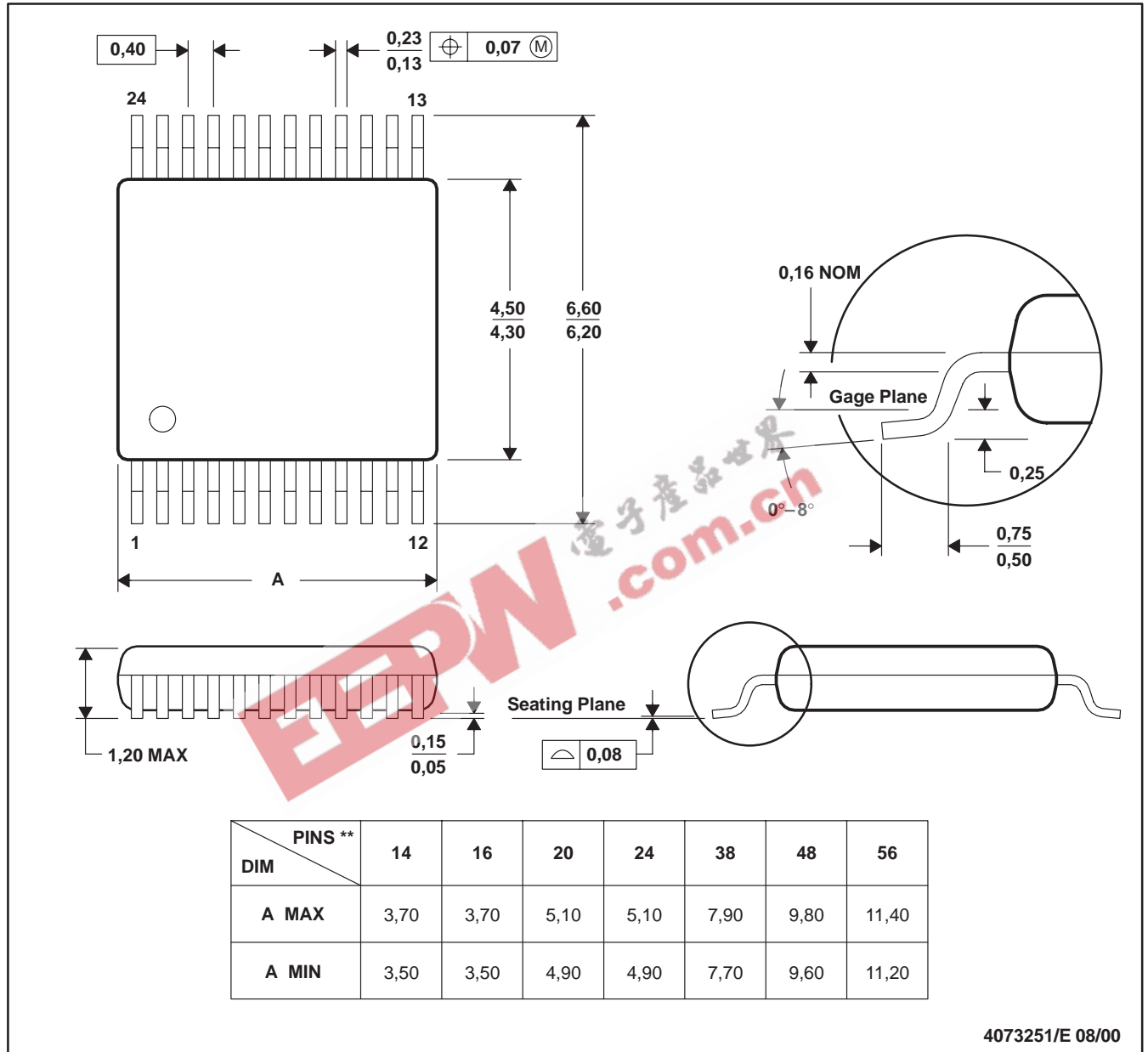
MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

DGV (R-PDSO-G)**

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

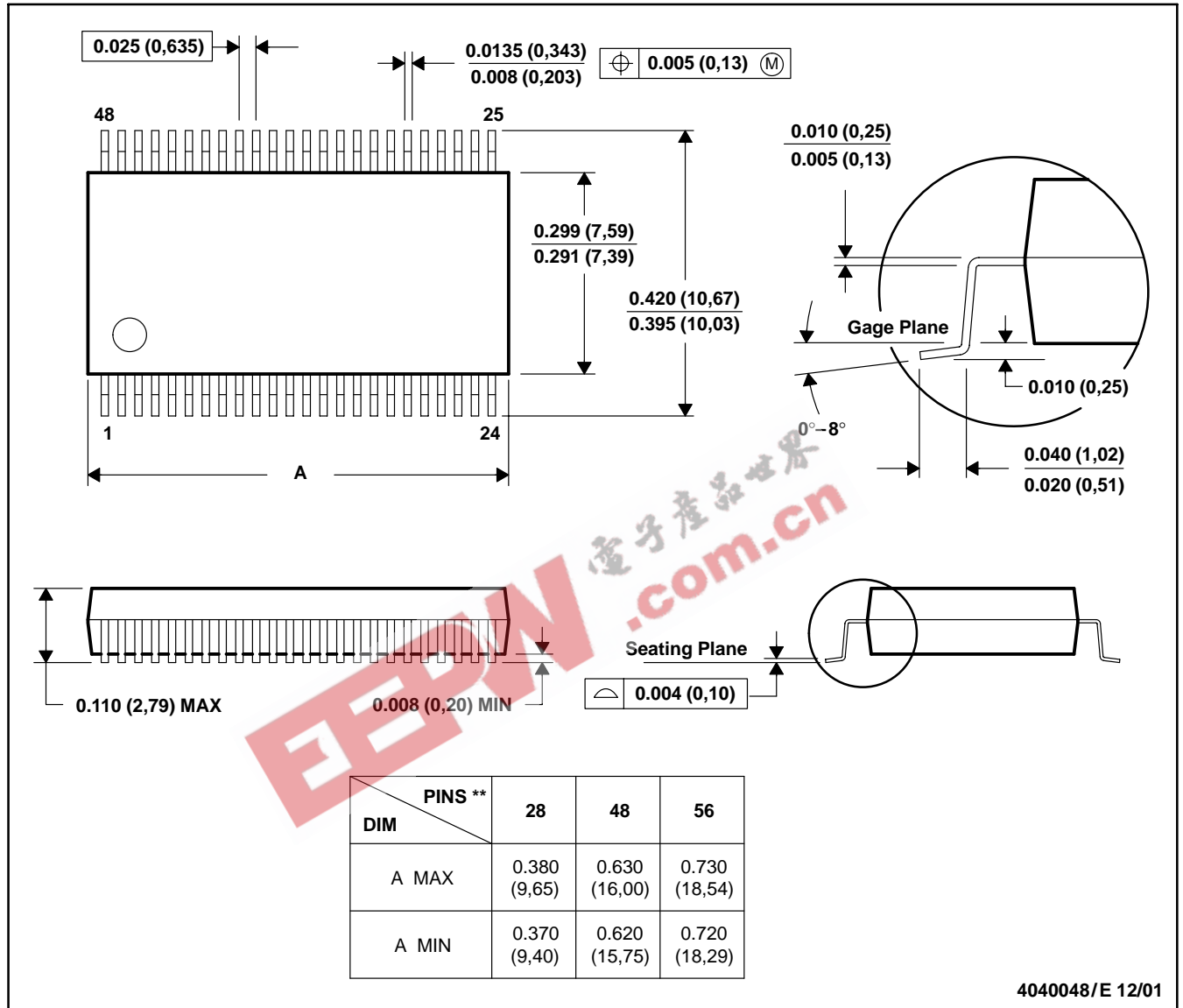
MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

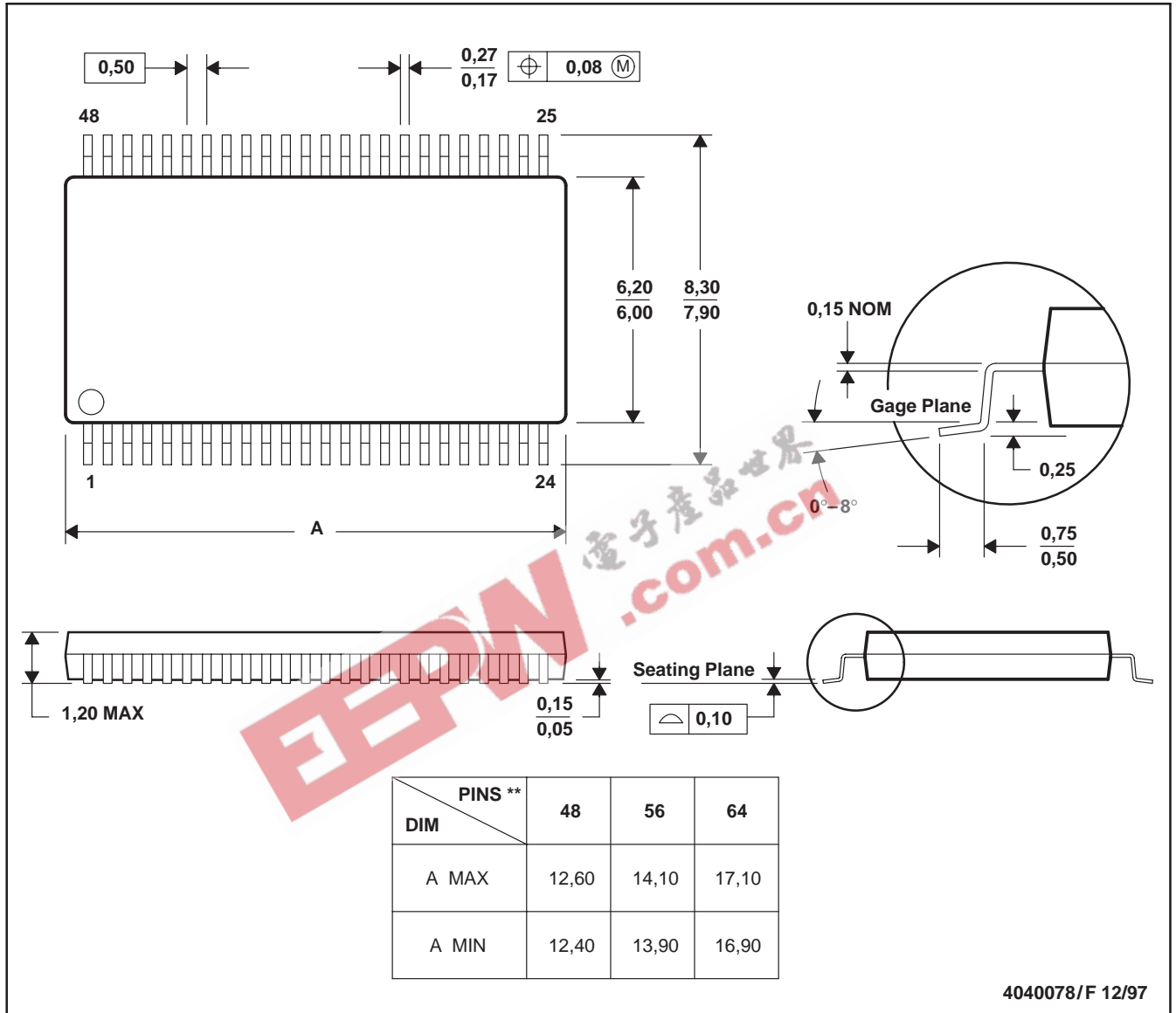
MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

4040078/F 12/97

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