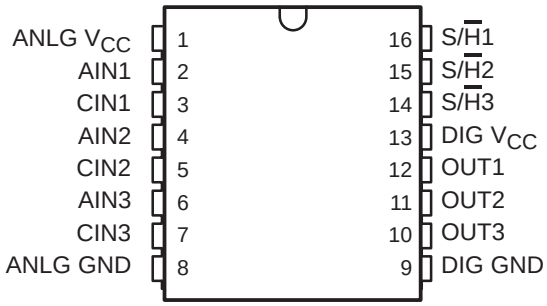
TL1593C
3-CHANNEL SAMPLE-AND-HOLD CIRCUIT

SOCS027B – APRIL 1987 – REVISED JULY 1991

- **Designed for Use With TI Virtual-Phase CCD Image Sensors**
- **Supports Both Color and Monochrome Applications**
- **Contains Three Separate Sample-and-Hold Circuits**
- **Differential Input With 11-dB Gain**
- **5-MHz Sampling Rate on Each Channel**
- **Separate Analog and Digital Supplies for Immunity to Switching Transients**

NS PACKAGE
(TOP VIEW)



description

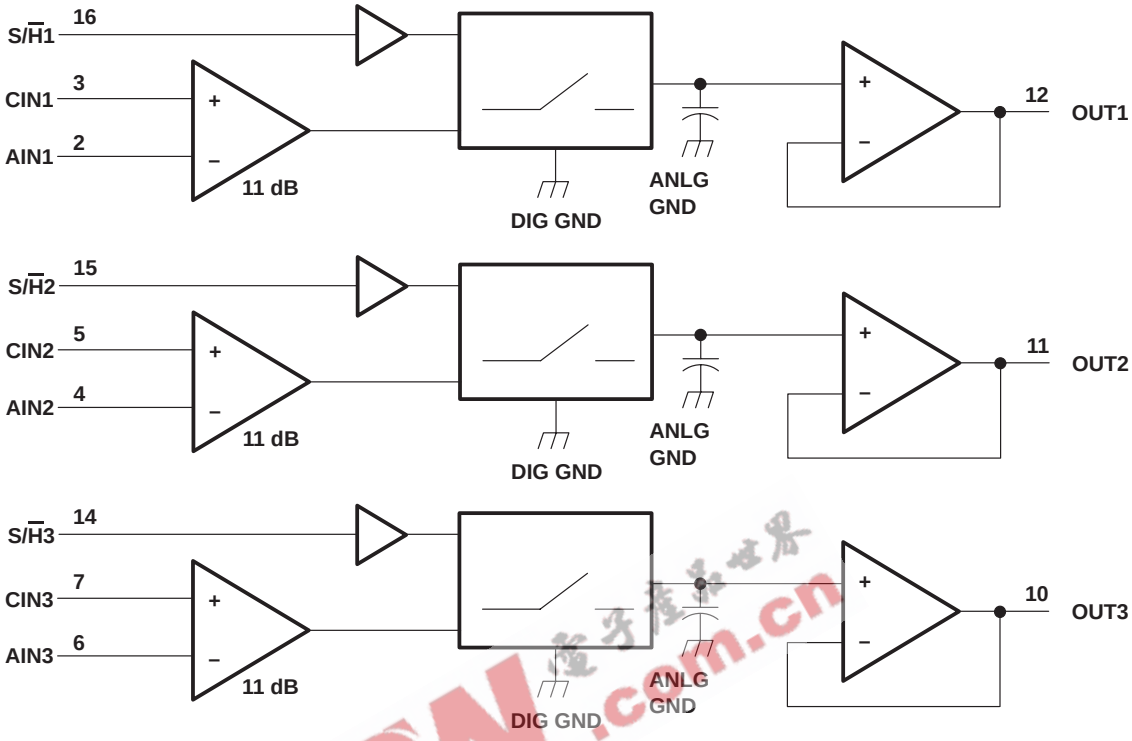
The TL1593C is a three-channel sample-and-hold integrated circuit designed for use in processing video signals generated by TI virtual-phase CCD image sensors. It can be used with one-, two-, and three-channel color and monochrome TI virtual-phase CCDs.

Each sample-and-hold channel consists of a differential-input buffer, a digitally controlled switch, and an output buffer that has high impedance. Separate supply and ground pins are provided for the analog and digital sections to ensure optimum isolation. Internal-hold capacitors are included to reduce the external parts count. The differential inputs allow the amplifier return pin of the imager to be connected to CIN of the sample-and-hold circuit to obtain common-mode rejection for antiblooming clock transients in the CCD. The analog inputs should be capacitively coupled from the CCD outputs to ensure optimum performance.

The TL1593C is supplied in a 16-pin plastic package and is characterized for operation from 0°C to 70°C.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, precautions should be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground. Specific guidelines for handling devices of this type are contained in the publication *Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies* available from Texas Instruments.

schematic



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AIN1	2	I	Channel 1 analog input
AIN2	4	I	Channel 2 analog input
AIN3	6	I	Channel 3 analog input
ANLG GND	8		Analog ground
ANLG V_{CC}	1		Analog supply voltage
CIN1	3	I	Channel 1 compensation input
CIN2	5	I	Channel 2 compensation input
CIN3	7	I	Channel 3 compensation input
DIG GND	9		Digital ground
DIG V_{CC}	13		Digital supply voltage
OUT1	12	O	Channel 1 output
OUT2	11	O	Channel 2 output
OUT3	10	O	Channel 3 output
$\overline{S/H}1$	16	I	Channel 1 sample-and-hold input
$\overline{S/H}2$	15	I	Channel 2 sample-and-hold input
$\overline{S/H}3$	14	I	Channel 3 sample-and-hold input

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Analog supply voltage range, ANLG V_{CC} (see Note 1) . . . . . –0.4 V to 16 V
Digital supply voltage range, DIG V_{CC} . . . . . –0.4 V to 16 V
Input voltage range, V_I: AINn inputs . . . . . –0.4 V to ANLG V_{CC}
CINn inputs . . . . . –0.4 V to ANLG V_{CC}
S/$\overline{H}$n inputs . . . . . –0.4 V to DIG V_{CC}
Continuous total power dissipation at (or below) $T_A \le 25°C$ . . . . . 625 mW
Operating free-air temperature range, T_A . . . . . 30°C to 75°C
Storage temperature range, T_{STG} . . . . . –55°C to 125°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Analog supply voltage, ANLG V_{CC}		10	12	13	V
Digital supply voltage, DIG V_{CC}		10	12	13	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Input bias voltage, V_{IB}	AINn inputs	4.9	5.1	5.3	V
	CINn inputs	2.2	2.4	2.6	
Input voltage, V_I	AINn inputs	V_{IB} – 0.3	V_{IB}	V_{IB} + 0.3	V
	CINn inputs	V_{IB} – 0.2	V_{IB}	V_{IB} + 0.2	
Sampling frequency				5	MHz
Sampling time		55			ns
Operating free-air temperature, T_A		30		75	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

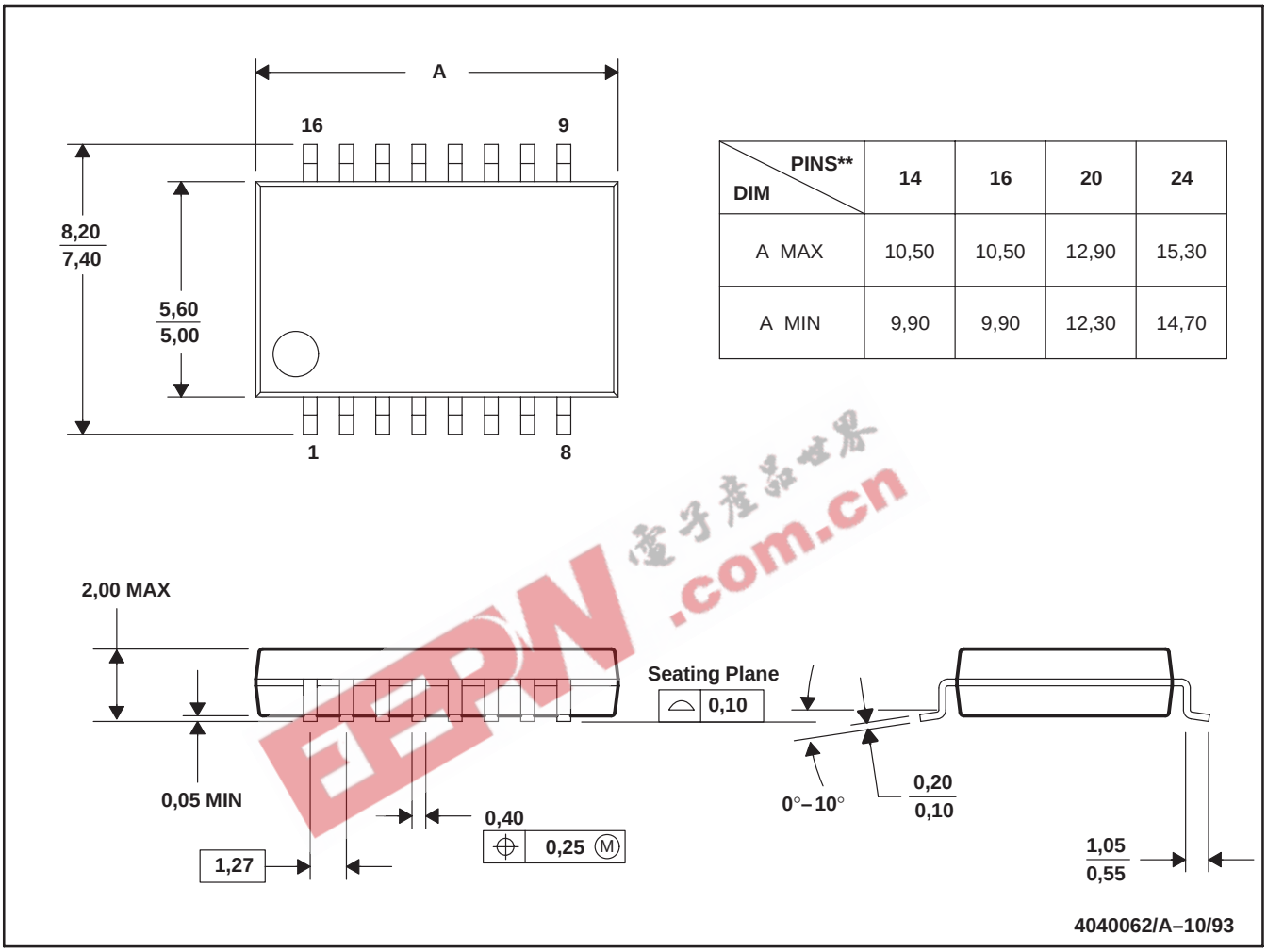
PARAMETER			TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
	Output voltage level				6	6.75	7.5	V
	Output voltage swing				2			V
I_{IH}	High-level input current		V_I = 2.7 V,	DIG V_{CC} = 12 V			10	µA
I_{IL}	Low-level input current		V_I = 0.4 V,	DIG V_{CC} = 12 V		–160	–300	µA
I_{O-}	Output source current				–5			mA
I_{O+}	Output sink current				0.4			mA
I_{CC}	Supply current		DIG V_{CC} = 12 V,	ANLG V_{CC} = 12 V		18.5	28	mA
C_i	Input capacitance	AINn inputs				5	7	pF
		CINn inputs				19	24	
		S/$\overline{H}$n inputs				13	18	
	Input impedance	AINn inputs				100		kΩ
	Output impedance					50	200	Ω

‡ All typical values are at T_A = 25° C.

MECHANICAL DATA

NS/R-PDSO-G** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS**	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

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