



# STD4LNK60Z STF4LNK60Z

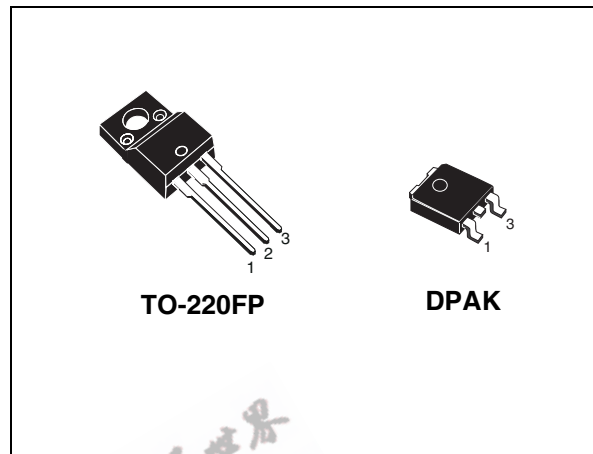
N-channel 600 V, 2.2  $\Omega$ , 3.3 A, TO-220FP, DPAK  
Zener-protected SuperMESH™ Power MOSFET

Preliminary Data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>w</sub>
STD4LNK60Z	600 V	< 2.7 $\Omega$	3.3 A	70 W
STF4LNK60Z	600 V	< 2.7 $\Omega$	3.3 A	25 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Improved ESD capability



## Application

- Switching applications

## Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST's full range of high voltage Power MOSFETs including revolutionary MDmesh™ products.

Figure 1. Internal schematic diagram

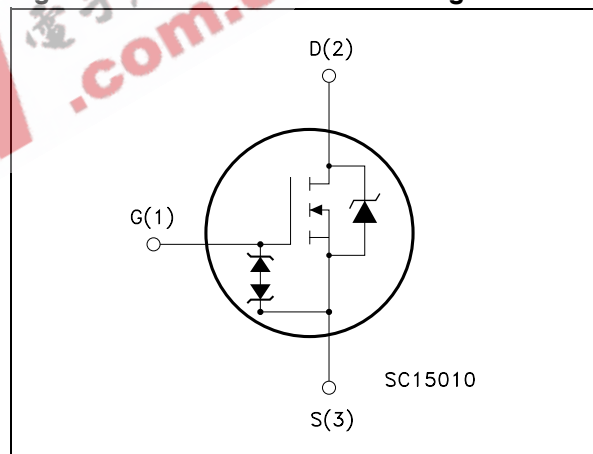


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD4LNK60Z	4LNK60Z	DPAK	Tape and reel
STF4LNK60Z	4LNK60Z	TO-220FP	Tube

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220FP	DPAK	
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	600		V
V <sub>GS</sub>	Gate-source voltage	± 30		V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	3.3 <sup>(1)</sup>	3.3	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	2 <sup>(1)</sup>	2	A
I <sub>DM</sub>	Drain current (pulsed)	13.2 <sup>(1)</sup>	13.2	A
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	25	70	W
	Derating factor	0.2	0.56	W/°C
V <sub>ISO</sub>	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T <sub>C</sub> =25 °C)	2500	--	V
T <sub>j</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature	-55 to 150		°C

1. Limited by package

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		TO-220FP	DPAK	
R <sub>thj-case</sub>	Thermal resistance junction-case	5	1.79	°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb <sup>(1)</sup>	--	50	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-amb	62.5	--	°C/W
T <sub>l</sub>	Maximum lead temperature for soldering purpose	300		°C

1. Minimum footprint

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>jmax</sub> )	TBD	A
E <sub>AS</sub>	Single pulse avalanche energy <sup>(1)</sup>	TBD	mJ

1. Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = I<sub>AR</sub>, V<sub>DD</sub> = 50 V

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating}$ , $T_c=125\text{ }^{\circ}\text{C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2.7\text{ A}$		2.2	2.7	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		400		pF
$C_{oss}$	Output capacitance			50		pF
$C_{rss}$	Reverse transfer capacitance			10		pF
$C_{oss\text{ eq.}}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0$		44.4		pF
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 3.3\text{ A}$		14		nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{ V}$		TBD		nC
$Q_{gd}$	Gate-drain charge	(see Figure 3)		TBD		nC

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 3.3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 2)		7.5		ns
$t_r$	Rise time				19.5	ns
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 300\text{ V}$ , $I_D = 3.3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 2)		28		ns
$t_f$	Fall time				24	ns

Table 8. Source drain diode

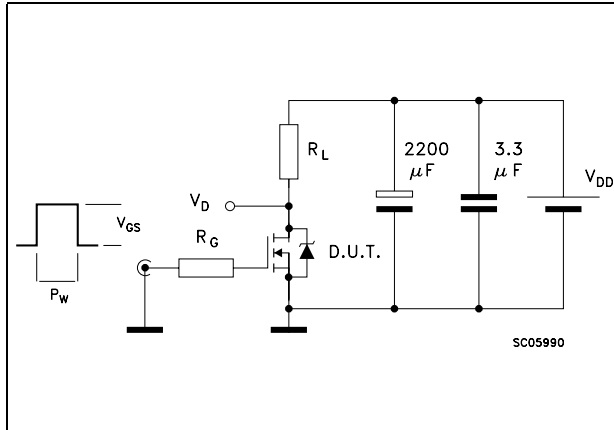
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				3.3	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				13.2	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 3.3 \text{ A}$ , $V_{GS} = 0$			TBD	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 3.3 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 480 \text{ V}$ , $T_j = 150^\circ\text{C}$ (see Figure 7)		TBD		ns
$Q_{rr}$	Reverse recovery charge			TBD		nC
$I_{RRM}$	Reverse recovery current			TBD		A

1. Pulse width limited by package
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

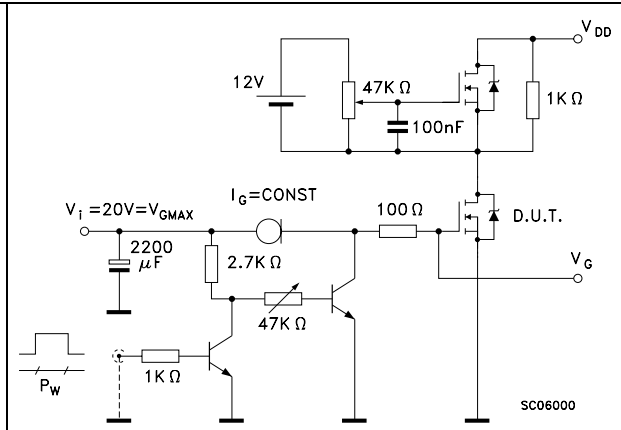
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### 3 Test circuits

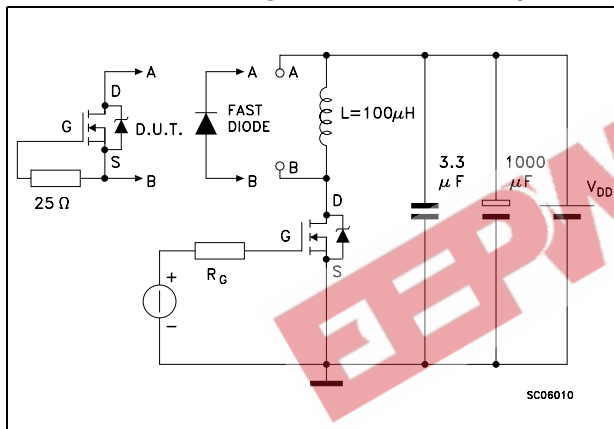
**Figure 2. Switching times test circuit for resistive load**



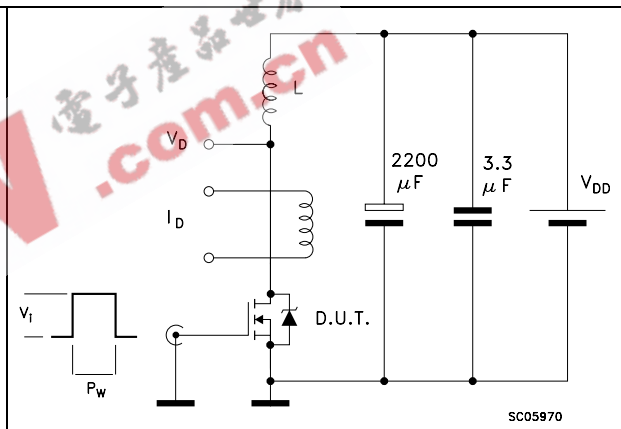
**Figure 3. Gate charge test circuit**



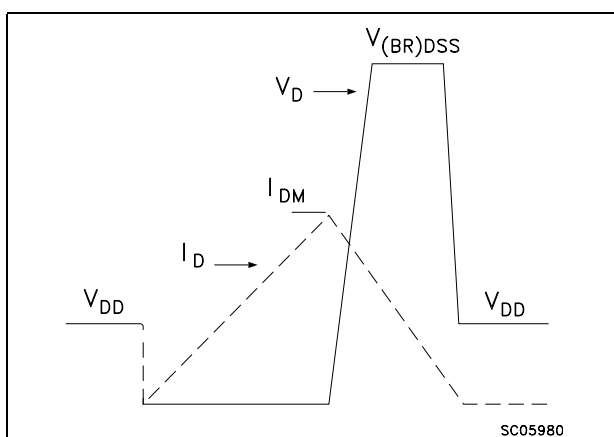
**Figure 4. Test circuit for inductive load switching and diode recovery times**



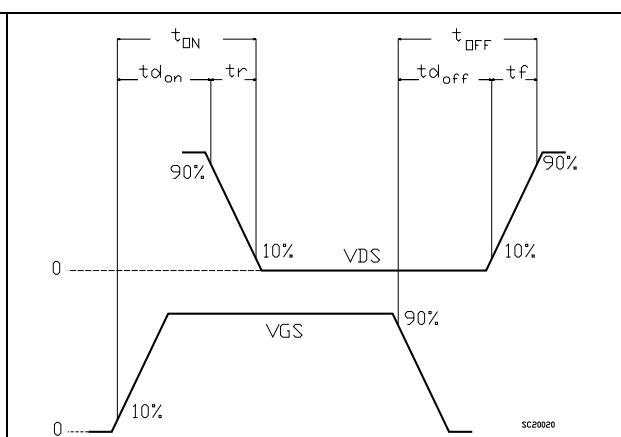
**Figure 5. Unclamped inductive load test circuit**



**Figure 6. Unclamped inductive waveform**



**Figure 7. Switching time waveform**



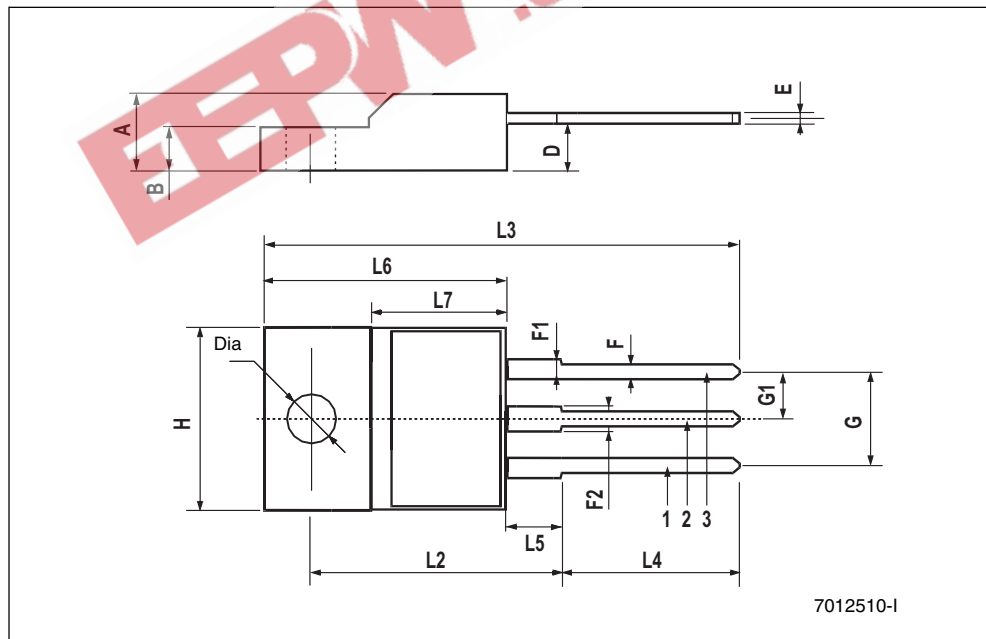
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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TO-220FP mechanical data

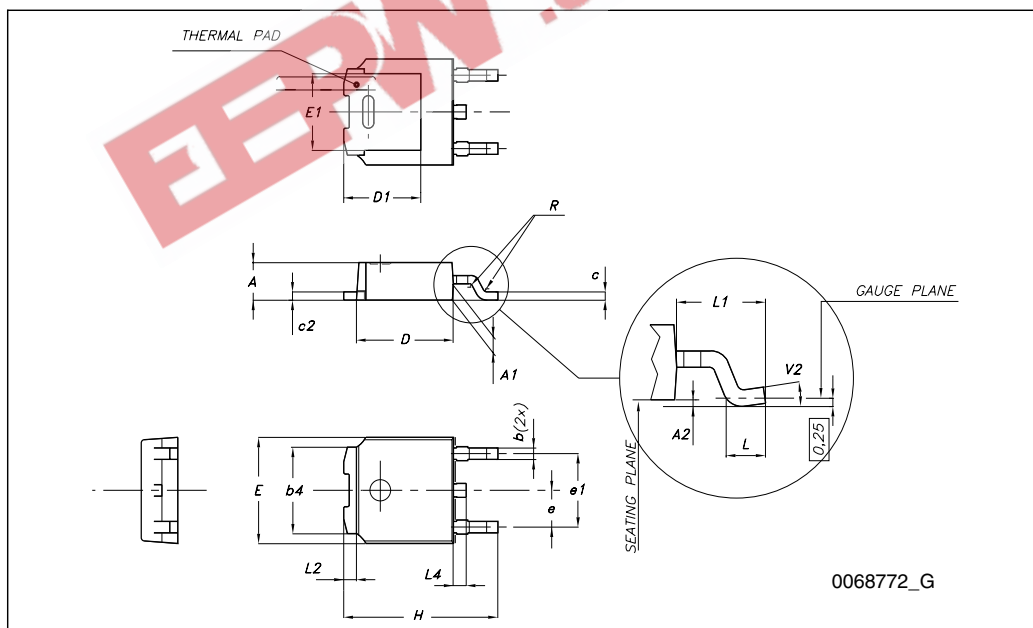
Dim.	mm.			inch		
	Min.	Typ	Max.	Min.	Typ.	Max.
A	4.40		4.60	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.70	0.017		0.027
F	0.75		1.00	0.030		0.039
F1	1.15		1.50	0.045		0.067
F2	1.15		1.50	0.045		0.067
G	4.95		5.20	0.195		0.204
G1	2.40		2.70	0.094		0.106
H	10		10.40	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.80		10.60	0.385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.90		16.40	0.626		0.645
L7	9		9.30	0.354		0.366
Dia	3		3.2	0.118		0.126





TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
24-Jul-2008	1	Initial release.

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