

# 4035B

## 4-BIT UNIVERSAL SHIFT REGISTER

**DESCRIPTION** — The 4035B is a fully synchronous edge-triggered 4-Bit Shift Register with a Clock Input (CP), four synchronous Parallel Data Inputs ( $P_0$ – $P_3$ ), two synchronous Serial Data Inputs (J,  $\bar{K}$ ), a synchronous Parallel Enable Input (PE), Buffered Parallel Outputs from all 4-bit positions ( $Q_0$ – $Q_3$ ), a True/Complement Input ( $T/\bar{C}$ ) and an overriding asynchronous Master Reset Input (MR).

Operation is synchronous (except for Master Reset) and is edge-triggered on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is HIGH, data is loaded into the register from Parallel Inputs ( $P_0$ – $P_3$ ) on the LOW-to-HIGH transition of the Clock Input (CP). When the Parallel Enable Input (PE) is LOW, data is shifted into the first register position from the Serial Data Inputs (J,  $\bar{K}$ ) and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of the Clock Input (CP). D-type entry is obtained by tying the two Serial Data Inputs (J,  $\bar{K}$ ) together.

The Outputs ( $Q_0$ – $Q_3$ ) are either inverting or non-inverting, depending on the True/Complement Input ( $T/\bar{C}$ ). With the  $T/\bar{C}$  Input HIGH, the Outputs ( $Q_0$ – $Q_3$ ) are non-inverting (Active HIGH). With the  $T/\bar{C}$  Input LOW, the Outputs ( $Q_0$ – $Q_3$ ) are inverting (Active LOW).

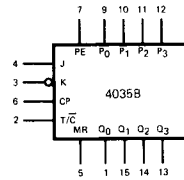
A HIGH on the Master Reset Input (MR) resets all four bit positions ( $Q_0$ – $Q_3$  = LOW if  $T/\bar{C}$  = HIGH,  $Q_0$ – $Q_3$  = HIGH if  $T/\bar{C}$  = LOW) independent of all other input conditions.

- TYPICAL SHIFT FREQUENCY OF 17 MHz AT  $V_{DD} = 10 V$
- J,  $\bar{K}$  INPUTS TO THE FIRST STAGE
- $T/\bar{C}$  INPUT FOR TRUE OR COMPLEMENTARY OUTPUTS
- SYNCHRONOUS PARALLEL ENABLE
- CLOCK EDGE-TRIGGERED ON LOW-TO-HIGH TRANSITION
- ASYNCHRONOUS MASTER RESET

### PIN NAMES

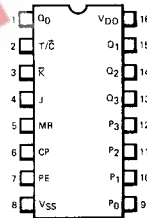
PE	Parallel Enable Input
$P_0$ – $P_3$	Parallel Data Inputs
J	First Stage J Input (Active HIGH)
$\bar{K}$	First Stage K Input (Active LOW)
CP	Clock Input (L→H Edge-Triggered)
$T/\bar{C}$	True/Complement Input
MR	Master Reset Input
$Q_0$ – $Q_3$	Buffered Parallel Outputs

### LOGIC SYMBOL



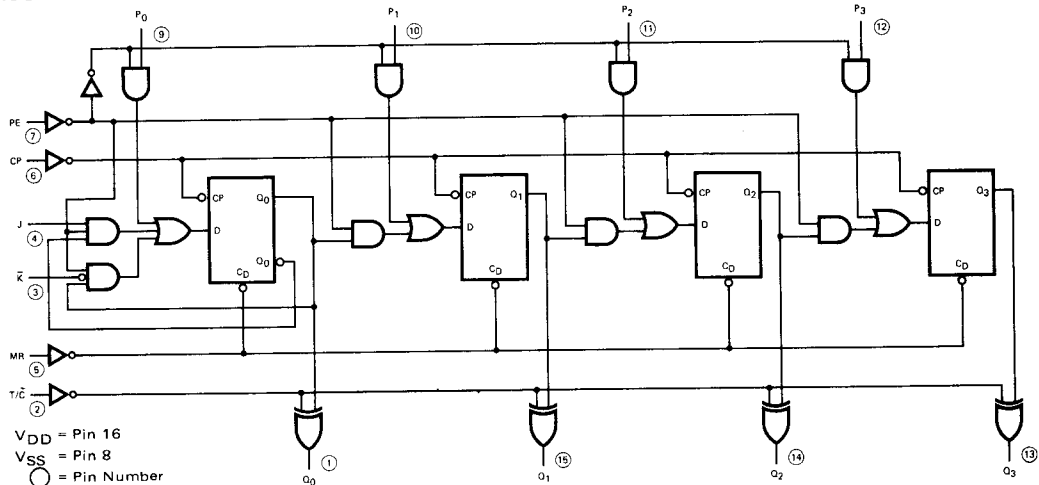
$V_{DD}$  = Pin 16  
 $V_{SS}$  = Pin 8

### CONNECTION DIAGRAM DIP (TOP VIEW)



**NOTE:**  
 The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

### LOGIC DIAGRAM



$V_{DD}$  = Pin 16  
 $V_{SS}$  = Pin 8  
 ○ = Pin Number

FAIRCHILD CMOS • 4035B

DC CHARACTERISTICS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V (See Note 1)

SYMBOL	PARAMETER	LIMITS									UNITS	TEMP	TEST CONDITIONS	
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V						
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
$I_{DD}$	Quiescent Power	XC			20			40			80	$\mu$ A	MIN, 25°C	All inputs at 0 V or $V_{DD}$
					150			300			600		MAX	
	Supply Current	XM			5			10			20	$\mu$ A	MIN, 25°C	
					150			300			600		MAX	

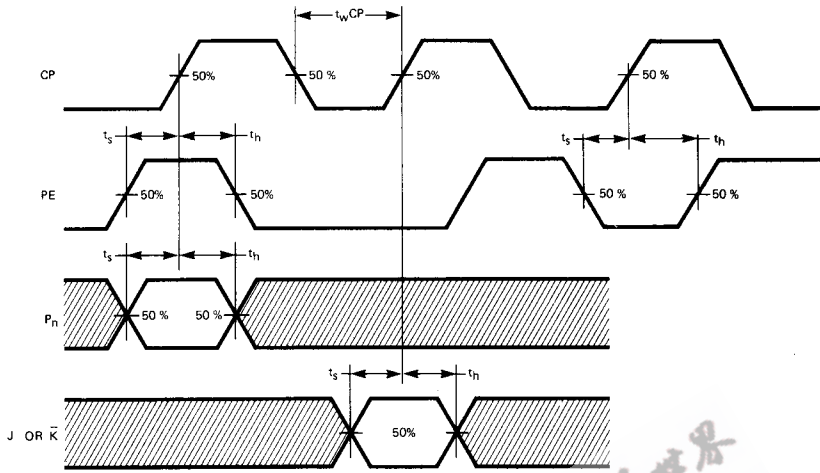
AC CHARACTERISTICS AND SET-UP REQUIREMENTS:  $V_{DD}$  as shown,  $V_{SS} = 0$  V,  $T_A = 25^\circ$ C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		$V_{DD} = 5$ V			$V_{DD} = 10$ V			$V_{DD} = 15$ V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
$t_{PLH}$	Propagation Delay, CP to $Q_n$		200	400		90	180	60	140		ns	$C_L = 50$ pF, $R_L = 200$ k $\Omega$ Input Transition Times $\leq 20$ ns
$t_{PHL}$			200	400		90	180	60	140			
$t_{PLH}$	Propagation Delay, MR to $Q_n$		250	500		120	230	75	180		ns	
$t_{PHL}$			250	500		120	230	75	180			
$t_{PLH}$	Propagation Delay, T/ $\bar{C}$ to $Q_n$		125	250		55	120	40	95		ns	
$t_{PHL}$			125	250		55	120	40	95			
$t_{TLH}$	Output Transition Time		85	135		45	75	30	45		ns	
$t_{THL}$			85	135		45	75	30	45			
$t_{wCP}$	CP Minimum Pulse Width	125	50		55	20		44	14		ns	
$t_{wMR}$	MR Minimum Pulse Width	150	60		70	25		56	20		ns	
$t_{rec}$	MR Recovery Time	120	60		54	30		43	22		ns	
$t_s$	Set-Up Time, $P_n$ to CP	250	100		110	46		88	32		ns	
$t_h$	Hold Time, $P_n$ to CP	10	-90		5	-32		0	-22			
$t_s$	Set-Up Time, PE to CP	250	100		110	46		88	32		ns	
$t_h$	Hold Time, PE to CP	10	-90		5	-32		0	-22			
$t_s$	Set-Up Time, J, $\bar{K}$ to CP	275	130		125	48		100	30		ns	
$t_h$	Hold Time, J, $\bar{K}$ to CP	25	-100		10	-37		5	-23			
$f_{MAX}$	Maximum Input Clock Frequency (Note 3)	4	8		8	17		10	20		MHz	

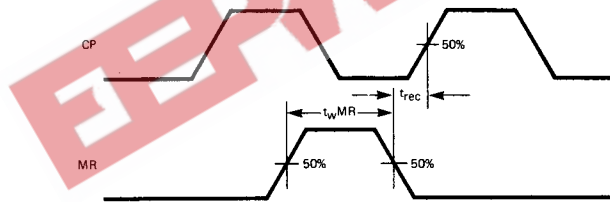
NOTES:

1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For  $t_{MAX}$ , input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15  $\mu$ s at  $V_{DD} = 5$  V, 4  $\mu$ s at  $V_{DD} = 10$  V, and 3  $\mu$ s at  $V_{DD} = 15$  V.

SWITCHING WAVEFORMS



MINIMUM CP PULSE WIDTH AND SET-UP AND HOLD TIMES, PE TO CP, P<sub>n</sub> TO CP, AND J OR K TO CP



MR RECOVERY TIME AND MINIMUM MR PULSE WIDTH

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.