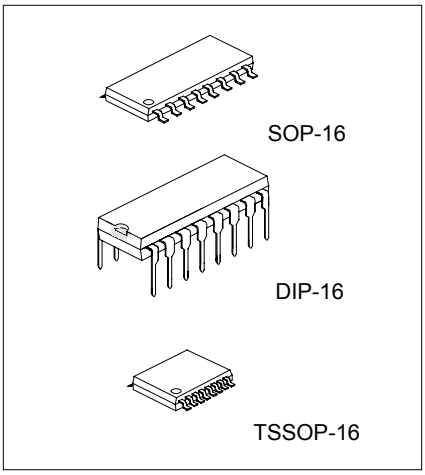
ANALOG MULTIPLEXERS/ DEMULTIPLEXERS



*Pb-free plating product number: 4053L

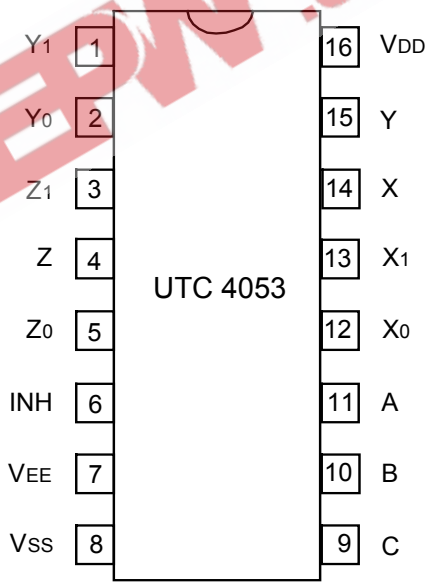
DESCRIPTION

The UTC **4053 are** Triple SPDT analog multiplexers for application as digitally–controlled analog switches.

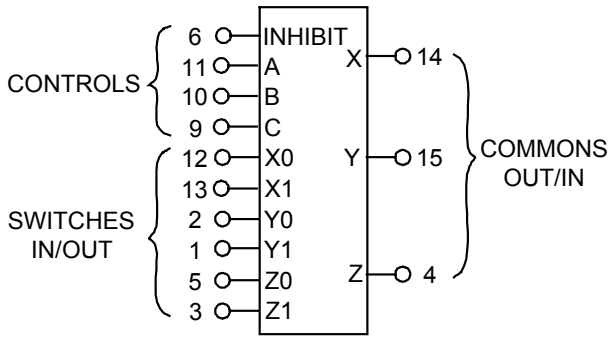
FEATURES

* Analog Voltage Range (V_{DD} – V_{EE}) = 3.0 ~ 18 V
  Note: V_{EE} must be $\leqq V_{SS}$
* Linearized Transfer Characteristics
* Pin–to–Pin Replacement for CD4053

PIN CONFIGURATIONS



UTC 4053 Triple 2–Channel Analog Multiplexer/Demultiplexer



V_{DD} = PIN 16
V_{SS} = PIN 8
V_{EE} = PIN 7

Note: Control Inputs referenced to V_{SS}, Analog Inputs and Outputs reference to V_{EE}. V_{EE} must be≦V_{SS}.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage (Referenced to V_{EE}, V_{SS}≧V_{EE})	V_{DD}	-0.5 ~ +18.0	V
Input or Output Voltage (DC or Transient) (Referenced to V_{SS} for Control Inputs and V_{EE} for Switch I/O)	V_{in}, V_{out}	-0.5 ~ V_{DD} +0.5	V
Input Current (DC or Transient), per Control Pin	I_{in}	±10	mA
Switch Through Current	I_{SW}	±25	mA
Power Dissipation. Per Package**	P_D	500	mW
Storage Temperature	T_{stg}	-65 ~ +150	℃
Lead Temperature (8 - Second Soldering)	T_{Lead}	260	℃

* Maximum Ratings are those values beyond which damage to the device may occur.
** Temperature Derating: “DIP and SOP” Packages: – 7.0 mW/℃ From 65℃ ~ 125℃

ELECTRICAL CHARACTERISTICS

(Ta=25℃, unless otherwise indicated.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
SUPPLY REQUIREMENTS (Voltages Referenced to V_{EE})						
Power Supply Voltage Range	V_{DD}	V_{DD} – 3.0≧V_{SS}≧V_{EE}	3.0		18	V
Quiescent Current per Package	I_{DD}	Control Inputs: Vin = V_{SS} or V_{DD} Switch I/O: V_{EE} ≦$V_{I/O}$ ≦V_{DD}, and ΔVswitch≦500mV* V_{DD}=5.0V V_{DD}=10V V_{DD}=15V		 0.005 0.010 0.015	 5.0 10 20	μA
Total Supply Current (Dynamic Plus Quiescent, Per Package)	$I_{D(AV)}$	T_a=25℃ only (The channel component, (Vin - Vout)/Ron, is not included.) V_{DD}=5.0V V_{DD}=10V V_{DD}=15V	 (0.07 μA/kHz) f + I_{DD} Typical (0.20 μA/kHz) f + I_{DD} (0.36 μA/kHz) f + I_{DD}			μA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
CONTROL INPUTS – INHIBIT A, B, C (Voltages Referenced to V_{SS})						
Low – Level Input Voltage	V_{IL}	Ron= per spec, Ioff = per spec V_{DD}=5.0V V_{DD}=10V V_{DD}=15V		 2.25 4.50 6.75	 1.5 3.0 4.0	V
High – Level Input Voltage	V_{IH}	Ron= per spec, Ioff = per spec V_{DD}=5.0V V_{DD}=10V V_{DD}=15V	 3.5 7.0 11	 2.75 5.50 8.25		V
Input Leakage Current	Iin	Vin= 0 or V_{DD}, V_{DD}=15V		±0.00001	±0.1	μA
Input Capacitance	Cin			5.0	7.5	pF
SWITCHES IN/OUT AND COMMONS OUT/IN -- X, Y, Z (Voltages Referenced to V_{EE})						
Recommended Peak–to–Peak Voltage Into or Out of the Switch	$V_{I/O}$	Channel On or Off	0		V_{DD}	V_{PP}
Recommended Static or Dynamic Voltage Across the Switch** (Figure 3)	ΔVswitch	Channel On	0		600	mV
Output Offset Voltage	V_{OO}	Vin = 0V, No Load		10		μV
ON Resistance	Ron	ΔVswitch≦500mV* Vin = V_{IL} or V_{IH} (Control), and Vin = 0 to V_{DD} (Switch) V_{DD}=5.0V V_{DD}=10V V_{DD}=15V		 250 120 80	 1050 500 280	Ω
△ON Resistance Between Any Two Channels in the Same Package	ΔRon	V_{DD}=5.0V V_{DD}=10V V_{DD}=15V		25 10 10	70 50 45	Ω
Off–Channel Leakage Current (Figure 8)	Ioff	Vin = V_{IL} or V_{IH} (Control) Channel to Channel or Any One Channel, V_{DD}=15V		±0.05	±100	nA
Capacitance, Switch I/O	$C_{I/O}$	Inhibit = V_{DD}		10		pF
Capacitance, Common O/I	$C_{O/I}$	Inhibit = V_{DD}		17		pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	Pins Not Adjacent Pins Adjacent		0.15 0.47		pF

#Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.

* For voltage drops across the switch (ΔVswitch) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See second page of this data sheet.)

ELECTRICAL CHARACTERISTICS*

(C_L = 50pF, T_a=25℃, $V_{EE} \leqq V_{SS}$, unless otherwise indicated.)

PARAMETER	SYMBOL	$V_{DD} - V_{EE}$ Vdc	TEST CONDITIONS	MIN	TYP#	MAX	UNIT
Propagation Delay Times (Figure 4) Switch Input to Switch Output (R_L = 10 kΩ)	t_{PLH}, t_{PHL}	5.0 10 15	t_{PLH}, t_{PHL} = (0.17 ns/pF) C_L + 16.5 ns t_{PLH}, t_{PHL} = (0.08 ns/pF) C_L + 4.0 ns t_{PLH}, t_{PHL} = (0.06 ns/pF) C_L + 3.0 ns		25 8.0 6.0	65 20 15	ns
Inhibit to Output	t_{PHZ}, t_{PLZ} t_{PZH}, t_{PZL}	5.0 10 15	(R_L=10kΩ, V_{EE}=V_{SS})Output “1” or “0” to High Impedance, or High Impedance to “1” or “0” Level		275 140 110	550 280 220	ns
Control Input to Output	t_{PLH}, t_{PHL}	5.0 10 15	R_L = 10 kΩ, V_{EE} = V_{SS}		300 120 80	600 240 160	ns
Second Harmonic Distortion		10	R_L = 10KΩ, f = 1 kHz, Vin = 5 V_{PP}		0.07		%
Bandwidth (Figure 5)	BW	10	R_L = 1kΩ, Vin = 1/2 (V_{DD}–V_{EE}) p–p, C_L = 50pF, 20 Log (Vout/Vin) = -3dB)		17		MHz
Off Channel Feedthrough Attenuation (Figure 5)		10	R_L = 1KΩ, Vin = 1/2 (V_{DD} – V_{EE}) p–p fin = 55 MHz		-50		dB
Channel Separation (Figure 6)		10	R_L = 1 kΩ, Vin = 1/2 (V_{DD}–V_{EE}) p–p fin = 3.0 MHz		-50		dB
Crosstalk, Control Input to Common O/I (Figure 7)		10	R_1 = 1 kΩ, R_L = 10 kΩ Control t_{TLH} = t_{THL} = 20 ns, Inhibit = V_{SS})		75		mV

* The formulas given are for the typical characteristics only at 25℃.

Data labelled “Typ” is not lo be used for design purposes but In intended as an indication of the IC’s potential performance.

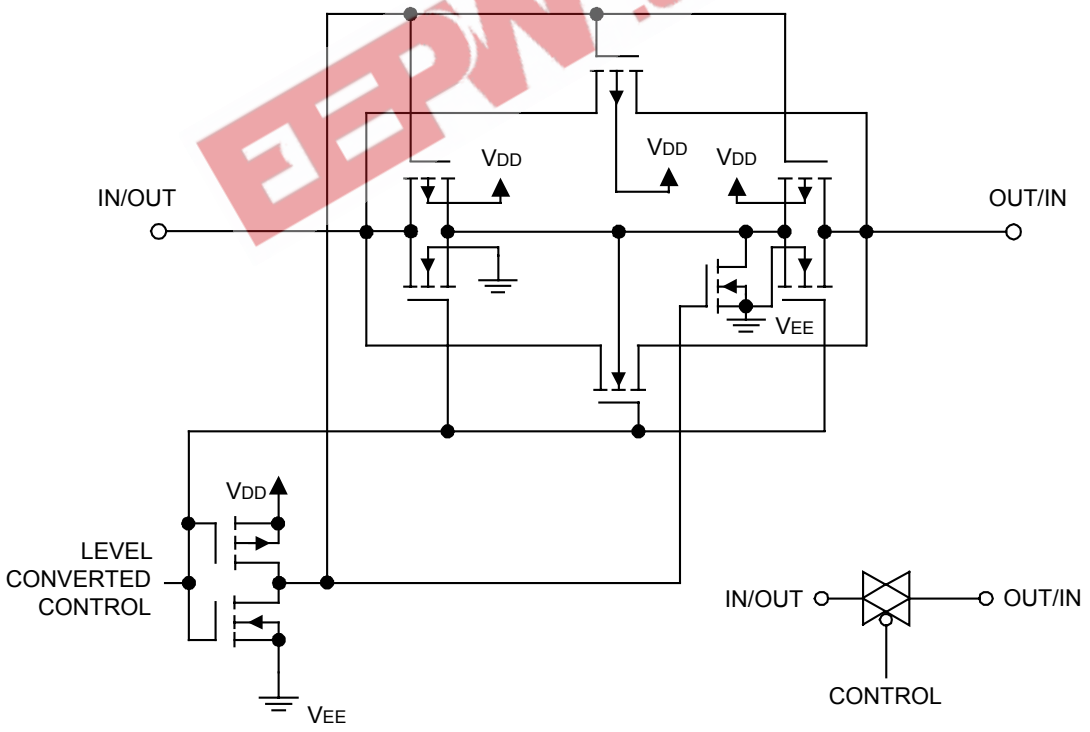


Figure 1. Switch Circuit Schematic

TRUTH TABLE

Control Inputs				ON Switches		
Inhibit	Select					
	C	B	A	UTC 4053		
0	0	0	0	Z0	Y0	X0
0	0	0	1	Z0	Y0	X1
0	0	1	0	Z0	Y1	X0
0	0	1	1	Z0	Y1	X1
0	1	0	0	Z1	Y0	X0
0	1	0	1	Z1	Y0	X1
0	1	1	0	Z1	Y1	X0
0	1	1	1	Z1	Y1	X1
1	x	x	x	None		

x = Don't Care

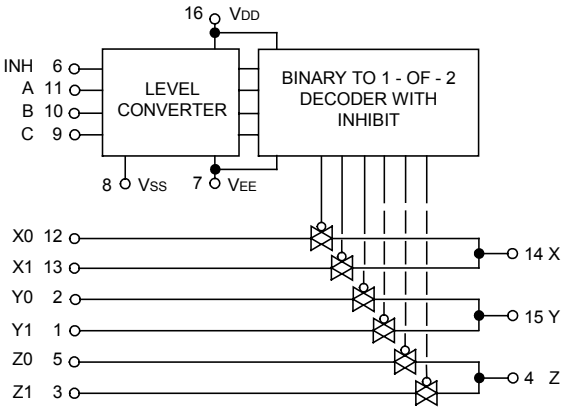


Figure 2. UTC 4053 Functional Diagram