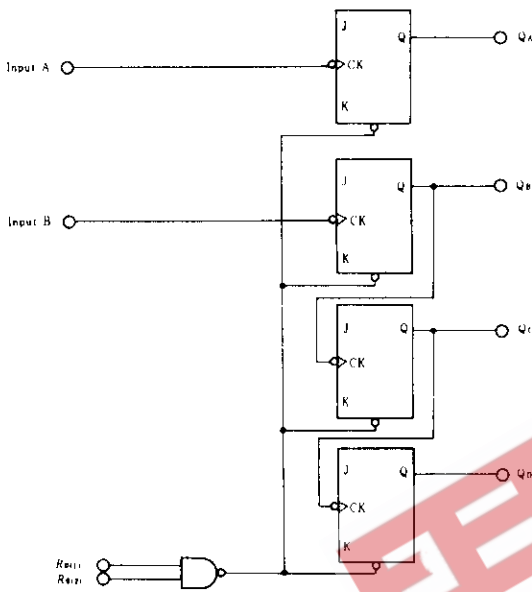


# HD74LS93 • 4-bit Binary Counters

The HD74LS93 contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and three-state binary counter for divide-by-eight. To use this maximum count length of this counter, the B input is connected to the  $Q_A$  output. The input count pulses are applied to input A and the outputs are described in the appropriate function table.

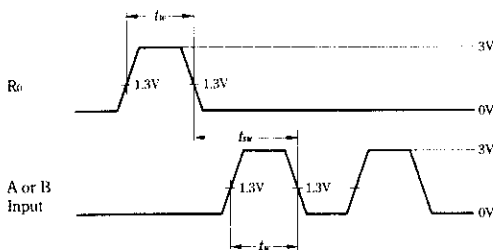
## ■ BLOCK DIAGRAM



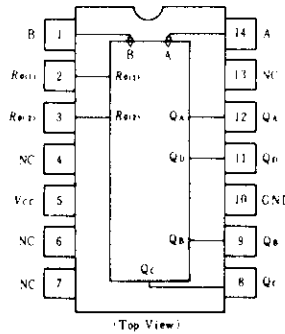
## ■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Count frequency	A input	0	—	32	MHz
	B input	0	—	16	
Pulse width	A input	15	—	—	ns
	B input	30	—	—	
	Reset inputs	15	—	—	
Setup time	$t_{su}$	25	—	—	ns

## ■ TIMING DEFINITION



## ■ PIN ARRANGEMENT



## ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	$V_{cc}$	7.0	V
Input voltage	R Inputs	7.0	V
	A, B Inputs	5.5	V
Operating temperature range	$T_{opr}$	-20 ~ +75	°C
Storage temperature range	$T_{stg}$	-65 ~ +150	°C

## ■ FUNCTION TABLE

### ● Reset/Count Function Table

Reset Inputs		Outputs			
R0(1)	R0(2)	QD	QC	QB	QA
H	H	L	L	L	L
L	X	Count			
X	L	Count			

### ● BCD Count Sequence (Notes 1)

Count	Outputs			
	QD	QC	QB	QA
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Notes) 1. Output  $Q_A$  is connected to input B for BCD count.  
2. H; high level, L; low level, X; irrelevant

# HD74LS93

## ■ ELECTRICAL CHARACTERISTICS ( $T_a = -20 \sim +75^\circ\text{C}$ )

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	$V_{IH}$		2.0	—	—	V	
	$V_{IL}$		—	—	0.8	V	
Output voltage	$V_{OH}$	$V_{CC}=4.75\text{V}$ , $V_{IH}=2\text{V}$ , $V_{IL}=0.8\text{V}$ , $I_{OH}=-400\mu\text{A}$	2.7	—	—	V	
	$V_{OL}$	$V_{CC}=4.75\text{V}$ , $V_{IH}=2\text{V}$ , $V_{IL}=0.8\text{V}$	$I_{OL}=4\text{mA}^{**}$ $I_{OL}=8\text{mA}^{**}$	—	—	0.4 0.5	V
Input current	Any Reset	$I_{IL}$	$V_{CC}=5.25\text{V}$ , $V_I=0.4\text{V}$	—	—	-0.4	mA
	A input			—	—	-2.4	
	B input			—	—	-1.6	
	Any Reset	$I_{IH}$	$V_{CC}=5.25\text{V}$ , $V_I=2.7\text{V}$	—	—	20	$\mu\text{A}$
	A input			—	—	40	
	B input			—	—	40	
Any Reset	$I_I$	$V_{CC}=5.25\text{V}$	$V_I=7\text{V}$	—	—	0.1	mA
A input			$V_I=5.5\text{V}$	—	—	0.2	
B input			$V_I=5.5\text{V}$	—	—	0.2	
Short-circuit output current	$I_{OS}$	$V_{CC}=5.25\text{V}$	-20	—	-100	mA	
Supply current	$I_{CC}^{***}$	$V_{CC}=5.25\text{V}$	—	9	15	mA	
Input clamp voltage	$V_{IK}$	$V_{CC}=4.75\text{V}$ , $I_{IN}=-18\text{mA}$	—	—	-1.5	V	

\*  $V_{CC}=5\text{V}$ ,  $T_a=25^\circ\text{C}$   
 \*\*  $Q_A$  output is tested at specified  $I_{OL}$  plus the limit value of  $I_{IL}$  for the B input. This permits driving the B input while maintaining full fan-out capability.

\*\*\*  $I_{CC}$  is measured with all outputs open, both  $R_0$  inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

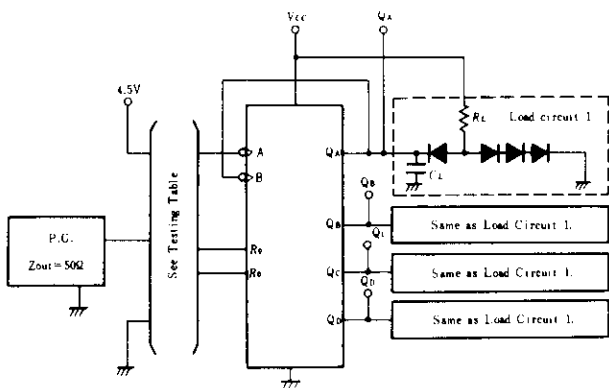
## ■ SWITCHING CHARACTERISTICS ( $V_{CC}=5\text{V}$ , $T_a=25^\circ\text{C}$ )

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum count frequency	$f_{max}$	A	$Q_A$	$C_L=15\text{pF}$ , $R_L=2\text{k}\Omega$	32	42	—	MHz
		B	$Q_B$		16	—	—	
Propagation delay time	$t_{PLH}$	A	$Q_A$		—	10	16	ns
	$t_{PHL}$				—	12	18	
	$t_{PLH}$	A	$Q_D$		—	46	70	ns
	$t_{PHL}$				—	46	70	
	$t_{PLH}$	B	$Q_B$		—	10	16	ns
	$t_{PHL}$				—	14	21	
	$t_{PLH}$	B	$Q_C$		—	21	32	ns
	$t_{PHL}$				—	23	35	
	$t_{PLH}$	B	$Q_D$	—	34	51	ns	
	$t_{PHL}$			—	34	51		
$t_{PHL}$	Set-to-0	$Q_A \sim Q_D$	—	26	40	ns		

# HD74LS93

## TESTING METHOD

### 1) Test Circuit



### 2) Testing Table

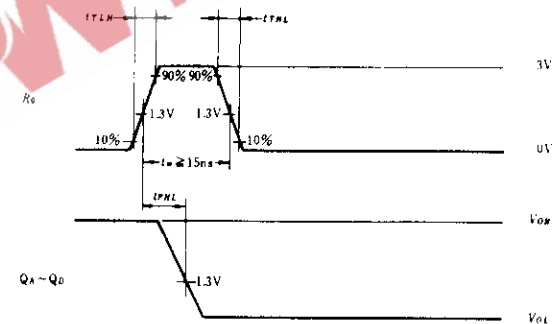
Item	From input to output	Inputs			Outputs			
		A	B	R <sub>0</sub>	Q <sub>A</sub>	Q <sub>B</sub>	Q <sub>C</sub>	Q <sub>D</sub>
$f_{max}$	A → Q	IN	to Q <sub>A</sub>	GND	Out	Out	Out	Out
	B → Q	4.5V	IN	GND	—	Out	Out	Out
$t_{PLH}$	A → Q <sub>A</sub>	IN	to Q <sub>A</sub>	GND	Out	—	—	—
	A → Q <sub>D</sub>	IN	to Q <sub>A</sub>	GND	—	—	—	Out
$t_{PHL}$	B → Q <sub>B</sub>	4.5V	IN	GND	—	Out	—	—
	B → Q <sub>C</sub>	4.5V	IN	GND	—	—	Out	—
	B → Q <sub>D</sub>	4.5V	IN	GND	—	—	—	Out
	R <sub>0</sub> <sup>*</sup> → Q	IN <sup>*</sup>	to Q <sub>A</sub>	IN	Out	Out	Out	Out

\* For initialized.

\*\* Measured with each input and unused inputs at 4.5V.

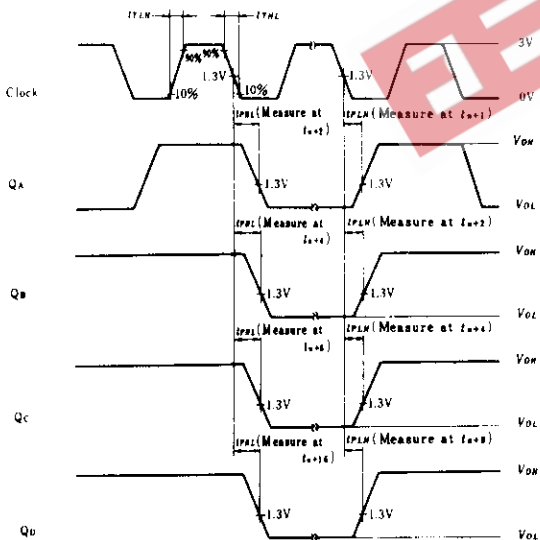
- Notes) 1.  $C_L$  includes probe and jig capacitance.  
2. All diodes are 1S2074 (H).

Waveform-2 ( $t_{PHL}(R_0 \rightarrow Q)$ )



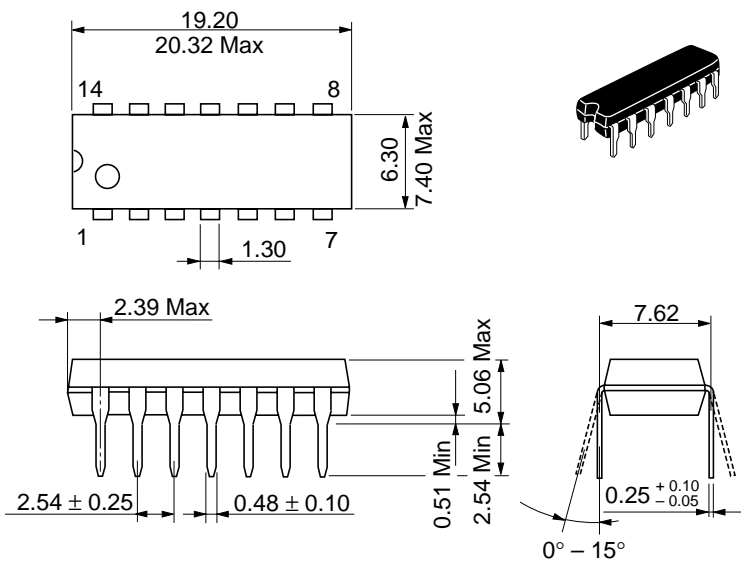
- Notes) 1.  $t_{TLH} \leq 15ns$ ,  $t_{THL} \leq 5ns$ .

Waveform-1 ( $f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Clock → Q))



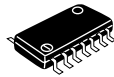
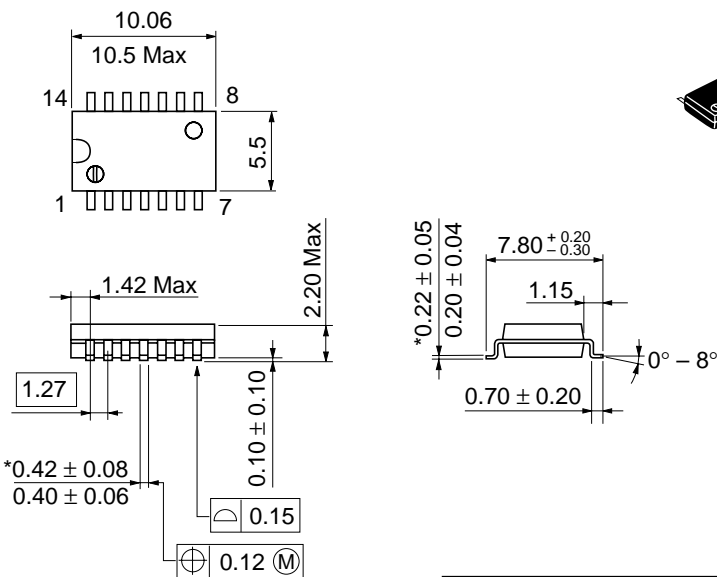
- Notes) 1. Input pulse;  $t_{TLH} \leq 15ns$ ,  $t_{THL} \leq 5ns$ ,  $PRR=1MHz$ , duty cycle=50% and: for  $f_{max}$ ,  $t_{TLH}=t_{THL} \leq 2.5ns$ .  
2.  $t_{PI}$  is reference bit time when all outputs are low.

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

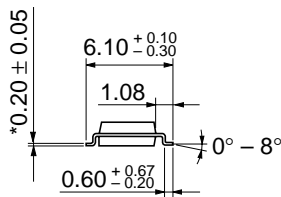
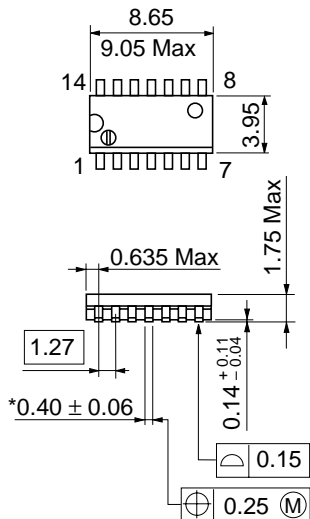


Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

\*Dimension including the plating thickness  
Base material dimension

EEPW 电子产品世界 .com.cn

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

\*Pd plating

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