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74AC/ACT11181

4-bit arithmetic logic unit

FEATURES

- Provides 16 arithmetic operations: add, subtract, compare, and double; plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full look-ahead Carry for high-speed arithmetic operation on long words
- Output capability: ±24 mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$ (sum mode)	C_L = 50pF	9.5	11.6	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	119	119	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.5	4.5	pF
C_{OUT}	Output capacitance	V_O = 0V or V_{CC} (A = B)	11	11	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
28-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11181N 74ACT11181N
28-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11181D 74ACT11181D

DESCRIPTION

The 74AC/ACT11181 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

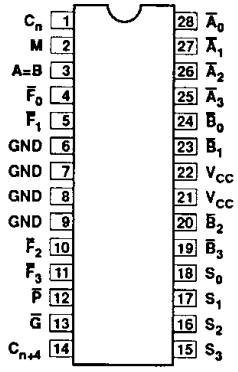
The 74AC/ACT11181 arithmetic logic units (ALU) are controlled by the four Function Select inputs (S_0 - S_3) and the Mode Control input (M) and can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Tables list these operations.

When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic opera-

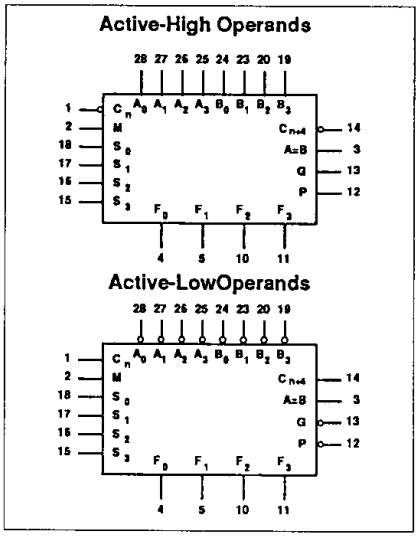
(continued)

PIN CONFIGURATION

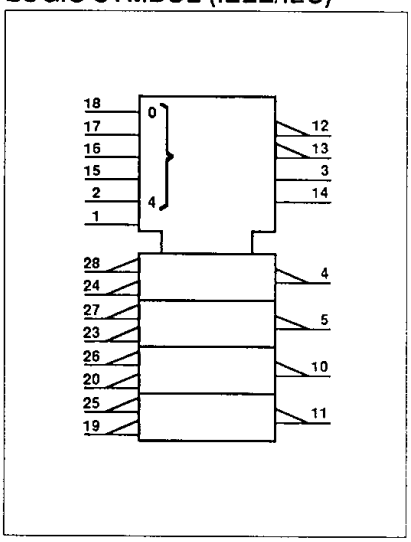
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



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tions on the individual bits as listed. When the Mode Control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry look-ahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the 74AC/ACT11882 carry look-ahead circuit. One carry look-ahead package is required for each group of eight 74AC/ACT11181 devices. Carry look-ahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes High when all four $\overline{F}$ outputs are High and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open-collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Tables list both the arithmetic operations that are performed without a carry in and with a carry in. Note that a carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active-High outputs. For either case, the tables list the operations that are performed to the operands labeled inside the logic symbol.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2	M	Mode control input
28, 27, 26, 25	$\overline{A}_0$ - $\overline{A}_3$	$\overline{A}$ operand inputs
24, 23, 20, 19	$\overline{B}_0$ - $\overline{B}_3$	$\overline{B}$ operand inputs
18, 17, 16, 15	S_0 - S_3	Function select inputs
1	C_n	Carry input
14	C_{n+4}	Carry output
3	A = B	Compare output
4, 5, 10, 11	$\overline{F}_0$ - $\overline{F}_3$	Outputs
13	$\overline{G}$	Carry generate output
12	$\overline{P}$	Carry propagate output
6, 7, 8, 9	GND	Ground (0V)
21, 22	V_{CC}	Positive supply voltage

The 74AC/ACT11181 devices will accomdate active-High or active-Low data if the pin designations are interpreted as follows:

PIN NUMBER	28	24	27	23	26	20	25	19	4	5	10	11	1	14	12	13
Active-Low data (Table 1)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_0$	$\overline{F}_0$	$\overline{F}_0$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$
Active-High data (Table 2)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_0	F_0	F_0	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y

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FUNCTION TABLE FOR ACTIVE-LOW DATA

SELECTION				ACTIVE LOW INPUTS & OUTPUTS		
				LOGIC (M = H)	ARITHMETIC** (M = L)	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	$\overline{A}$	A minus 1	A
L	L	L	H	$\overline{AB}$	AB minus 1	AB
L	L	H	L	$\overline{A}+B$	$A\overline{B}$ minus 1	$A\overline{B}$
L	L	H	H	Logical 1	minus 1	0 (zero)
L	H	L	L	$\overline{A+B}$	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1
L	H	L	H	$\overline{B}$	AB plus $(A+\overline{B})$	AB plus $(A+\overline{B})$ plus 1
L	H	H	L	$\overline{A\oplus B}$	A minus B minus 1	A minus B
L	H	H	H	$A+\overline{B}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
H	L	L	L	$\overline{AB}$	A plus (A + B)	A plus (A + B) plus 1
H	L	L	H	$A\oplus B$	A plus B	A plus B plus 1
H	L	H	L	B	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
H	L	H	H	A + B	(A + B)	(A + B) plus 1
H	H	L	L	Logical 0	A plus A*	A plus A plus 1
H	H	L	H	$A\overline{B}$	AB plus A	AB plus A plus 1
H	H	H	L	AB	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
H	H	H	H	A	A	A plus 1

L = Low voltage
H = High voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in two's complement notation.

FUNCTION TABLE FOR ACTIVE-HIGH DATA

SELECTION				ACTIVE HIGH INPUTS & OUTPUTS		
				LOGIC (M = H)	ARITHMETIC** (M = L)	
S3	S2	S1	S0		C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$\overline{A}$	A	A plus 1
L	L	L	H	$\overline{A+B}$	(A + B)	(A + B) plus 1
L	L	H	L	$\overline{AB}$	$A+\overline{B}$	$(A+\overline{B})$ plus 1
L	L	H	H	Logical 0	minus 1	0 (zero)
L	H	L	L	$\overline{AB}$	A plus $A\overline{B}$	A plus $A\overline{B}$ plus 1
L	H	L	H	$\overline{B}$	$A\overline{B}$ plus (A + B)	$A\overline{B}$ plus (A + B) plus 1
L	H	H	L	$A\oplus B$	A minus B minus 1	A minus B
L	H	H	H	$A\overline{B}$	$A\overline{B}$ minus 1	$A\overline{B}$
H	L	L	L	$\overline{A}+B$	AB plus A	AB plus A plus 1
H	L	L	H	$\overline{A\oplus B}$	A plus B	A plus B plus 1
H	L	H	L	B	AB plus $(A+\overline{B})$	AB plus $(A+\overline{B})$ plus 1
H	L	H	H	AB	AB minus 1	AB
H	H	L	L	Logical 1	A plus A*	A plus A plus 1
H	H	L	H	$A+\overline{B}$	A plus (A + B)	A plus (A + B) plus 1
H	H	H	L	A + B	A plus $(A+\overline{B})$	A plus $(A+\overline{B})$ plus 1
H	H	H	H	A	A minus 1	A

L = Low voltage
H = High voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in two's complement notation.

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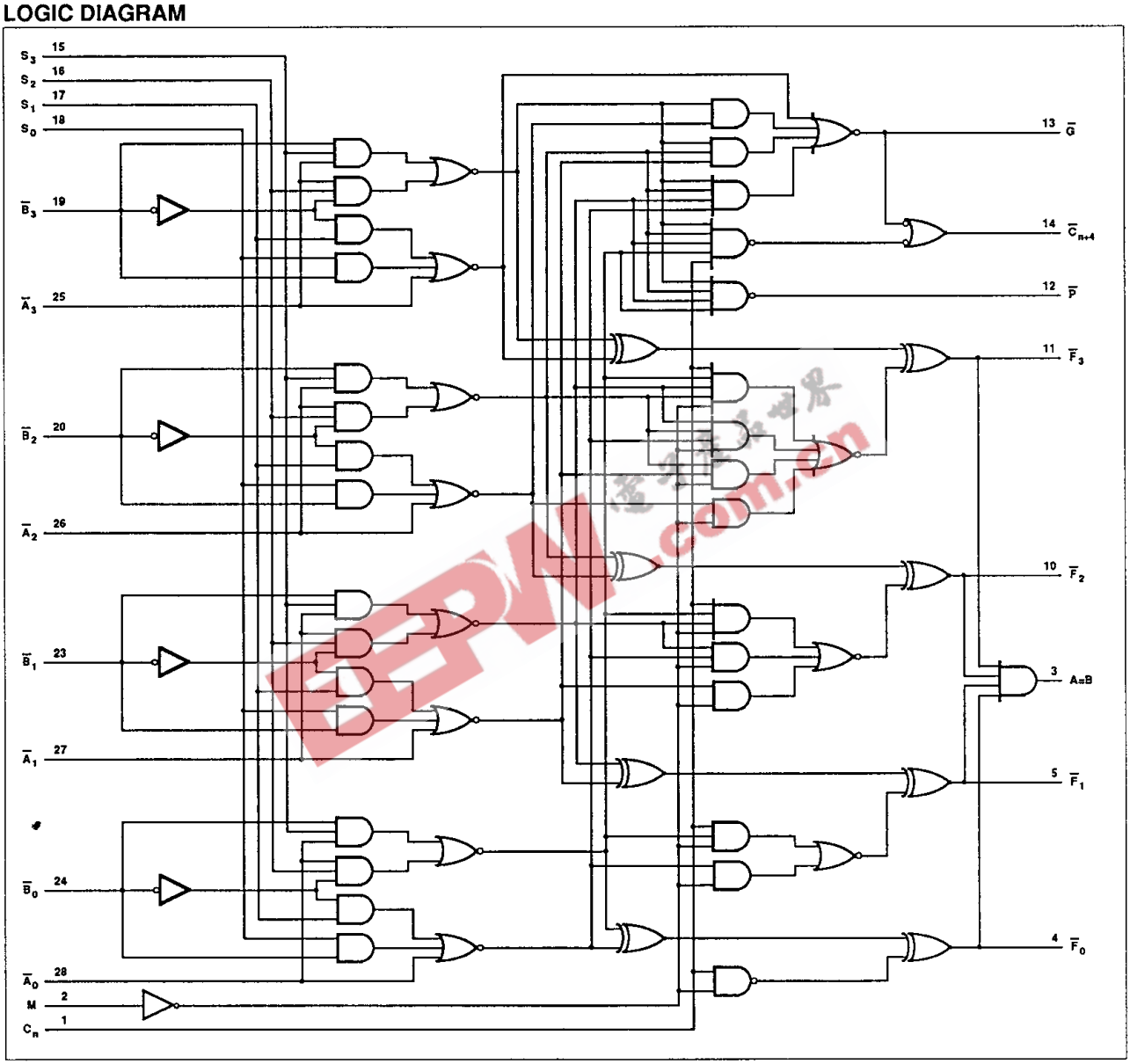
LOGIC DIAGRAM



4-bit arithmetic logic unit

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SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = V_{CC}$, $S_1 = S_2 = M = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	WAVEFORM
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$	1
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining C_n	$\overline{G}$	1
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}	2
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}	1

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = V_{CC}$, $S_0 = S_3 = M = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	WAVEFORM
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$	2
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$	2
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	1
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$	2
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	1
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	A = B	2
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	2
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}	1
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}	1

LOGIC MODE TEST TABLE III

FUNCTION INPUTS: $S_1 = S_2 = M = V_{CC}$, $S_0 = S_3 = GND$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	WAVEFORM
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	2
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	2

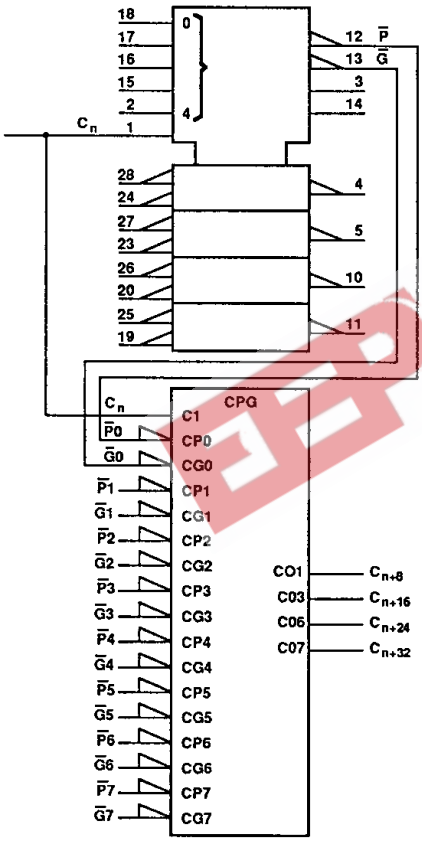


Figure 1

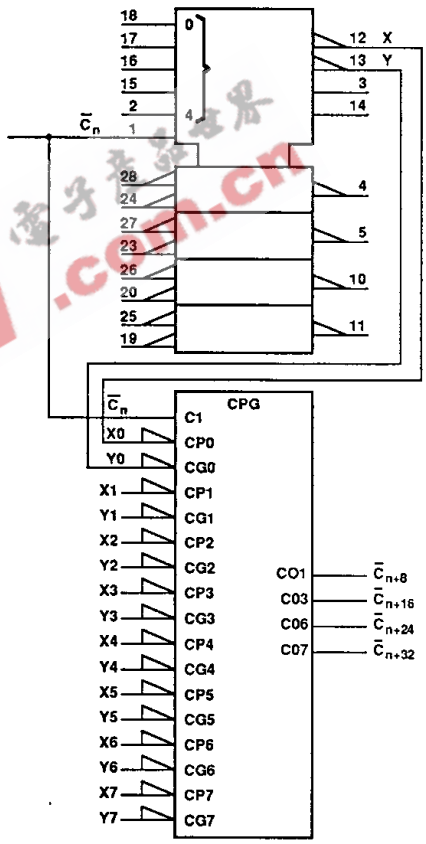


Figure 2

The signal designations in Figure 1 agree with the indicated internal functions based on active-Low data and are for use with the logic functions and arithmetic operations shown in the Function Table for Active-Low Data. The signal designators have been changed in Figure 2 to accommodate the logic functions and arithmetic operations given in the Function Table for Active-High Data.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11181			74ACT11181			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11181				74ACT11181				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
I_{OH}	High-level output current	A = B; V_O = V_{CC}		5.5		0.5		5.0		0.5		5.0	µA
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage (any output except A=B)	V_I = V_{IL} or V_{IH}	I_{OH} = -50µA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50µA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	µA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	µA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V—SUM MODE; M = S_1 = S_2 = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$		1.5 1.5	10.5 8.1	14.9 11.6	1.5 1.5	15.6 15.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	13.0 13.7	18.5 17.7	1.5 1.5	19.7 20.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	S_0 = S_3 = 4.5V	1.5 1.5	14.4 13.5	19.4 17.6	1.5 1.5	21.2 19.8	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M = 0V	1.5 1.5	13.2 10.7	21.0 16.5	1.5 1.5	22.4 17.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	S_0 = S_3 = 4.5V	1.5 1.5	14.2 10.9	19.6 14.5	1.5 1.5	21.3 18.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	S_0 = S_3 = 4.5V	1.5 1.5	13.8 11.8	19.2 14.7	1.5 1.5	20.8 17.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	S_0 = S_3 = 4.5V	1.5 1.5	12.6 9.8	15.9 12.3	1.5 1.5	17.6 13.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	12.4 10.2	15.7 13.2	1.5 1.5	17.2 14.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	14.4 11.8	18.4 14.6	1.5 1.5	19.7 16.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	S_0 = S_3 = 4.5V	1.5 1.5	13.7 12.7	17.7 15.4	1.5 1.5	19.4 17.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	S_0 = S_3 = 4.5V	1.5 1.5	16.2 13.9	21.7 18.4	1.5 1.5	23.7 20.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	S_0 = S_3 = 4.5V	1.5 1.5	16.0 14.4	21.5 19.1	1.5 1.5	23.6 21.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	S_0 = S_3 = 4.5V	1.5 1.5	10.3 9.2	13.2 11.2	1.5 1.5	14.5 12.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	S_0 = S_3 = 4.5V	1.5 1.5	16.6 12.2	20.7 14.8	1.5 1.5	21.6 17.1	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V—DIFF MODE; M = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	10.5 8.1	14.9 11.6	1.5 1.5	15.6 15.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.5 13.6	18.7 17.9	1.5 1.5	19.9 20.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	15.4 14.0	20.3 18.3	1.5 1.5	21.8 20.4	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	13.2 10.7	21.0 16.5	1.5 1.5	22.4 17.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.1 10.8	19.7 14.6	1.5 1.5	21.3 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.5 12.4	20.0 15.7	1.5 1.5	21.3 18.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.8 9.9	16.4 12.5	1.5 1.5	18.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.1 11.2	16.4 14.1	1.5 1.5	17.9 15.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.7 11.9	18.8 14.9	1.5 1.5	20.1 16.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	14.5 13.5	18.3 16.2	1.5 1.5	19.9 18.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.4 14.1	22.0 18.8	1.5 1.5	24.0 20.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.5 15.3	22.2 19.8	1.5 1.5	24.2 21.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	20.6 15.0	25.1 18.2	1.5 1.5	27.5 21.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	20.4 16.7	25.0 19.7	1.5 1.5	27.0 22.1	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V—LOGIC AND $\overline{ARITH}$ MODE

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	11.5 12.2	15.2 15.0	1.5 1.5	16.6 16.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	14.7 13.3	18.9 16.5	1.5 1.5	20.4 18.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	16.1 12.5	20.5 15.1	1.5 1.5	21.2 17.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	22.8 16.0	27.1 19.0	1.5 1.5	29.5 21.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	M = 4.5V (LOGIC mode)	1.5 1.5	14.9 17.0	20.3 24.0	1.5 1.5	21.4 26.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	15.7 12.6	21.6 17.8	1.5 1.5	23.6 21.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	M = 4.5V (LOGIC mode)	1.5 1.5	16.7 12.0	20.0 15.5	1.5 1.5	22.4 17.6	ns

NOTE: "$\overline{B}_n$ to $\overline{F}_n$" means any $\overline{B}$ to any $\overline{F}$ while "$\overline{B}_i$ to $\overline{F}_i$" means $\overline{B}_1$ to $\overline{F}_1$; $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—SUM MODE; M = S_1 = S_2 = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$		1.5 1.5	7.1 7.5	9.9 11.4	1.5 1.5	10.8 14.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	9.6 10.0	14.3 17.2	1.5 1.5	14.5 18.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	S_0 = S_3 = 4.5V	1.5 1.5	9.6 10.6	14.8 17.0	1.5 1.5	15.2 18.5	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M = 0V	1.5 1.5	9.2 8.3	14.0 13.1	1.5 1.5	14.9 14.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	S_0 = S_3 = 4.5V	1.5 1.5	9.2 8.3	13.2 14.3	1.5 1.5	14.6 16.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	S_0 = S_3 = 4.5V	1.5 1.5	9.1 8.8	13.0 13.6	1.5 1.5	14.4 16.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	S_0 = S_3 = 4.5V	1.5 1.5	8.4 7.7	13.3 10.7	1.5 1.5	14.1 11.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	7.9 8.3	13.0 10.7	1.5 1.5	13.8 11.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	S_0 = S_3 = 4.5V	1.5 1.5	9.5 9.4	14.3 14.6	1.5 1.5	15.5 15.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	S_0 = S_3 = 4.5V	1.5 1.5	9.2 10.0	14.0 15.3	1.5 1.5	15.2 16.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	S_0 = S_3 = 4.5V	1.5 1.5	10.8 10.3	14.1 15.3	1.5 1.5	15.4 16.7	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	S_0 = S_3 = 4.5V	1.5 1.5	10.4 10.7	14.1 15.6	1.5 1.5	15.3 17.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	S_0 = S_3 = 4.5V	1.5 1.5	7.3 8.3	9.2 11.2	1.5 1.5	9.9 12.1	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	S_0 = S_3 = 4.5V	1.5 1.5	14.3 11.7	17.7 14.8	1.5 1.5	18.5 17.1	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—DIFF MODE; M = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	7.1 7.5	9.9 11.4	1.5 1.5	10.8 14.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.5 10.5	14.6 17.3	1.5 1.5	14.8 19.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	10.5 11.3	15.4 17.4	1.5 1.5	16.0 19.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	9.2 8.3	14.0 13.1	1.5 1.5	14.9 14.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.1 8.4	13.4 14.6	1.5 1.5	14.7 16.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.6 9.5	13.8 14.2	1.5 1.5	15.0 17.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	8.7 8.0	13.4 10.2	1.5 1.5	14.2 11.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	8.6 8.8	13.3 11.3	1.5 1.5	14.1 12.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.7 9.7	14.5 14.5	1.5 1.5	15.7 15.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	9.4 10.8	14.4 16.0	1.5 1.5	15.5 17.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	11.0 10.5	14.3 15.5	1.5 1.5	15.6 16.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	10.9 11.2	14.3 15.3	1.5 1.5	15.7 17.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.5 12.8	20.2 16.4	1.5 1.5	22.7 21.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	16.3 13.6	20.0 18.4	1.5 1.5	22.1 21.2	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—LOGIC AND $\overline{\text{ARITH}}$ MODE

SYMBOL	PARAMETER	TEST CONDITIONS	74AC11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	7.6 9.8	11.7 15.0	1.5 1.5	12.7 16.1	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	9.8 10.5	14.5 15.6	1.5 1.5	15.5 17.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	M=0V ($\overline{\text{ARITH}}$ mode)	1.5 1.5	10.6 9.8	13.9 12.7	1.5 1.5	15.2 16.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M=0V ($\overline{\text{ARITH}}$ mode)	1.5 1.5	17.7 12.3	21.4 19.0	1.5 1.5	22.7 20.9	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	M = 4.5V (LOGIC mode)	1.5 1.5	9.9 11.6	14.3 21.0	1.5 1.5	15.4 23.3	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	M=0V ($\overline{\text{ARITH}}$ mode)	1.5 1.5	10.1 9.0	14.4 15.2	1.5 1.5	16.0 18.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	M = 4.5V (LOGIC mode)	1.5 1.5	10.8 9.0	14.8 11.5	1.5 1.5	16.4 14.3	ns

NOTE: "$\overline{B}_n$ to $\overline{F}_n$" means any $\overline{B}$ to any $\overline{F}$ while "$\overline{B}_1$ to $\overline{F}_1$" means $\overline{B}_1$ to $\overline{F}_1$; $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—SUM MODE; $M = S_1 = S_2 = 0V$

SYMBOL	PARAMETER	TEST CONDITIONS	74ACT11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	10.7 11.3	17.5 16.2	1.5 1.5	18.6 18.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 4.5V$	1.5 1.5	12.7 14.0	20.3 19.7	1.5 1.5	21.8 22.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 4.5V$	1.5 1.5	13.5 13.6	21.6 19.7	1.5 1.5	23.2 22.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	11.2 9.9	17.1 15.9	1.5 1.5	18.7 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 4.5V$	1.5 1.5	12.8 12.7	20.9 17.8	1.5 1.5	23.3 20.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 4.5V$	1.5 1.5	12.7 14.3	20.6 19.2	1.5 1.5	22.1 21.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.4 9.6	18.4 16.6	1.5 1.5	19.6 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.3 10.6	18.2 15.6	1.5 1.5	19.3 16.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.8 11.0	17.7 17.1	1.5 1.5	19.5 18.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 4.5V$	1.5 1.5	11.6 12.0	17.3 19.4	1.5 1.5	19.1 20.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	13.0 12.4	18.9 18.8	1.5 1.5	21.0 20.2	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	13.1 13.5	18.7 19.8	1.5 1.5	21.0 21.3	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F}_n$	$S_0 = S_3 = 4.5V$	1.5 1.5	9.5 10.6	15.0 16.4	1.5 1.5	16.3 17.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B	$S_0 = S_3 = 4.5V$	1.5 1.5	15.7 14.0	19.3 18.7	1.5 1.5	20.1 21.8	ns

NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

4-bit arithmetic logic unit | 74AC/ACT11181

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—DIFF MODE; M = 0V

SYMBOL	PARAMETER	TEST CONDITIONS	74ACT11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}		1.5 1.5	10.7 11.0	17.3 16.2	1.5 1.5	18.6 18.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.7 13.5	20.3 19.7	1.5 1.5	21.8 20.8	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to C_{n+4}	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.8 14.8	21.1 20.7	1.5 1.5	22.7 23.0	ns
t_{PLH} t_{PHL}	Propagation delay C_n to $\overline{F}_n$	M = 0V	1.5 1.5	11.2 9.9	17.1 15.9	1.5 1.5	18.7 17.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.8 12.7	20.8 18.4	1.5 1.5	22.2 20.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{G}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.2 13.4	20.8 18.7	1.5 1.5	21.6 21.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	11.5 9.6	18.5 14.6	1.5 1.5	19.6 15.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{P}$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	10.8 10.4	18.8 15.1	1.5 1.5	20.0 16.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	11.9 11.2	17.8 17.2	1.5 1.5	19.6 19.9	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	12.1 12.0	17.8 18.6	1.5 1.5	19.5 20.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.2 12.6	19.0 18.9	1.5 1.5	21.1 20.3	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to $\overline{F}_n$	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	13.6 13.1	19.4 18.7	1.5 1.5	21.5 20.4	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	18.0 16.0	21.6 21.5	1.5 1.5	23.7 24.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_n$ to A=B	$S_0 = S_3 = 0V$, $S_1 = S_2 = 4.5V$	1.5 1.5	18.5 16.5	22.7 22.0	1.5 1.5	23.9 25.4	ns

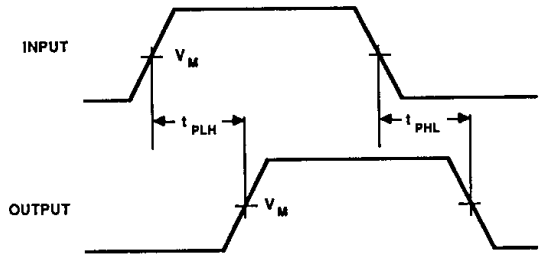
NOTE: "$\overline{A}_n$ to $\overline{F}_n$" means any $\overline{A}$ to any $\overline{F}$ while "$\overline{A}_i$ to $\overline{F}_i$" means $\overline{A}_1$ to $\overline{F}_1$; $\overline{A}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V—LOGIC AND $\overline{ARITH}$ MODE

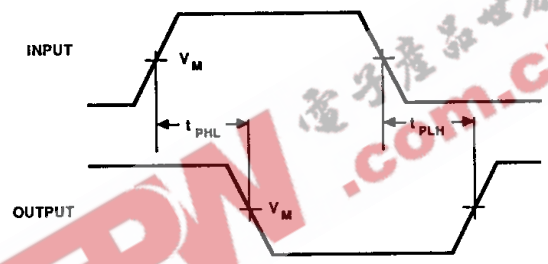
SYMBOL	PARAMETER	TEST CONDITIONS	74ACT11181					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay $\overline{A}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	10.0 11.0	15.9 17.4	1.5 1.5	18.3 19.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{B}_i$ to $\overline{F}_i$	M = 4.5V (LOGIC mode)	1.5 1.5	12.2 11.5	18.0 18.3	1.5 1.5	19.6 19.6	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{F}_n$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	12.1 10.6	18.3 15.8	1.5 1.5	20.1 17.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to A=B	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	18.7 17.2	22.1 22.2	1.5 1.5	23.4 25.4	ns
t_{PLH} t_{PHL}	Propagation delay S_n to C_{n+4}	M = 4.5V (LOGIC mode)	1.5 1.5	13.9 15.3	21.8 22.3	1.5 1.5	23.6 25.2	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{G}$	M=0V ($\overline{ARITH}$ mode)	1.5 1.5	12.7 13.5	20.5 19.7	1.5 1.5	22.3 22.0	ns
t_{PLH} t_{PHL}	Propagation delay S_n to $\overline{P}$	M = 4.5V (LOGIC mode)	1.5 1.5	12.4 11.7	18.6 17.7	1.5 1.5	20.5 18.0	ns

NOTE: "$\overline{B}_n$ to $\overline{F}_n$" means any $\overline{B}$ to any $\overline{F}$ while "$\overline{B}_i$ to $\overline{F}_i$" means $\overline{B}_1$ to $\overline{F}_1$; $\overline{B}_2$ to $\overline{F}_2$ (the subscripts must be the same).

AC WAVEFORMS



Waveform 1. Waveforms Showing Propagation Delays for Non-Inverting Paths

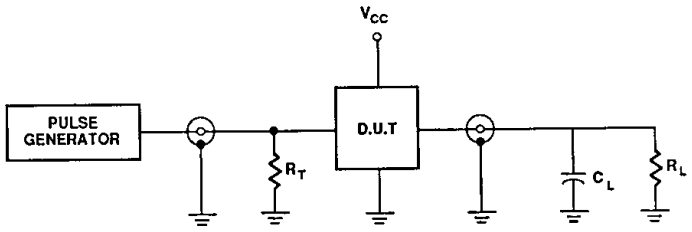


Waveform 2. Waveforms Showing Propagation Delays for Inverting Paths

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns

Ordering Information

ACL Products

TYPE NUMBER DESIGNATIONS