

# 74HC4852; 74HCT4852

Dual 4-channel analog multiplexer/demultiplexer with injection-current effect control

Rev. 03 — 2 September 2008

Product data sheet

## 1. General description

The 74HC4852; 74HCT4852 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7A.

The 74HC4852; 74HCT4852 are dual 4-channel analog multiplexers/demultiplexers with common select inputs (S0 and S1). Both multiplexers have a common active LOW enable input ( $\bar{E}$ ), four independent inputs/outputs (nY0 to nY3) and two common inputs/outputs (1Z, 2Z). The devices feature injection-current effect control, which has excellent value in automotive applications where voltages in excess of the supply voltage are common.

With  $\bar{E}$  LOW, two of the eight switches are selected (low impedance ON-state) by S0 and S1. With  $\bar{E}$  HIGH, all switches are in the high-impedance OFF-state, independent of S0 and S1.

The injection-current effect control allows signals at disabled analog input channels to exceed the supply voltage without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply-voltage range.

## 2. Features

- Injection-current cross coupling < 1 mV/mA
- Wide supply voltage range from 2.0 V to 6.0 V for 74HC4852
- ESD protection:
  - ◆ HBM JESD22-A114E exceeds 2000 V
  - ◆ CDM JESD22-C101C exceeds 1000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II level A
- Low ON-state resistance:
  - ◆ 400  $\Omega$  (typical) at  $V_{CC} = 2.0$  V
  - ◆ 215  $\Omega$  (typical) at  $V_{CC} = 3.0$  V
  - ◆ 120  $\Omega$  (typical) at  $V_{CC} = 3.3$  V
  - ◆ 76  $\Omega$  (typical) at  $V_{CC} = 4.5$  V
  - ◆ 59  $\Omega$  (typical) at  $V_{CC} = 6.0$  V

## 3. Applications

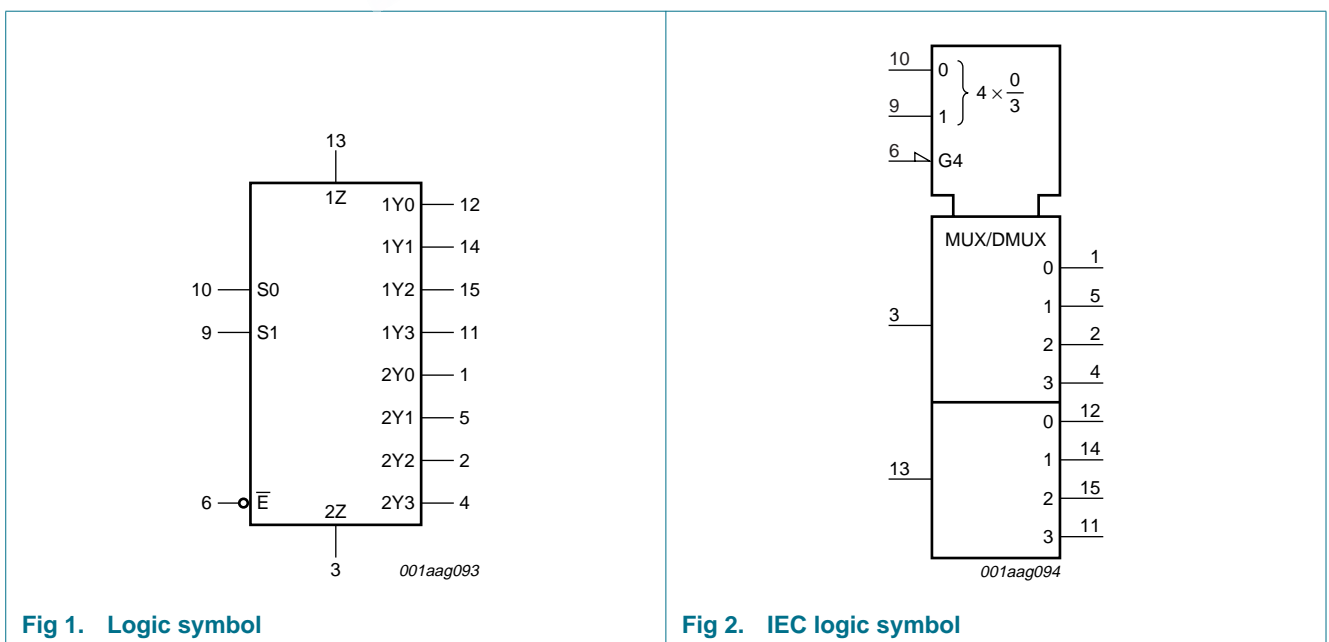
- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating
- Automotive application

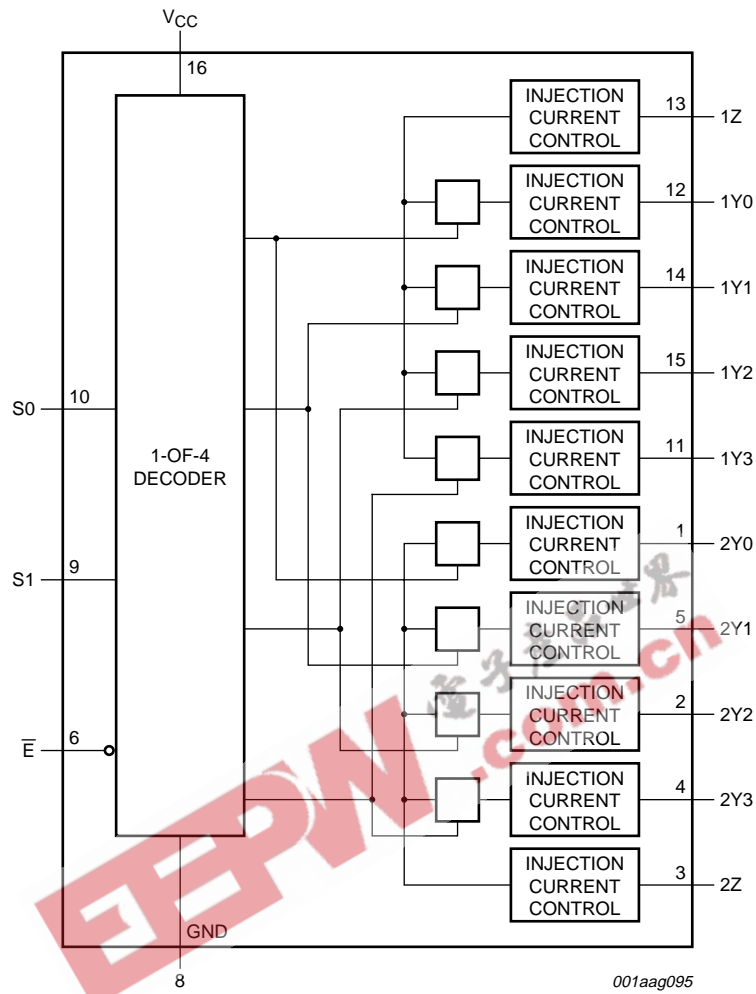
## 4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74HC4852D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4852PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4852BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74HCT4852D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4852PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4852BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

## 5. Functional diagram



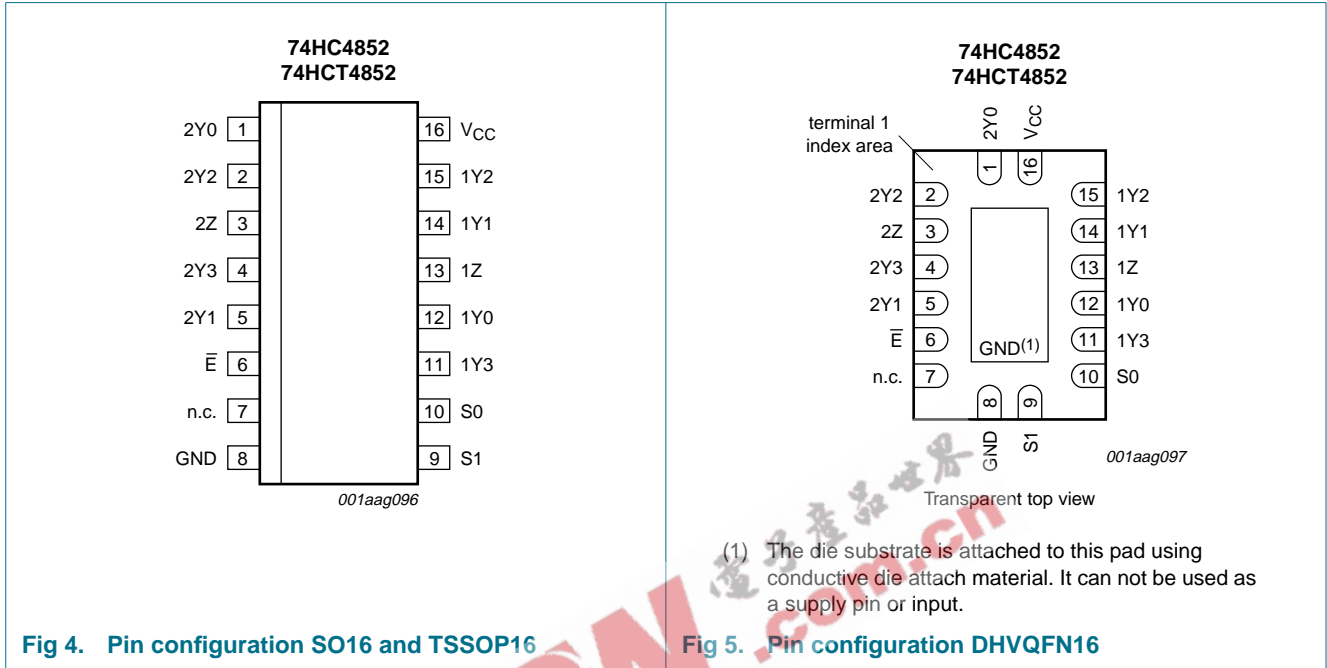


001aag095

Fig 3. Functional diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
2Y0	1	independent input/output
2Y2	2	independent input/output
2Z	3	common input/output
2Y3	4	independent input/output
2Y1	5	independent input/output
$\bar{E}$	6	enable input (active LOW)
n.c.	7	not connected
GND	8	ground (0 V)
S1	9	select input
S0	10	select input
1Y3	11	independent input/output
1Y0	12	independent input/output
1Z	13	common input/output
1Y1	14	independent input/output
1Y2	15	independent input/output
V <sub>CC</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table<sup>[1]</sup>

Input			Channel ON
$\bar{E}$	S1	S0	
L	L	L	nY0 to nZ
L	L	H	nY1 to nZ
L	H	L	nY2 to nZ
L	H	H	nY3 to nZ
H	X	X	-

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 X = don't care.

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7.0	V
$V_I$	input voltage		<sup>[1]</sup> -0.5	$V_{CC} + 0.5$	V
$V_{SW}$	switch voltage		<sup>[2]</sup> -0.5	$V_{CC} + 0.5$	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{SK}$	switch clamping current	$V_{SW} < -0.5\text{ V}$ or $V_{SW} > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{SW}$	switch current	$V_{SW} > -0.5\text{ V}$ or $V_{SW} < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$	<sup>[3]</sup> -	500	mW

- [1] The minimum and maximum input voltage rating may be exceeded if the input clamping current rating is observed.  
 [2] The minimum and maximum switch voltage rating may be exceeded if the switch clamping current rating is observed.  
 [3] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.  
 For TSSOP16 package:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.  
 For DHVQFN16 packages:  $P_{tot}$  derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4852			74HCT4852			Unit
			Min	Typ	Max	Min	Typ	Max	
V <sub>CC</sub>	supply voltage		2.0	-	6.0	4.5	5.0	5.5	V
V <sub>I</sub>	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
V <sub>SW</sub>	switch voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 2.0 V	-	6.0	1000	-	-	-	ns/V
		V <sub>CC</sub> = 3.0 V	-	6.0	800	-	-	-	ns/V
		V <sub>CC</sub> = 3.3 V	-	6.0	800	-	-	-	ns/V
		V <sub>CC</sub> = 4.5 V	-	6.0	500	-	6.0	500	ns/V
		V <sub>CC</sub> = 6.0 V	-	6.0	400	-	-	-	ns/V

10. Static characteristics

Table 6. R<sub>ON</sub> resistance

At recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see Figure 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4852</b>										
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = V <sub>CC</sub> to GND; $\bar{E}$ = V <sub>IL</sub>								
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 2 mA	-	400	650	-	670	-	700	Ω
		V <sub>CC</sub> = 3.0 V; I <sub>SW</sub> ≤ 2 mA	-	215	330	-	360	-	380	Ω
		V <sub>CC</sub> = 3.3 V; I <sub>SW</sub> ≤ 2 mA	-	120	270	-	305	-	345	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> ≤ 2 mA	-	76	210	-	240	-	270	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> ≤ 2 mA	-	59	195	-	220	-	250	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = 0.5 × V <sub>CC</sub> ; $\bar{E}$ = V <sub>IL</sub>								
		V <sub>CC</sub> = 2.0 V; I <sub>SW</sub> = 2 mA	-	4	10	-	15	-	20	Ω
		V <sub>CC</sub> = 3.0 V; I <sub>SW</sub> ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V <sub>CC</sub> = 3.3 V; I <sub>SW</sub> ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> ≤ 2 mA	-	2	8	-	12	-	16	Ω
		V <sub>CC</sub> = 6.0 V; I <sub>SW</sub> ≤ 2 mA	-	3	9	-	13	-	18	Ω
<b>74HCT4852</b>										
R <sub>ON(peak)</sub>	ON resistance (peak)	V <sub>I</sub> = V <sub>CC</sub> to GND; $\bar{E}$ = V <sub>IL</sub>								
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> ≤ 2 mA	-	76	210	-	240	-	270	Ω
ΔR <sub>ON</sub>	ON resistance mismatch between channels	V <sub>I</sub> = 0.5 × V <sub>CC</sub> ; $\bar{E}$ = V <sub>IL</sub>								
		V <sub>CC</sub> = 4.5 V; I <sub>SW</sub> ≤ 2 mA	-	2	8	-	12	-	16	Ω

**Table 7. Injection current coupling**

At recommended operating conditions; voltages are referenced to GND (ground 0 V); For test circuit see [Figure 9](#).

Symbol	Parameter	Conditions	74HC4852			74HCT4852			Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Typ <sup>[1]</sup>	Max		
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>										
$\Delta V_O$	output voltage variation	$I_{SW} \leq 1 \text{ mA}; R_S \leq 3.9 \text{ k}\Omega$ <sup>[2][3]</sup>	$V_{CC} = 3.3 \text{ V}$	-	0.05	1	-	-	-	mV
			$V_{CC} = 5.0 \text{ V}$	-	0.03	1	-	0.03	1	mV
		$I_{SW} \leq 10 \text{ mA}; R_S \leq 3.9 \text{ k}\Omega$	$V_{CC} = 3.3 \text{ V}$	-	0.55	5	-	-	-	mV
			$V_{CC} = 5.0 \text{ V}$	-	0.27	5	-	0.27	5	mV
		$I_{SW} \leq 1 \text{ mA}; R_S \leq 20 \text{ k}\Omega$	$V_{CC} = 3.3 \text{ V}$	-	0.04	2	-	-	-	mV
			$V_{CC} = 5.0 \text{ V}$	-	0.03	2	-	0.03	2	mV
		$I_{SW} \leq 10 \text{ mA}; R_S \leq 20 \text{ k}\Omega$	$V_{CC} = 3.3 \text{ V}$	-	0.56	20	-	-	-	mV
			$V_{CC} = 5.0 \text{ V}$	-	0.48	20	-	0.48	20	mV

[1] Typical values are measured at T<sub>amb</sub> = 25 °C.

[2]  $\Delta V_O$  here is the maximum variation of output voltage of an enabled analog channel when current is injected into any disabled channel.

[3]  $I_{SW}$  = total current injected into all disabled channels.

**Table 8. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC4852</b>										
$V_{IH}$	HIGH-level input voltage	control inputs								
		$V_{CC} = 2.0 \text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0 \text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 3.3 \text{ V}$	2.3	-	-	2.3	-	2.3	-	V
		$V_{CC} = 4.5 \text{ V}$	3.15	-	-	3.15	-	3.15	-	V
$V_{IL}$	LOW-level input voltage	control inputs								
		$V_{CC} = 2.0 \text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0 \text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 3.3 \text{ V}$	-	-	1.0	-	1.0	-	1.0	V
		$V_{CC} = 4.5 \text{ V}$	-	-	1.35	-	1.35	-	1.35	V
$I_I$	input leakage current	control inputs; $V_I = \text{GND or } V_{CC}$								
		$V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±0.1	-	±1.0	µA

**Table 8. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
I <sub>S(OFF)</sub>	OFF-state leakage current	$\bar{E} = V_{IH}; V_I = \text{GND or } V_{CC}; V_O = V_{CC} \text{ or GND}; V_{CC} = 6.0 \text{ V};$ see <a href="#">Figure 6</a>	nYn; per channel	-	-	±0.1	-	±0.5	-	±1.0	µA
			nZ; all channels	-	-	±0.2	-	±2.0	-	±4.0	µA
I <sub>S(ON)</sub>	ON-state leakage current	$\bar{E} = V_{IL}; V_I = \text{GND or } V_{CC}; V_O = V_{CC} \text{ or GND}; V_{CC} = 6.0 \text{ V};$ see <a href="#">Figure 7</a>	-	-	±0.1	-	±0.5	-	±1.0	µA	
I <sub>CC</sub>	supply current	$V_I = \text{GND or } V_{CC}$ $V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	5.0	-	20.0	µA	
C <sub>I</sub>	input capacitance	S0, S1, S2 and $\bar{E}$	-	2	10	-	10	-	10	pF	
C <sub>SW</sub>	switch capacitance	nZ; OFF-state	-	15	40	-	40	-	40	pF	
		nYn; OFF-state	-	3	15	-	15	-	15	pF	
<b>74HCT4852</b>											
V <sub>IH</sub>	HIGH-level input voltage	control inputs									
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	-	-	2.0	-	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	control inputs									
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	-	0.8	-	0.8	-	0.8	-	0.8
I <sub>I</sub>	input leakage current	control inputs; $V_I = \text{GND or } V_{CC}$ $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±0.1	-	±1.0	µA	
I <sub>S(OFF)</sub>	OFF-state leakage current	$\bar{E} = V_{IH}; V_I = \text{GND or } V_{CC}; V_O = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V};$ see <a href="#">Figure 6</a>	per channel	-	-	±0.1	-	±0.5	-	±1.0	µA
			all channels	-	-	±0.2	-	±2.0	-	±4.0	µA
				-	-	±0.1	-	±0.5	-	±1.0	µA
I <sub>S(ON)</sub>	ON-state leakage current	$\bar{E} = V_{IL}; V_I = \text{GND or } V_{CC}; V_O = V_{CC} \text{ or GND}; V_{CC} = 5.5 \text{ V};$ see <a href="#">Figure 7</a>	-	-	±0.1	-	±0.5	-	±1.0	µA	
I <sub>CC</sub>	supply current	$V_I = \text{GND or } V_{CC}$ $V_{CC} = 5.5 \text{ V}$	-	-	2.0	-	5.0	-	20.0	µA	
ΔI <sub>CC</sub>	additional supply current	control inputs; $V_I = V_{CC} - 2.1 \text{ V};$ other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}; I_O = 0 \text{ A}$	-	-	300	-	370	-	370	µA	
C <sub>I</sub>	input capacitance	S0, S1, S2 and $\bar{E}$	-	2	10	-	10	-	10	pF	
C <sub>SW</sub>	switch capacitance	nZ; OFF-state	-	9	40	-	40	-	40	pF	
		nYn; OFF-state	-	3	15	-	15	-	15	pF	



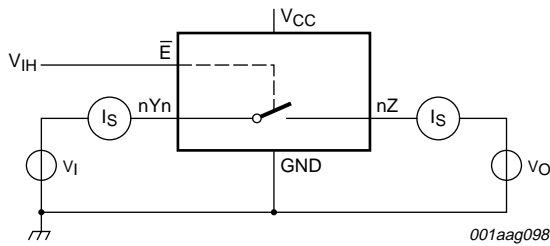
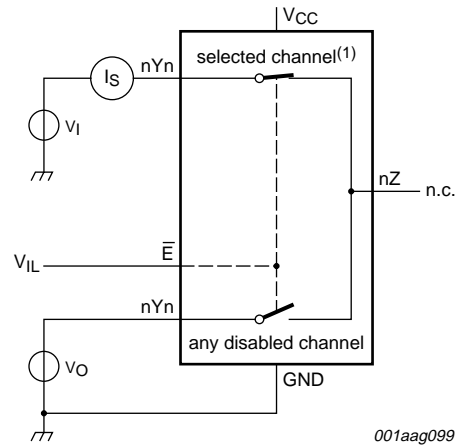
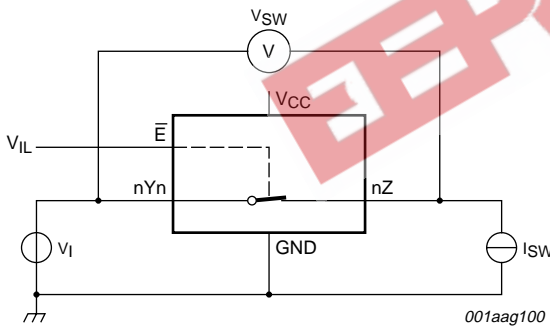


Fig 6. Test circuit for measuring OFF-state leakage current

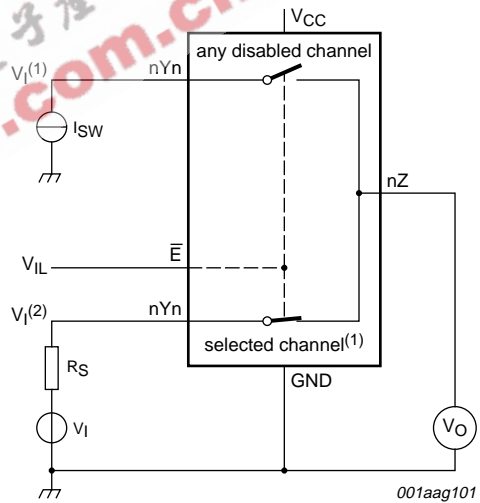


(1) Channel is selected by S0 and S1.  
Fig 7. Test circuit for measuring ON-state leakage current



$$R_{ON} = V_{SW} / I_{SW}$$

Fig 8. Test circuit for measuring ON resistance



(1) Channel is selected by S0 and S1.  
 $V_i^{(1)} < GND$  or  $V_i^{(1)} > V_{CC}$ .  
 $GND < V_i^{(2)} < V_{CC}$ .

Fig 9. Test circuit for injection current coupling

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for load circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ	Max	Min	Max	Min	Max		
<b>74HC4852</b>											
$t_{pd}$	propagation delay	nZ, nYn to nYn, nZ; see <a href="#">Figure 10</a> <sup>[1]</sup>									
		$V_{CC} = 2.0\text{ V}$	2.2	9.3	33	2.2	34	2.2	35	ns	
		$V_{CC} = 3.0\text{ V}$	2.2	4.9	16.5	1.9	18	1.9	19.5	ns	
		$V_{CC} = 3.3\text{ V}$	2.0	4.4	15.0	1.6	16.5	1.6	18.5	ns	
		$V_{CC} = 4.5\text{ V}$	1.6	3.2	11.6	1.1	12.5	1.1	13.5	ns	
		$V_{CC} = 6.0\text{ V}$	1.5	2.5	10.2	0.9	11	0.9	12	ns	
		Sn to nZ, nYn; see <a href="#">Figure 11</a> <sup>[1]</sup>									
		$V_{CC} = 2.0\text{ V}$	7.7	16.8	38	6.3	40	6.3	42	ns	
		$V_{CC} = 3.0\text{ V}$	4.9	8.8	20	3.9	21.5	3.9	23	ns	
		$V_{CC} = 3.3\text{ V}$	4.4	7.9	17.5	3.4	19	3.4	22	ns	
		$V_{CC} = 4.5\text{ V}$	3.2	5.8	14	2.3	15	2.3	17	ns	
		$V_{CC} = 6.0\text{ V}$	2.4	4.8	12.6	1.6	14.5	1.6	16.5	ns	
$t_{en}$	enable time	$\bar{E}$ to nZ, nYn; see <a href="#">Figure 12</a> <sup>[2]</sup>									
		$V_{CC} = 2.0\text{ V}$	10.5	20.5	47.5	8.5	52.5	8.5	57.5	ns	
		$V_{CC} = 3.0\text{ V}$	6.2	10.6	45	5.2	50	5.2	55	ns	
		$V_{CC} = 3.3\text{ V}$	5.6	9.4	42.5	4.6	47.5	4.6	52.5	ns	
		$V_{CC} = 4.5\text{ V}$	4.2	6.9	40	3	45	3	50	ns	
		$V_{CC} = 6.0\text{ V}$	3.2	5.6	39	2.2	40	2.2	40	ns	
$t_{dis}$	disable time	$\bar{E}$ to nZ, nYn; see <a href="#">Figure 12</a> <sup>[3]</sup>									
		$V_{CC} = 2.0\text{ V}$	39.5	75.4	100	39.3	105	39	115	ns	
		$V_{CC} = 3.0\text{ V}$	35.2	69.5	90	35.5	100	35	110	ns	
		$V_{CC} = 3.3\text{ V}$	34.6	68.1	85	34.6	95	34.5	105	ns	
		$V_{CC} = 4.5\text{ V}$	28.5	63	80	28.2	90	28	100	ns	
		$V_{CC} = 6.0\text{ V}$	14.4	57.9	78	13.5	80	13.0	80	ns	
$C_{PD}$	power dissipation capacitance	per channel; see <a href="#">Figure 13</a> <sup>[4]</sup>									
		$V_{CC} = 3.3\text{ V}$	-	42	-	-	-	-	-	pF	
		$V_{CC} = 5.0\text{ V}$	-	47	-	-	-	-	-	pF	

**Table 9. Dynamic characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground 0 V); for load circuit see [Figure 14](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HCT4852</b>										
t <sub>pd</sub>	propagation delay	nZ, nYn to nYn, nZ; see <a href="#">Figure 10</a> [1]								
		V <sub>CC</sub> = 4.5 V	1.6	3.5	11.5	1.1	12.5	1.1	13.5	ns
		Sn to nZ, nYn; see <a href="#">Figure 11</a> [1]								
		V <sub>CC</sub> = 4.5 V	3.2	7.6	13	2.3	15	1.6	17	ns
t <sub>en</sub>	enable time	$\bar{E}$ to nZ, nYn; see <a href="#">Figure 12</a> [2]								
		V <sub>CC</sub> = 4.5 V	4.2	8.3	25	3.0	30	3.0	35	ns
t <sub>dis</sub>	disable time	$\bar{E}$ to nZ, nYn; see <a href="#">Figure 12</a> [3]								
		V <sub>CC</sub> = 4.5 V	28.5	61.8	80	28.2	90	28.0	100	ns
C <sub>PD</sub>	power dissipation capacitance	per channel; see <a href="#">Figure 13</a> [4]								
		V <sub>CC</sub> = 5.0 V	-	47	-	-	-	-	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

[2] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.

[3] t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_{sw}) \times V_{CC}^2 \times f_o\}$$

f<sub>i</sub> = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

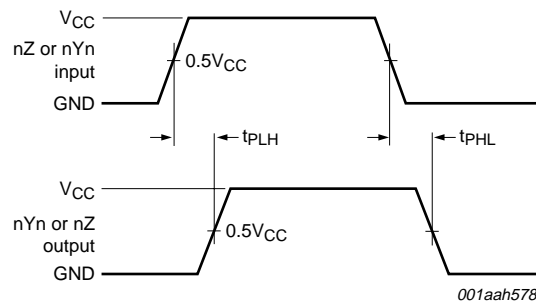
∑{(C<sub>L</sub> + C<sub>sw</sub>) × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>} = sum of outputs;

C<sub>L</sub> = output load capacitance in pF;

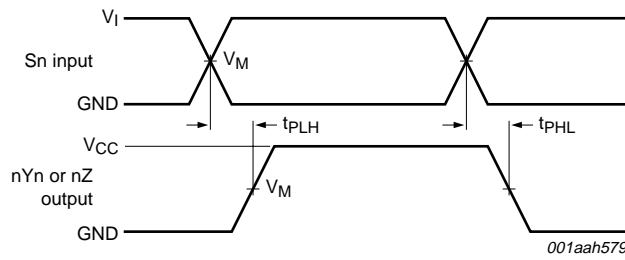
C<sub>sw</sub> = switch capacitance in pF;

V<sub>CC</sub> = supply voltage in V.

## 12. Waveforms

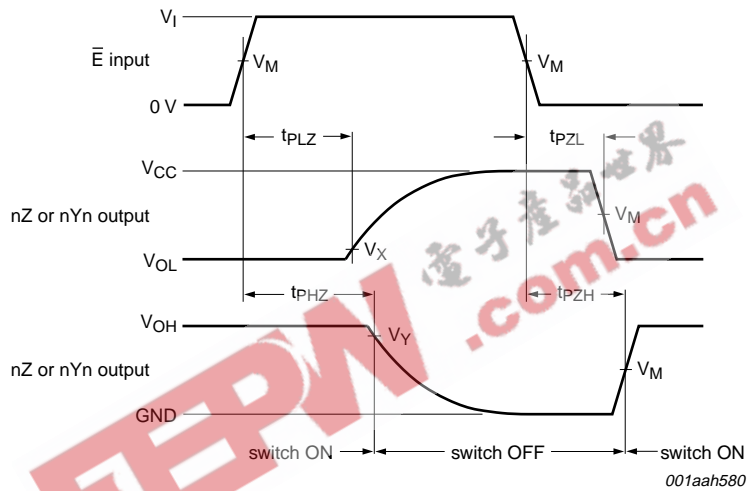


**Fig 10. Input (nZ, nYn) to output (nYn, nZ) propagation delays**



Measurement points are given in [Table 10](#).

**Fig 11. Input (Sn) to output (nYn, nZ) propagation delays**



Measurement points are shown in [Table 10](#).

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 12. Enable and disable times**

**Table 10. Measurement points**

Type	Input		Output		
	$V_M$	$V_I$	$V_M$	$V_X$	$V_Y$
74HC4852	$0.5V_{CC}$	$V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.1(V_{CC} - V_{OL})$	$0.9V_{OH}$
74HCT4852	1.3 V	3.0 V	$0.5V_{CC}$	$V_{OL} + 0.1(V_{CC} - V_{OL})$	$0.9V_{OH}$

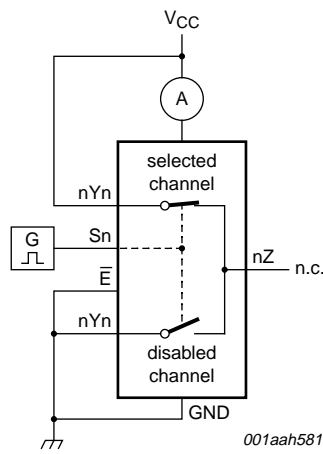
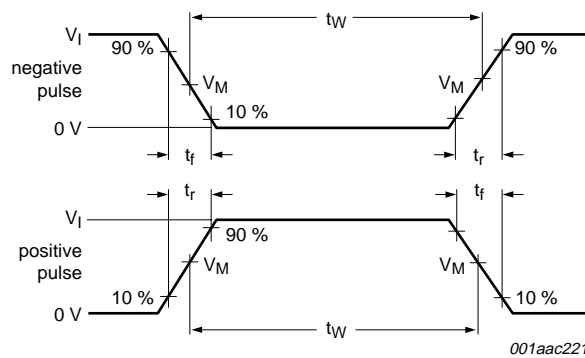
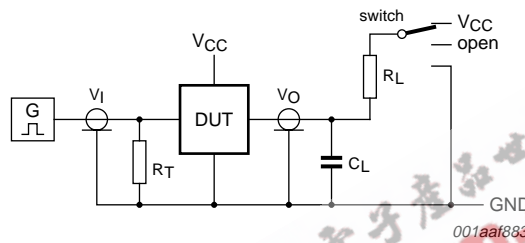


Fig 13. Test circuit for measuring power dissipation capacitance

EEPW 电子产品世界 .com.cn



a. Input pulse definition



Definitions for test circuit:

$R_L$  = load resistance.

$C_L$  = load capacitance including jig and probe capacitance.

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

b. Load circuit

Test data is given in [Table 11](#).

Fig 14. Input pulse definition and load circuit

Table 11. Test data

Test	Input			Output		S1 position
	Control $\bar{E}$ , Sn	Switch nYn (nZ)	$t_r, t_f$	Switch nZ (nYn)		
	$V_I$ <sup>[1]</sup>	$V_I$		$C_L$	$R_L$	
$t_{PHL}, t_{PLH}$	$V_{CC}$	$V_{CC}$	6 ns	50 pF	-	open
$t_{PHZ}, t_{PZH}$	$V_{CC}$	$V_{CC}$	6 ns	50 pF	10 k $\Omega$	GND
$t_{PLZ}, t_{PZL}$	$V_{CC}$	$V_{CC}$	6 ns	50 pF	10 k $\Omega$	$V_{CC}$
$C_{PD}$	$V_{CC}$	$V_{CC}$	6 ns	0 pF	-	open

[1] For 74HCT4852: input voltage  $V_I = 3.0$  V.

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

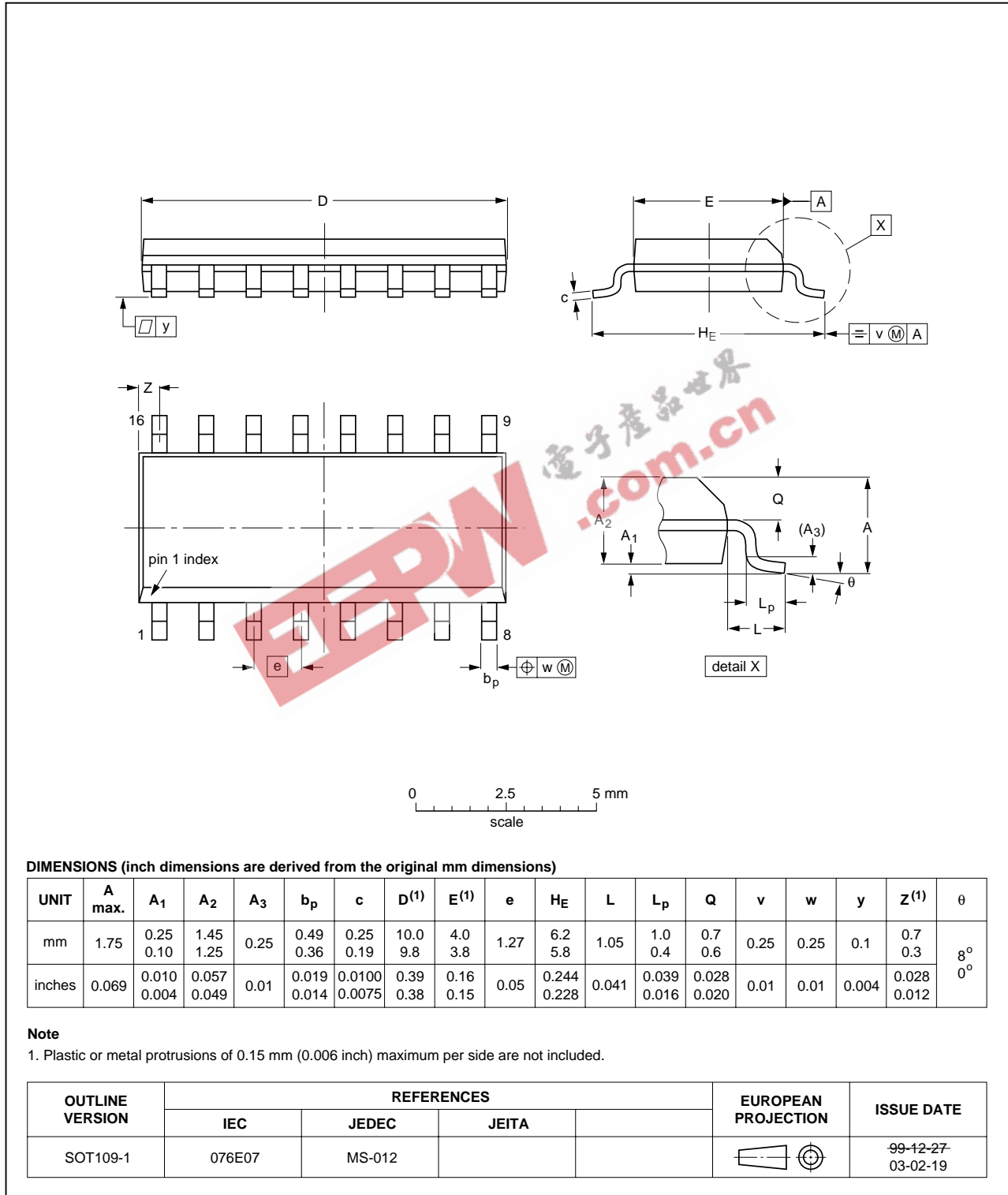


Fig 15. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

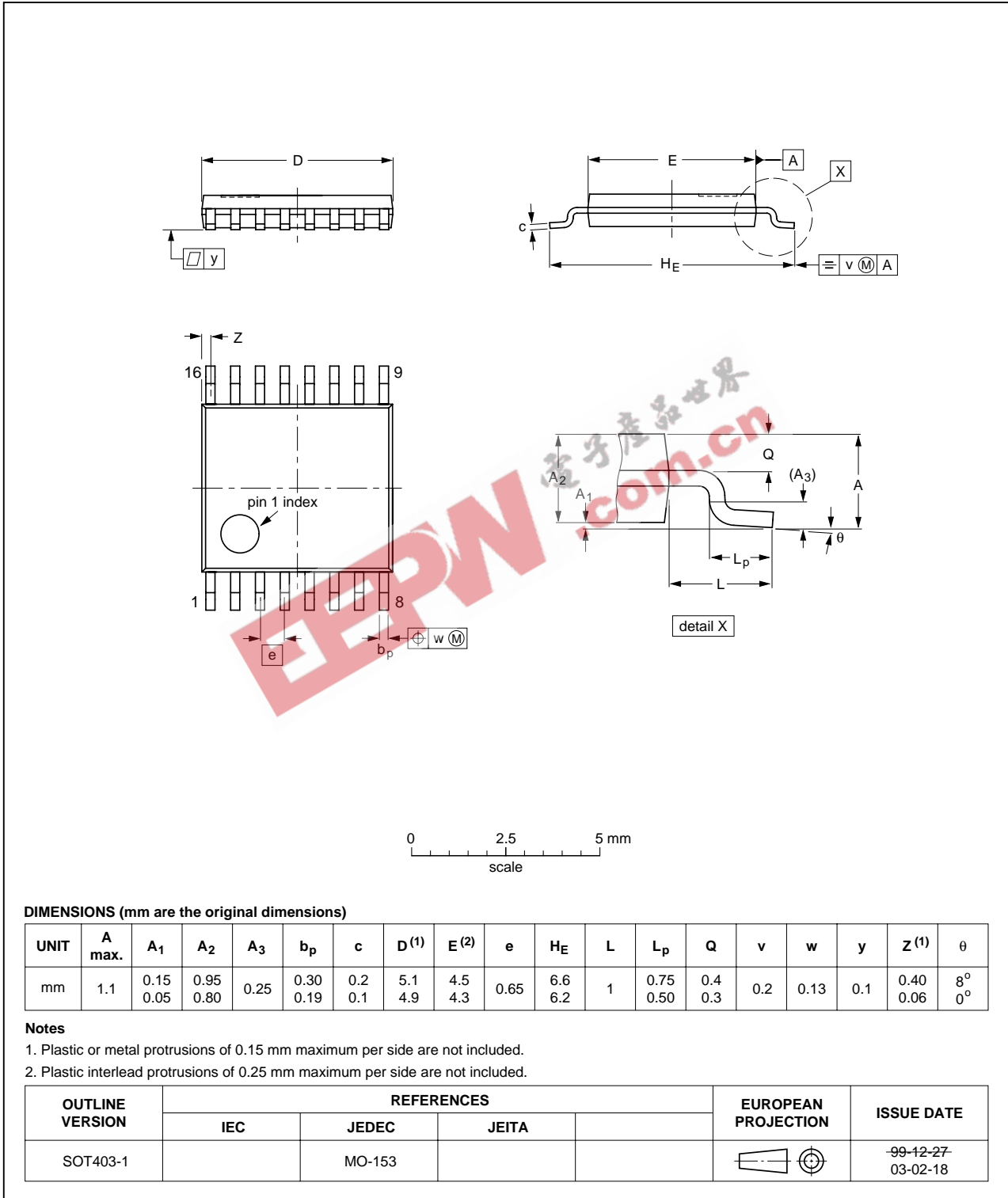


Fig 16. Package outline SOT403-1 (TSSOP16)



DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

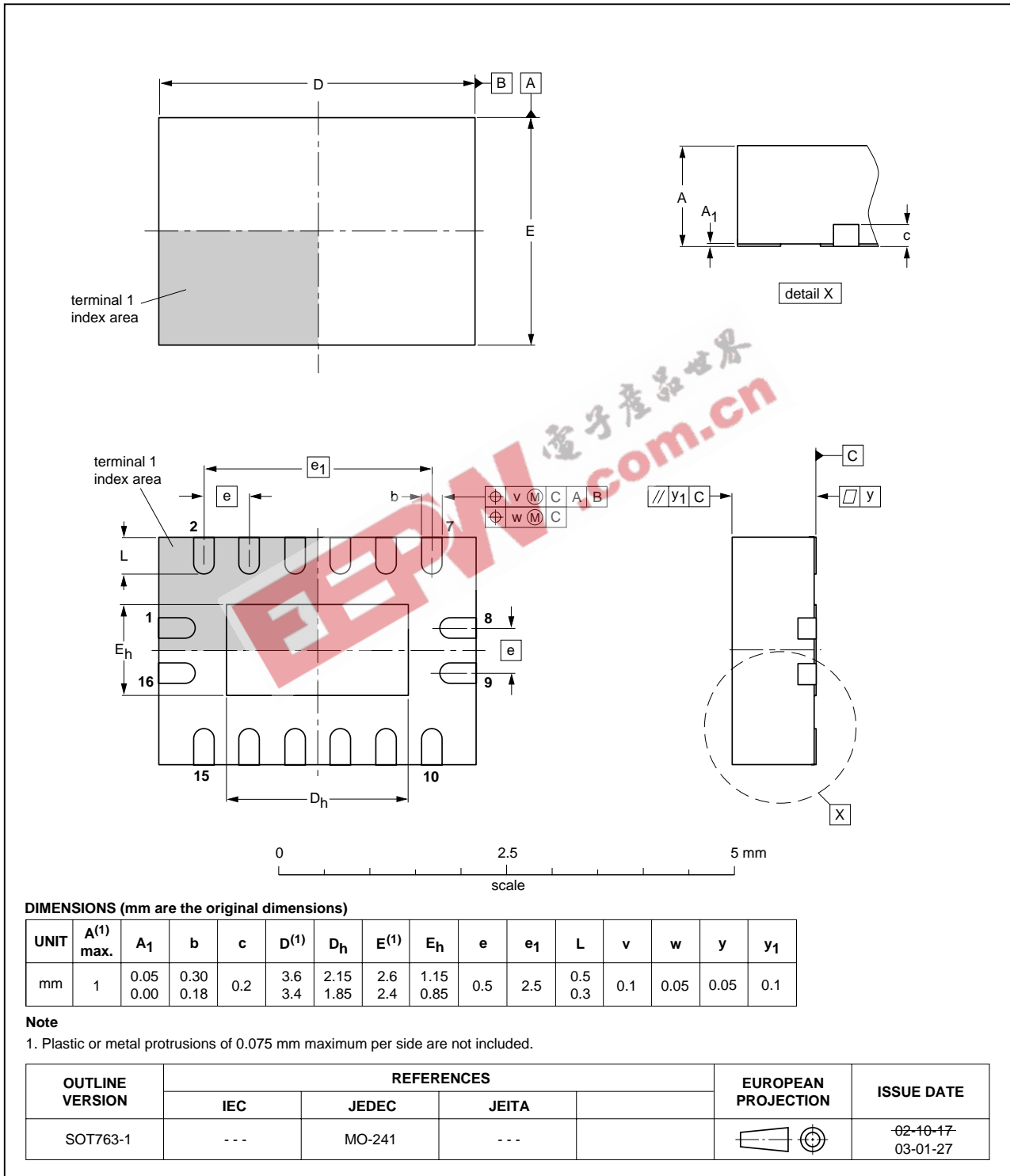


Fig 17. Package outline SOT763-1 (DHVQFN16)

## 14. Abbreviations

**Table 12. Abbreviations**

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 15. Revision history

**Table 13. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4852_3	20080902	Product data sheet	-	74HC4852_2
Modifications:	• 74HCT4852 device added.			
74HC4852_2	20070530	Product data sheet	-	74HC4852_1
74HC4852_1	20070323	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

### 16.3 Disclaimers

**General** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Terms and conditions of sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

### 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

18. Contents

1 General description ..... 1

2 Features ..... 1

3 Applications ..... 2

4 Ordering information ..... 2

5 Functional diagram ..... 2

6 Pinning information ..... 4

6.1 Pinning ..... 4

6.2 Pin description ..... 4

7 Functional description ..... 5

8 Limiting values ..... 5

9 Recommended operating conditions ..... 6

10 Static characteristics ..... 6

11 Dynamic characteristics ..... 10

12 Waveforms ..... 11

13 Package outline ..... 15

14 Abbreviations ..... 18

15 Revision history ..... 18

16 Legal information ..... 19

16.1 Data sheet status ..... 19

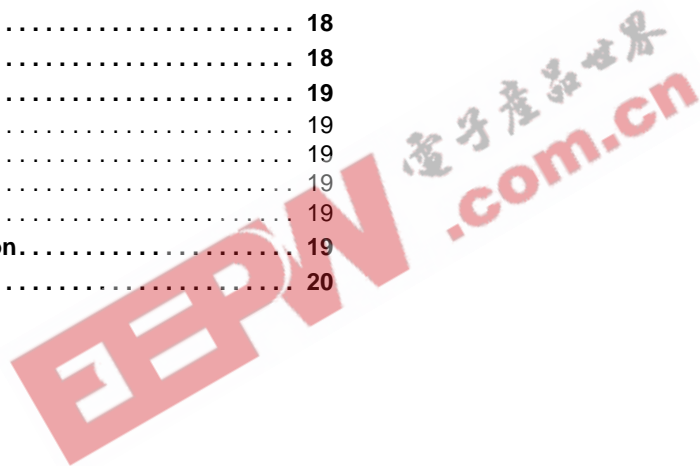
16.2 Definitions ..... 19

16.3 Disclaimers ..... 19

16.4 Trademarks ..... 19

17 Contact information ..... 19

18 Contents ..... 20



Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 2 September 2008

Document identifier: 74HC\_HCT4852\_3