

# 54/7495A 54LS/74LS95B

## 4-BIT RIGHT/LEFT SHIFT REGISTER

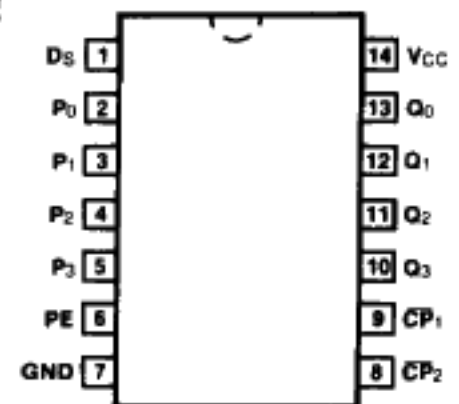
**DESCRIPTION** — The '95 is a 4-bit shift register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH-to-LOW transition of the appropriate clock input.

- SYNCHRONOUS, EXPANDABLE SHIFT RIGHT
- SYNCHRONOUS SHIFT LEFT CAPABILITY
- SYNCHRONOUS PARALLEL LOAD
- SEPARATE SHIFT AND LOAD CLOCK INPUTS

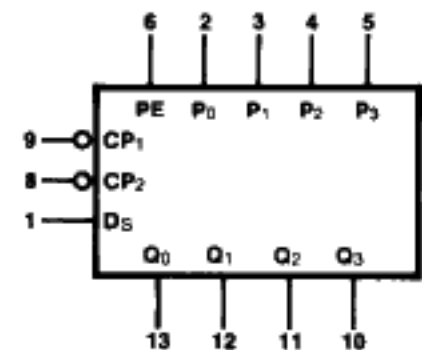
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V <sub>CC</sub> = +5.0 V ±5%, T <sub>A</sub> = 0°C to +70°C	V <sub>CC</sub> = +5.0 V ±10%, T <sub>A</sub> = -55°C to +125°C	
Plastic DIP (P)	A	7495APC, 74LS95BPC		9A
Ceramic DIP (D)	A	7495ADC, 74LS95BDC	5495ADM, 54LS95BDM	6A
Flatpak (F)	A	7495AFC, 74LS95BFC	5495AFM, 54LS95BFM	3I

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



V<sub>CC</sub> = Pin 14  
GND = Pin 7

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
CP <sub>1</sub>	Serial Clock Input (Active Falling Edge)	1.0/1.0	0.5/0.25
CP <sub>2</sub>	Parallel Clock Input (Active Falling Edge)	1.0/1.0	0.5/0.25
D <sub>S</sub>	Serial Data Input	1.0/1.0	0.5/0.25
P <sub>0</sub> — P <sub>3</sub>	Parallel Data Inputs	1.0/1.0	0.5/0.25
PE	Parallel Enable Input (Active HIGH)	2.0/2.0	1.0/0.5
Q <sub>0</sub> — Q <sub>3</sub>	Parallel Outputs	20/10	10/5.0 (2.5)

**FUNCTIONAL DESCRIPTION** — The '95 is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial ( $D_S$ ) and four Parallel ( $P_0 - P_3$ ) Data inputs and four Parallel Data outputs ( $Q_0 - Q_3$ ). The serial or parallel mode of operation is controlled by a Parallel Enable input (PE) and two Clock inputs,  $\overline{CP}_1$  and  $\overline{CP}_2$ . The serial (right-shift) or parallel data transfers occur synchronous with the HIGH-to-LOW transition of the selected clock input.

When PE is HIGH,  $\overline{CP}_2$  is enabled. A HIGH-to-LOW transition on enabled  $\overline{CP}_2$  transfers parallel data from the  $P_0 - P_3$  inputs to the  $Q_0 - Q_3$  outputs. When PE is LOW,  $\overline{CP}_1$  is enabled. A HIGH-to-LOW transition on enabled  $\overline{CP}_1$  transfers the data from Serial input ( $D_S$ ) to  $Q_0$  and shifts the data in  $Q_0$  to  $Q_1$ ,  $Q_1$  to  $Q_2$ , and  $Q_2$  to  $Q_3$  respectively (right-shift). A left-shift is accomplished by externally connecting  $Q_3$  to  $P_2$ ,  $Q_2$  to  $P_1$ , and  $Q_1$  to  $P_0$ , and operating the '95 in the parallel mode (PE = HIGH). For normal operation, PE should only change states when both Clock inputs are LOW. However, changing PE from LOW to HIGH while  $\overline{CP}_2$  is HIGH, or changing PE from HIGH to LOW while  $\overline{CP}_1$  is HIGH and  $\overline{CP}_2$  is LOW will not cause any changes on the register outputs.

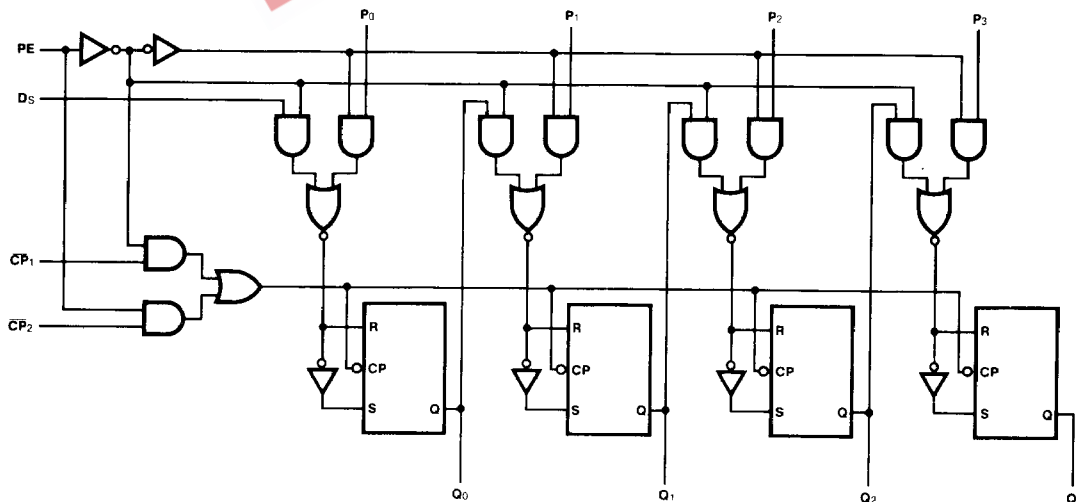
**MODE SELECT TABLE**

OPERATING MODE	INPUTS					OUTPUTS			
	PE	$\overline{CP}_1$	$\overline{CP}_2$	$D_S$	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Shift	L	L	X	l	X	L	$q_0$	$q_1$	$q_2$
	L	L	X	h	X	H	$q_0$	$q_1$	$q_2$
Parallel Load	H	X	L	X	$p_n$	$p_0$	$p_1$	$p_2$	$p_3$
Mode Change	L	L	L	X	X	No Change			
	L	L	L	X	X	No Change			
	L	H	L	X	X	No Change			
	L	H	L	X	X	Undetermined			
	L	L	H	X	X	Undetermined			
	L	L	H	X	X	No Change			
	L	H	H	X	X	Undetermined			
	L	H	H	X	X	No Change			

l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.  
 h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.  
 $p_n$  = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial

**LOGIC DIAGRAM**



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

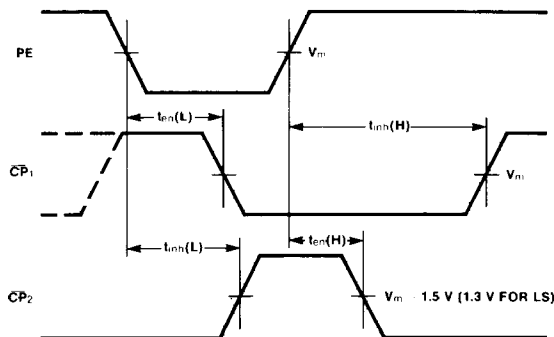
SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
$I_{CC}$	Power Supply Current	63		21		mA	$V_{CC} = \text{Max}$

**AC CHARACTERISTICS:**  $V_{CC} = +5.0 \text{ V}$ ,  $T_A = +25^\circ \text{C}$  (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITONS
		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$		$C_L = 15 \text{ pF}$ $R_L = 400 \Omega$			
		Min	Max	Min	Max		
$f_{max}$	Maximum Shift Frequency	25		30		MHz	Figs. 3-1, 3-9
$t_{PLH}$ $t_{PHL}$	Propagation Delay $\overline{CP}_1$ or $\overline{CP}_2$ to $Q_n$	27		27		ns	Figs. 3-1, 3-9
		32		27			

**AC OPERATING REQUIREMENTS:**  $V_{CC} = +5.0 \text{ V}$ ,  $T_A = +25^\circ \text{C}$ 

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS
		Min	Max	Min	Max		
$t_s$ (H) $t_s$ (L)	Setup Time HIGH or LOW $D_s$ or $P_n$ to $\overline{CP}_n$	15	15	20	20	ns	Fig. 3-7
$t_h$ (H) $t_h$ (L)	Hold Time HIGH or LOW $D_s$ or $P_n$ to $\overline{CP}_n$	0	0	10	10	ns	Fig. 3-7
$t_w$ (H)	$\overline{CP}_n$ Pulse Width HIGH	20		20		ns	Fig. 3-9
$t_{en}$ (L)	Enable Time LOW PE to $\overline{CP}_1$	15		25		ns	Fig. a
$t_{inh}$ (H)	Inhibit Time HIGH PE to $\overline{CP}_1$	5.0		20		ns	Fig. a
$t_{en}$ (H)	Enable Time HIGH PE to $\overline{CP}_2$	15		25		ns	Fig. a
$t_{inh}$ (L)	Inhibit Time LOW PE to $\overline{CP}_2$	5.0		20		ns	Fig. a


**Fig. a**