

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT4514

4-to-16 line decoder/demultiplexer
with input latches

Product specification
File under Integrated Circuits, IC06

September 1993

4-to-16 line decoder/demultiplexer with input latches

74HC/HCT4514

FEATURES

- Non-inverting outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4514 are high-speed Si-gate CMOS devices and are pin compatible with "4514" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4514 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A₀ to A₃), with latches, a latch enable input (LE), and an active LOW enable input (\bar{E}). The 16 outputs (Q₀ to Q₁₅) are mutually exclusive active HIGH. When LE is HIGH, the selected output is determined by the data on A_n. When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When \bar{E} is LOW, the selected output, determined by the contents of the latch, is HIGH. At \bar{E} HIGH, all outputs are LOW. The enable input (\bar{E}) does not affect the state of the latch.

When the "4514" is used as a demultiplexer, \bar{E} is the data input and A₀ to A₃ are the address inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|--|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay A _n to Q _n | C _L = 15 pF; V _{CC} = 5 V | 23 | 26 | ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per package | notes 1 and 2 | 44 | 45 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

ORDERING INFORMATION

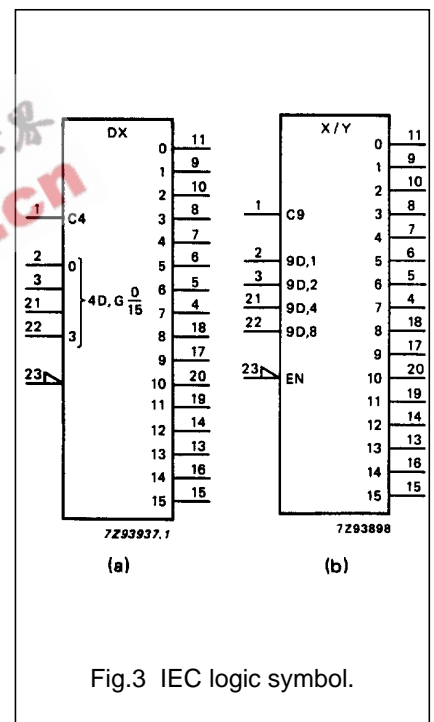
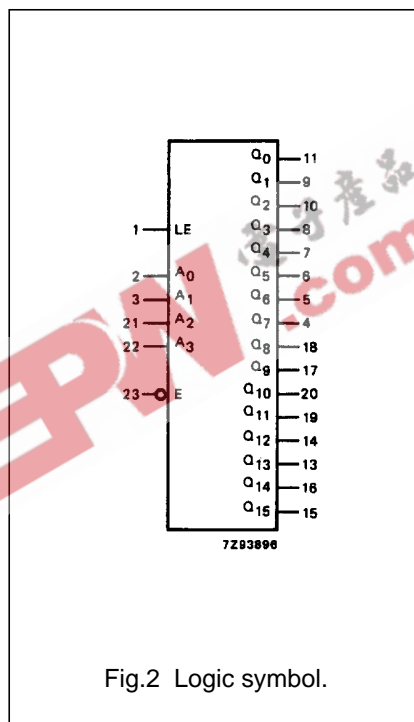
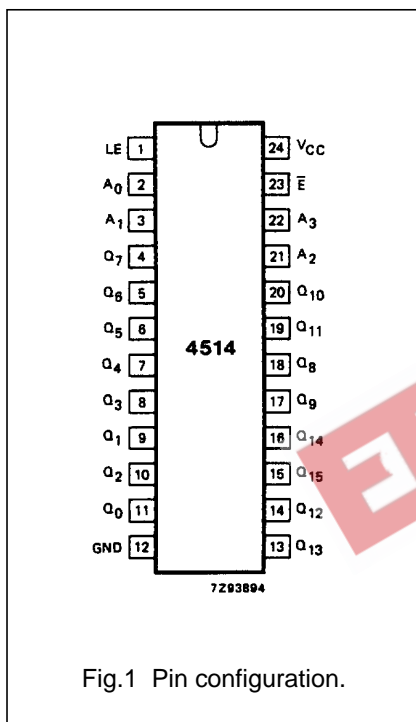
See "74HC/HCT/HCU/HCMOS Logic Package Information".

4-to-16 line decoder/demultiplexer with input latches

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--|-----------------------------------|-----------------------------------|
| 1 | LE | latch enable input (active HIGH) |
| 2, 3, 21, 22 | A ₀ to A ₃ | address inputs |
| 11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15 | Q ₀ to Q ₁₅ | multiplexer outputs (active HIGH) |
| 12 | GND | ground (0 V) |
| 23 | \bar{E} | enable input (active LOW) |
| 24 | V _{CC} | positive supply voltage |



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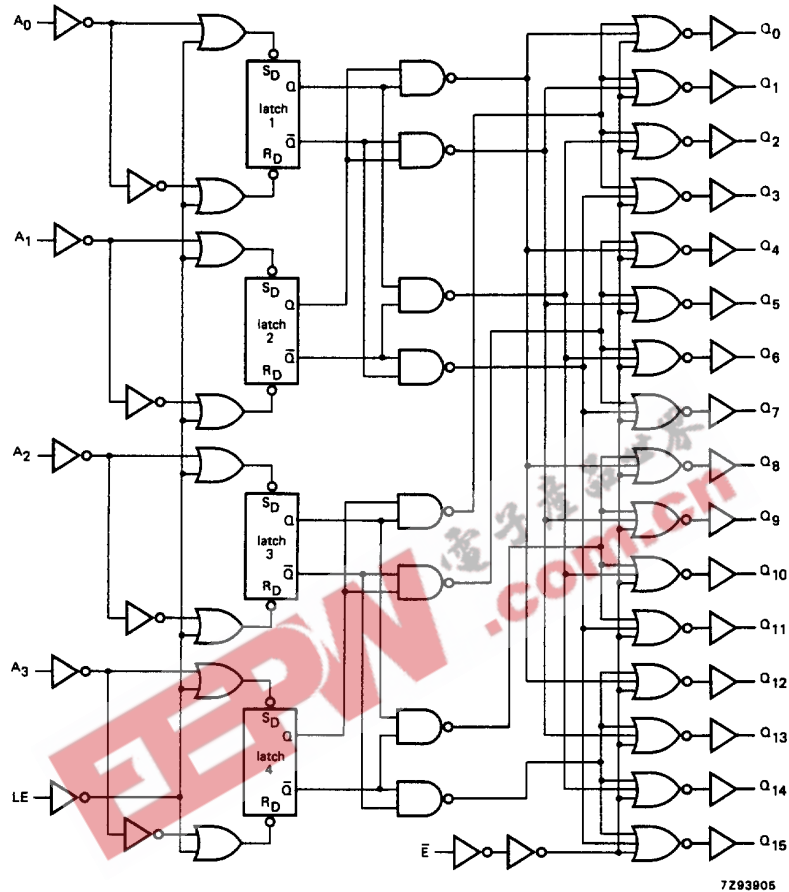


Fig.5 Logic diagram.

4-to-16 line decoder/demultiplexer with
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DC CHARACTERISTICS FOR 74HCFor the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|---|-----------------------|-----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay A _n to Q _n | | 74 27 22 | 230 46 39 | | 290 58 49 | 345 69 59 | ns | 2.0 4.5 6.0 | Fig.6 | |
| t _{PHL} / t _{PLH} | propagation delay LE to Q _n | | 74 27 22 | 230 46 39 | | 290 58 49 | 345 69 59 | ns | 2.0 4.5 6.0 | Fig.6 | |
| t _{PHL} / t _{PLH} | propagation delay \bar{E} to Q _n | | 41 15 12 | 175 35 30 | | 220 44 37 | 265 53 45 | ns | 2.0 4.5 6.0 | Fig.6 | |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.6 | |
| t _W | latch enable pulse width HIGH | 80 16 14 | 14 5 4 | | 100 20 17 | | 120 24 20 | ns | 2.0 4.5 6.0 | Fig.7 | |
| t _{SU} | set-up time A _n to LE | 90 18 15 | 25 9 7 | | 115 23 20 | | 135 27 23 | ns | 2.0 4.5 6.0 | Fig.7 | |
| t _H | hold time A _n to LE | 1 1 1 | -11 -4 -3 | | 1 1 1 | | 1 1 1 | ns | 2.0 4.5 6.0 | Fig.7 | |

4-to-16 line decoder/demultiplexer with input latches

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|----------------|-----------------------|
| A _n | 0.65 |
| LE | 1.40 |
| \bar{E} | 1.00 |

AC CHARACTERISTICS FOR 74HCT

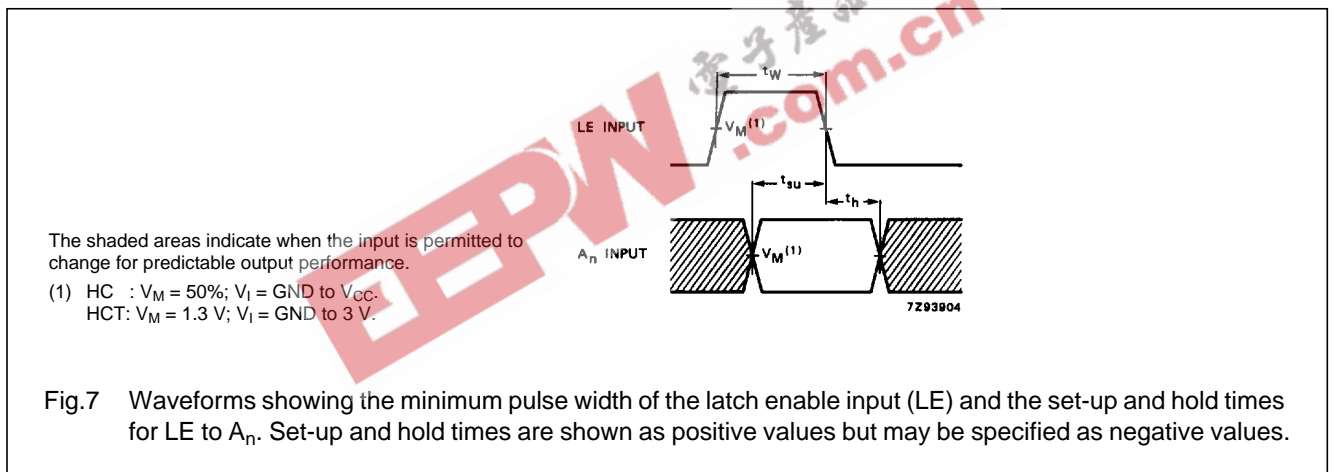
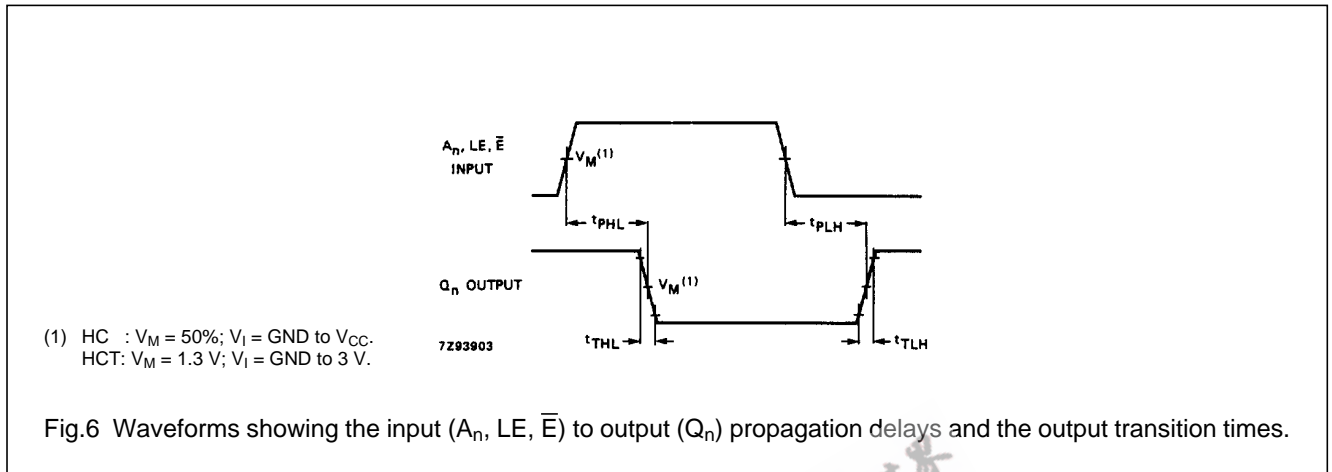
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|----|------|------------------------|-----------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay A _n to Q _n | | 30 | 55 | | 69 | | 83 | ns | 4.5 | Fig.6 | |
| t _{PHL} / t _{PLH} | propagation delay LE to Q _n | | 29 | 50 | | 63 | | 75 | ns | 4.5 | Fig.6 | |
| t _{PHL} / t _{PLH} | propagation delay \bar{E} to Q _n | | 17 | 40 | | 50 | | 60 | ns | 4.5 | Fig.6 | |
| t _{THL} / t _{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.6 | |
| t _w | latch enable pulse width HIGH | 16 | 4 | | 20 | | 24 | | ns | 4.5 | Fig.7 | |
| t _{su} | set-up time A _n to LE | 18 | 9 | | 23 | | 27 | | ns | 4.5 | Fig.7 | |
| t _h | hold time A _n to LE | 3 | -3 | | 3 | | 3 | | ns | 4.5 | Fig.7 | |

4-to-16 line decoder/demultiplexer with input latches

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AC WAVEFORMS



4-to-16 line decoder/demultiplexer with input latches

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APPLICATION INFORMATION

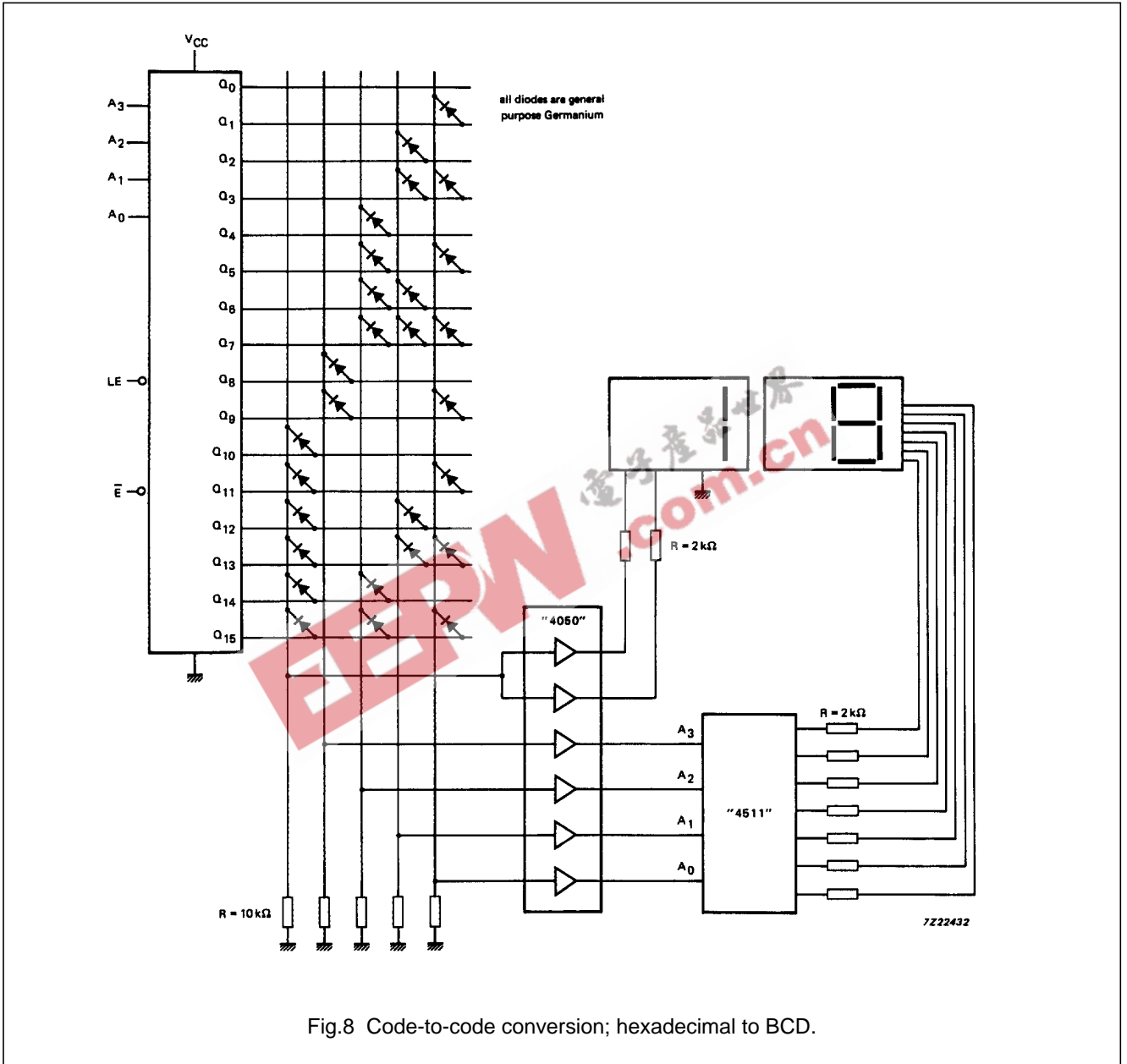


Fig.8 Code-to-code conversion; hexadecimal to BCD.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".