



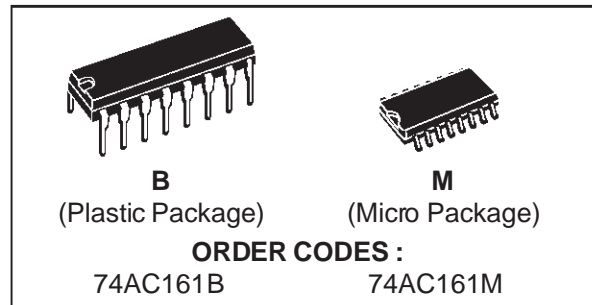
SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

- HIGH SPEED:
 $f_{MAX} = 125 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 8 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2\text{V to } 6\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 161
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The AC161 is a high-speed CMOS SYNCHRONOUS PRESETTABLE COUNTER fabricated with sub-micron silicon gate and double-layer metal wiring CMOS technology. It is ideal for low power applications maintaining high speed operation similar to equivalent Bipolar Schottky TTL. It is a 4 bit binary counter with Asynchronous Clear.

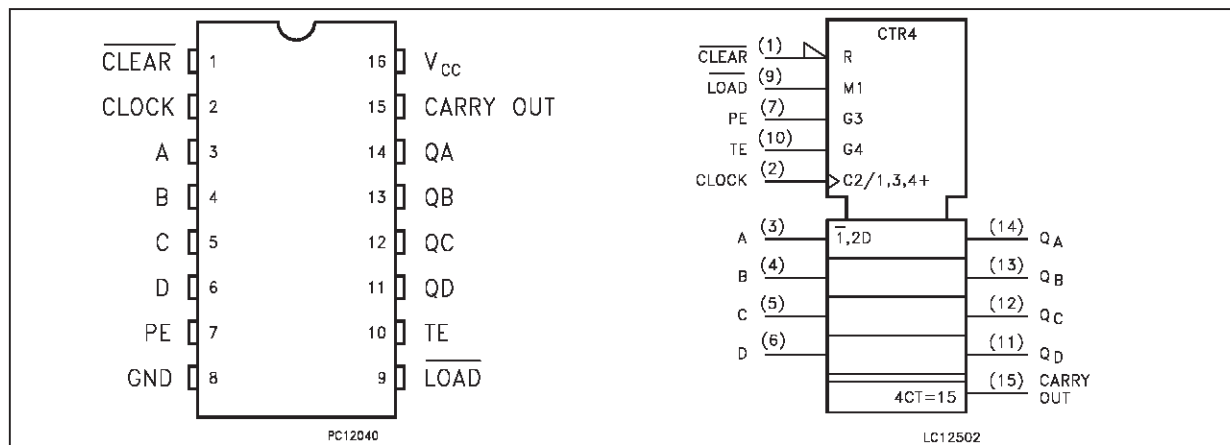
The circuit have four fundamental modes of operation, in order of preference: synchronous



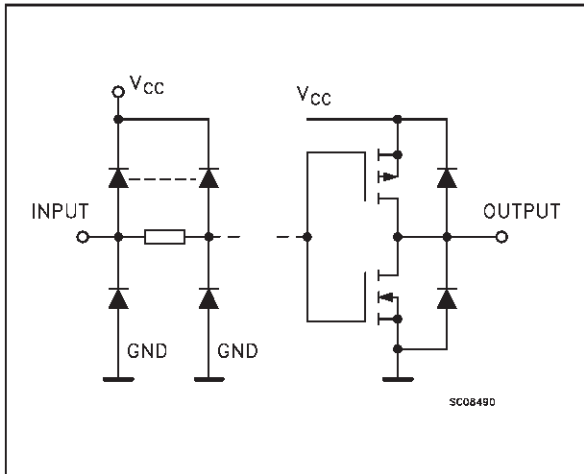
reset, parallel load, count-up and hold. Four control inputs, Master Reset (CLEAR), Parallel Enable Input (LOAD), Count Enable Input (PE) and Count Enable Carry Input (TE), determine the mode of operation as shown in the Truth Table. A LOW signal on CLEAR overrides counting and parallel loading and sets all outputs on LOW state. A LOW signal on LOAD overrides counting and allows information on Parallel Data Qn inputs to be loaded into the flip-flops on the next rising edge of CLOCK. With LOAD and CLEAR, PE and TE permit counting when both are HIGH. Conversely, a LOW signal on either PE and TE inhibits counting.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

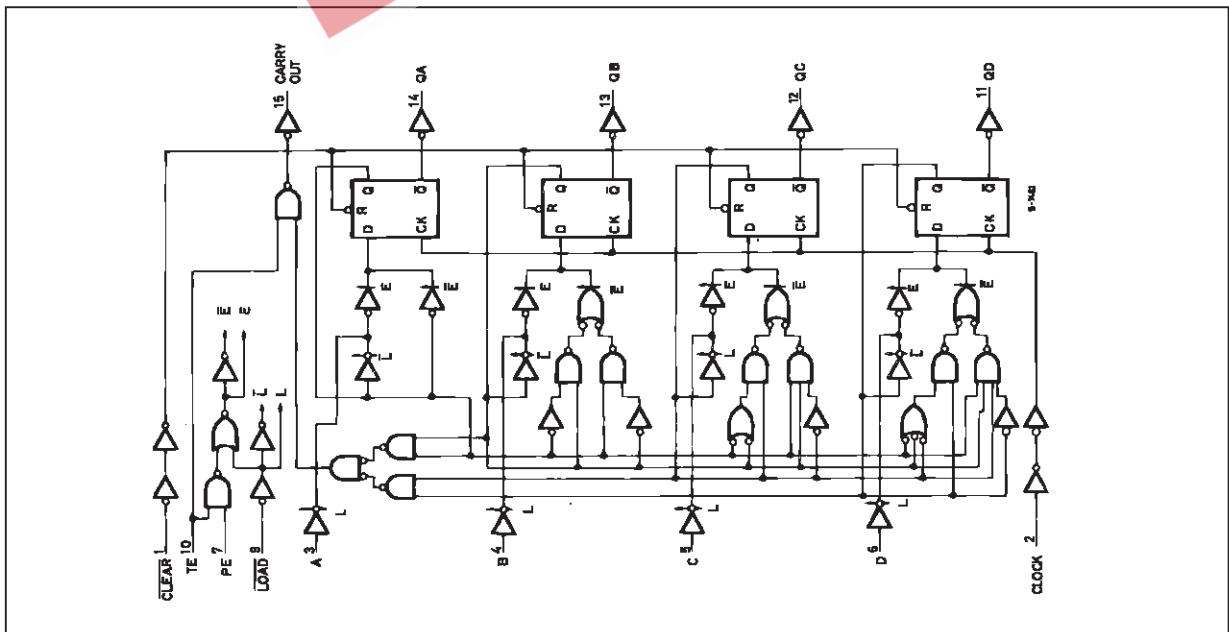
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Master Reset
2	CLOCK	Clock Input (LOW-to-HIGH, Edge- Triggered)
3, 4, 5, 6	A, B, C, D	Data Inputs
7	PE	Count Enable Input
10	$\overline{\text{TE}}$	Count Enable Carry Input
9	$\overline{\text{LOAD}}$	Parallel Enable Input
14, 13, 12, 11	QA to QD	Flip-Flop Output
15	CARRY OUT	Terminal Count Output
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

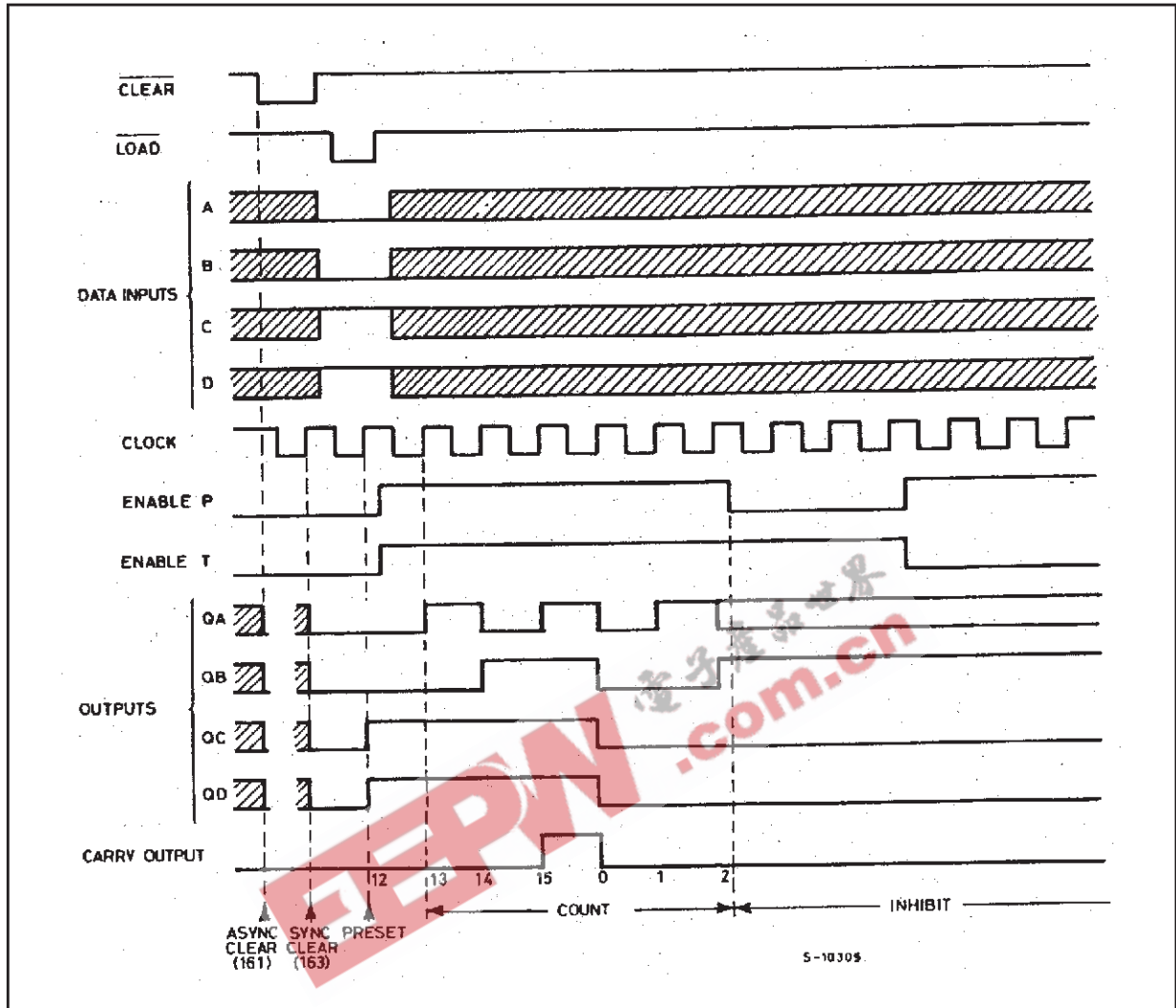
INPUTS					OUTPUTS				FUNCTION
$\overline{\text{CLEAR}}$	$\overline{\text{LOAD}}$	PE	TE	CLOCK	QA	QB	QC	QD	
L	X	X	X	X	L	L	L	L	RESET TO "0"
H	L	X	X		A	B	C	D	PRESET DATA
H	H	X	L		NO CHANGE				NO COUNT
H	H	L	X		NO CHANGE				NO COUNT
H	H	H	H		COUNT UP				COUNT
H	X	X	X		NO CHANGE				NO COUNT

NOTE: X: Don't Care
 A, B, C, D: Logic level of data input
 $\text{CARRY OUT} = \text{TE} \cdot \text{QA} \cdot \text{QB} \cdot \text{QC} \cdot \text{QD}$

LOGIC DIAGRAMS



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 300	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature:	-40 to +85	$^{\circ}C$
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0, 4.5$ or 5.5 V (note 1)	8	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit	
				T _A = 25 °C			-40 to 85 °C			
				V _{CC} (V)	Min.	Typ.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} - 0.1 V	2.1	1.5		2.1		V	
		4.5		3.15	2.25		3.15			
		5.5		3.85	2.75		3.85			
V _{IL}	Low Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} - 0.1 V		1.5	0.9		0.9	V	
		4.5			2.25	1.35		1.35		
		5.5			2.75	1.65		1.65		
V _{OH}	High Level Output Voltage	3.0	V _I ^(*) = V _{IH} or V _{IL}	I _O = -50 μA	2.9	2.99		2.9	V	
		4.5		I _O = -50 μA	4.4	4.49		4.4		
		5.5		I _O = -50 μA	5.4	5.49		5.4		
		3.0		I _O = -12 mA	2.56			2.46		
		4.5		I _O = -24 mA	3.86			3.76		
		5.5		I _O = -24 mA	4.86			4.76		
V _{OL}	Low Level Output Voltage	3.0	V _I ^(*) = V _{IH} or V _{IL}	I _O = 50 μA		0.002	0.1		0.1	V
		4.5		I _O = 50 μA		0.001	0.1		0.1	
		5.5		I _O = 50 μA		0.001	0.1		0.1	
		3.0		I _O = 12 mA			0.36		0.44	
		4.5		I _O = 24 mA			0.36		0.44	
		5.5		I _O = 24 mA			0.36		0.44	
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			±0.1		±1	μA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			8		80	μA	
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75	mA	
I _{OHD}			V _{OHD} = 3.85 V min					-75	mA	

1) Maximum test duration 2ms, one output loaded at time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50 Ω.

(*) All outputs loaded.

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3 \text{ ns}$)

Symbol	Parameter	Test Condition		Value					Unit	
				V _{CC} (V)	T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time CK to Q	3.3 ^(*)		7.0	12.0		13.0	ns		
		5.0 ^(**)		5.0	9.0		10.0			
t _{PLH} t _{PHL}	Propagation Delay Time CK to CARRY OUT	3.3 ^(*)		8.5	14.0		15.0	ns		
		5.0 ^(**)		6.0	10.0		11.0			
t _{PLH} t _{PHL}	Propagation Delay Time TE to CARRY OUT	3.3 ^(*)		5.5	9.5		11.0	ns		
		5.0 ^(**)		3.5	6.5		7.5			
t _{PHL}	Propagation Delay Time CLR to Q	3.3 ^(*)		6.5	12.0		13.0	ns		
		5.0 ^(**)		5.5	9.0		10.0			
t _{PHL}	Propagation Delay Time CLR to CARRY OUT	3.3 ^(*)		7.0	12.0		13.0	ns		
		5.0 ^(**)		5.5	9.5		10.0			
t _{wL}	CLR pulse Width, LOW (LOAD)	3.3 ^(*)		3.0	5.5		7.5	ns		
		5.0 ^(**)		2.5	4.5		6.0			
t _w	CK pulse Width HIGH or LOW	3.3 ^(*)		2.0	3.5		4.0	ns		
		5.0 ^(**)		2.0	3.0		3.5			
t _s	Setup Time HIGH or LOW (INPUT to CLOCK)	3.3 ^(*)		4.0	13.5		16.0	ns		
		5.0 ^(**)		1.5	8.5		10.5			
t _h	Hold Time HIGH or LOW (INPUT to CLOCK)	3.3 ^(*)		-1.0	-1.0		0.5	ns		
		5.0 ^(**)		-0.5	0.5		1.0			
t _s	Setup Time HIGH or LOW (CLEAR to CLOCK)	3.3 ^(*)		3.0	11.5		14.0	ns		
		5.0 ^(**)		2.0	7.5		8.5			
t _h	Hold Time HIGH or LOW (CLEAR to CLOCK)	3.3 ^(*)		-2.5	0		0	ns		
		5.0 ^(**)		-2.0	0.5		1.0			
t _s	Setup Time HIGH or LOW (PE or TE to CLOCK)	3.3 ^(*)		3.0	6.0		7.0	ns		
		5.0 ^(**)		2.0	4.5		5.0			
t _h	Hold Time HIGH or LOW (PE or TE to CLOCK)	3.3 ^(*)		-3.5	0		0	ns		
		5.0 ^(**)		-2.0	0		0.5			
t _{REM}	Recovery Time CLR to CLOCK	3.3 ^(*)		-1.0	0		0.5	ns		
		5.0 ^(**)		-0.5	0.5		1.0			
f _{MAX}	Maximum Clock Frequency	3.3 ^(*)		70	110		60	MHz		
		5.0 ^(**)		110	165		95			

(*) Voltage range is 3.3V ± 0.3V

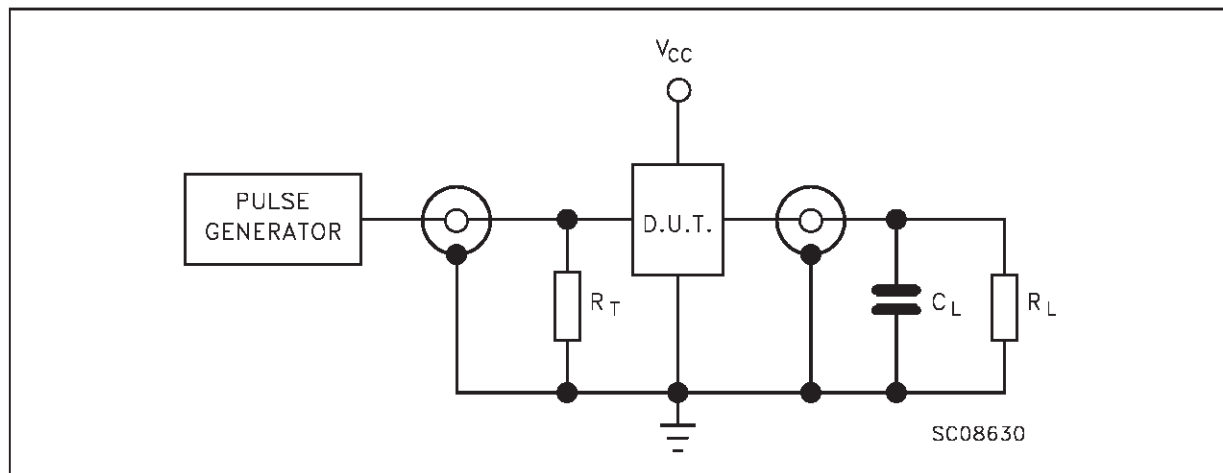
(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions		Value					Unit	
				V _{CC} (V)	T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			4.5				pF	
C _{PD}	Power Dissipation Capacitance (note 1)	5.0	f _{IN} = 10 MHz		45				pF	

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(oper)} = C_{PD} • V_{CC} • f_{IN} + I_{CC/n} (per circuit)

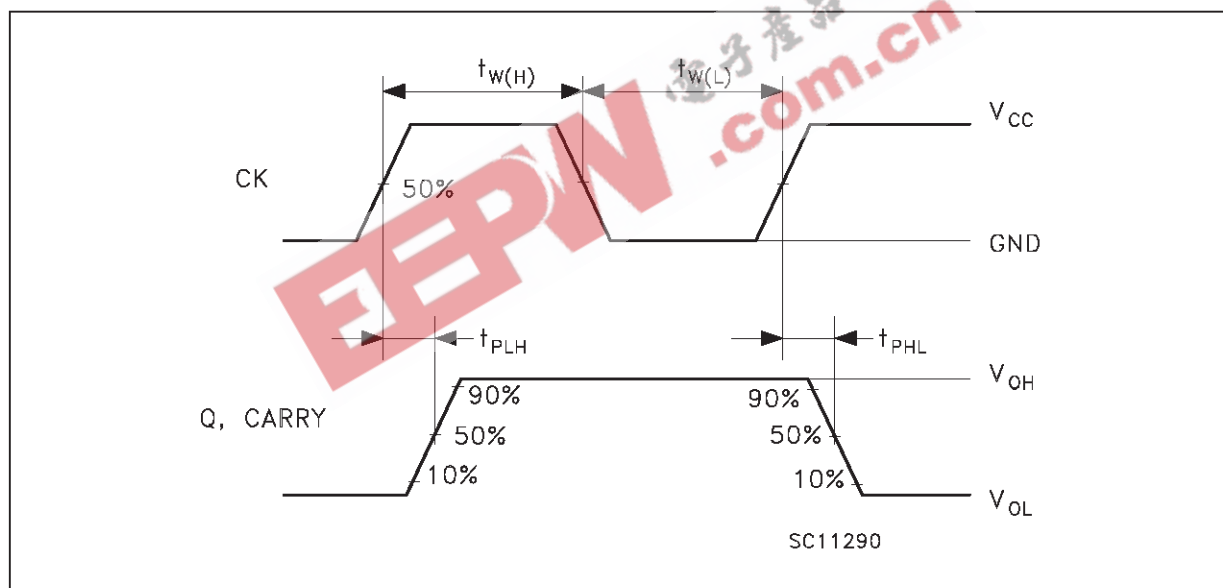
TEST CIRCUIT



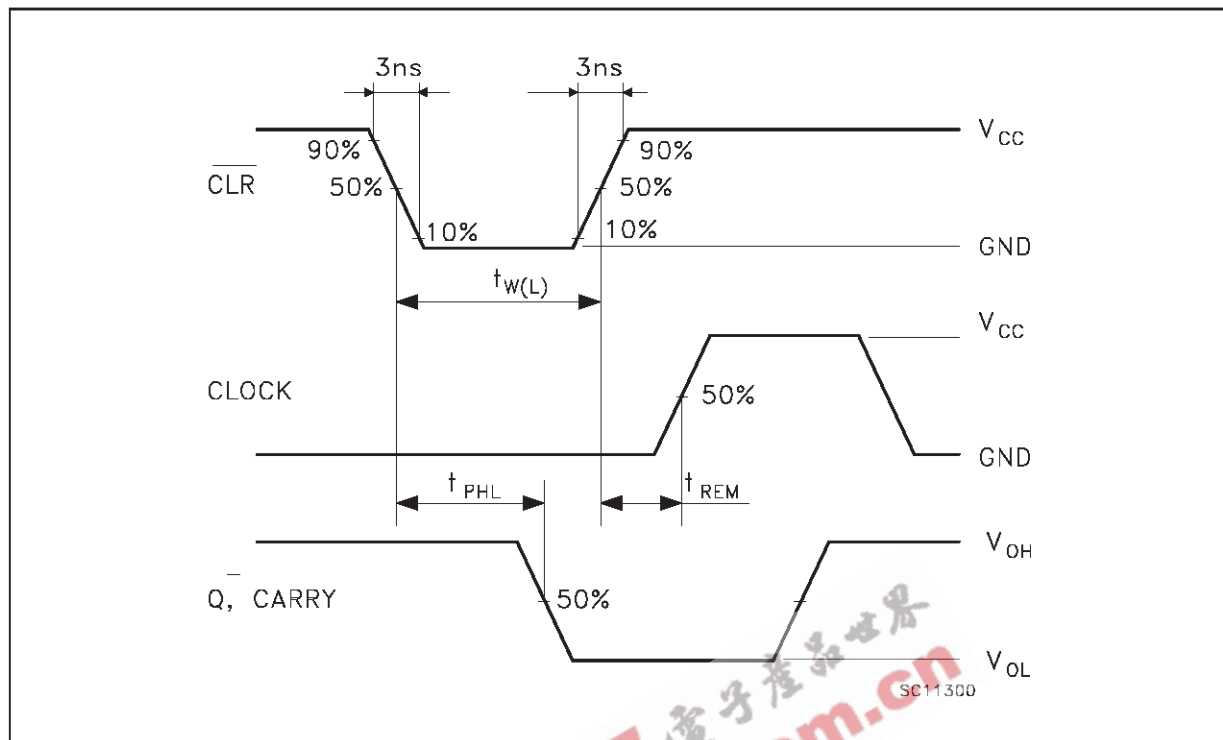
$C_L = 50$ pF or equivalent (includes jig and probe capacitance)

$R_L = R_T = 500\Omega$ or equivalent

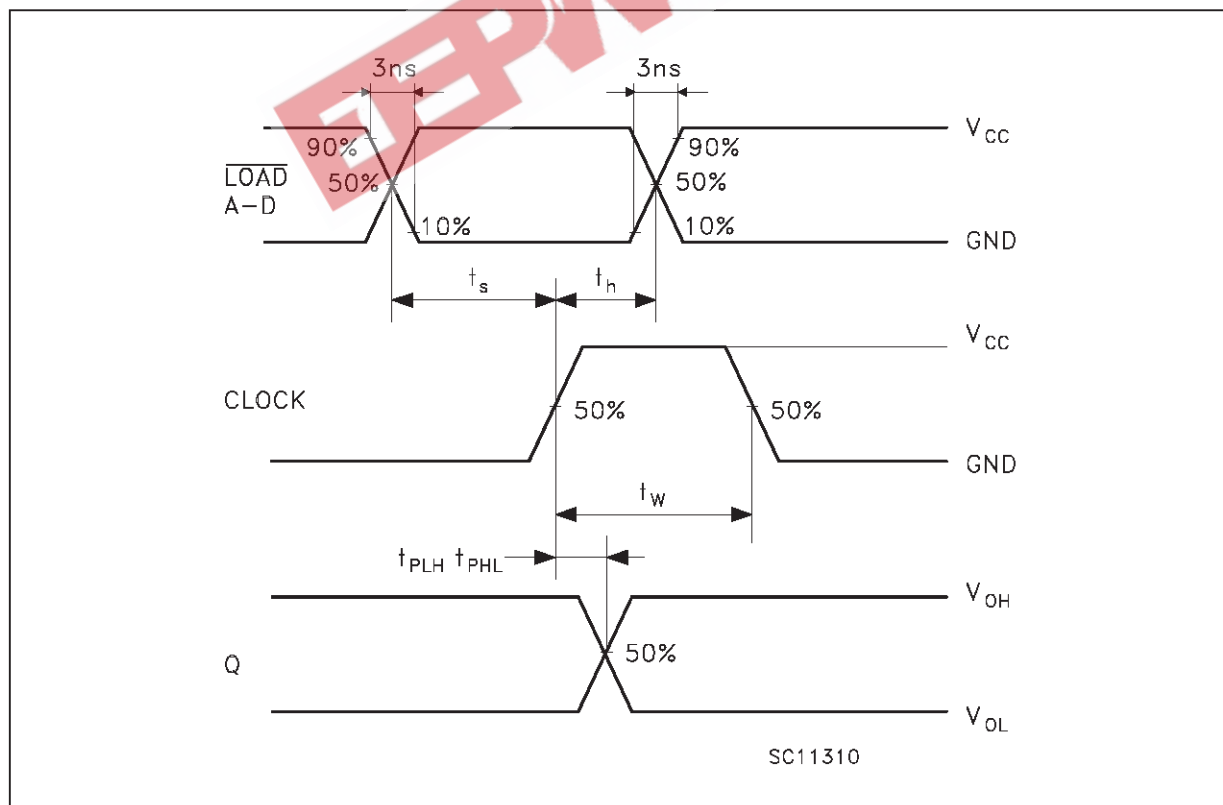
$R_T = Z_{out}$ of pulse generator (typically 50Ω)

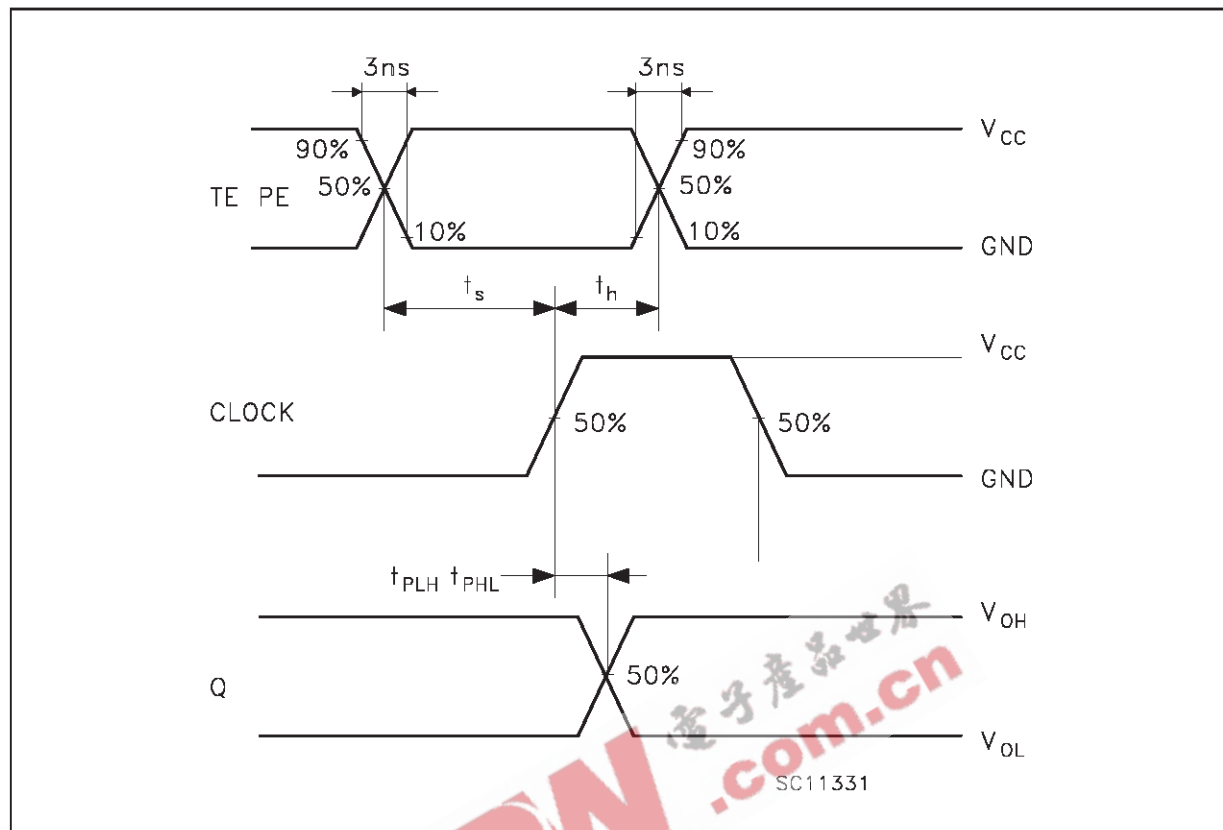
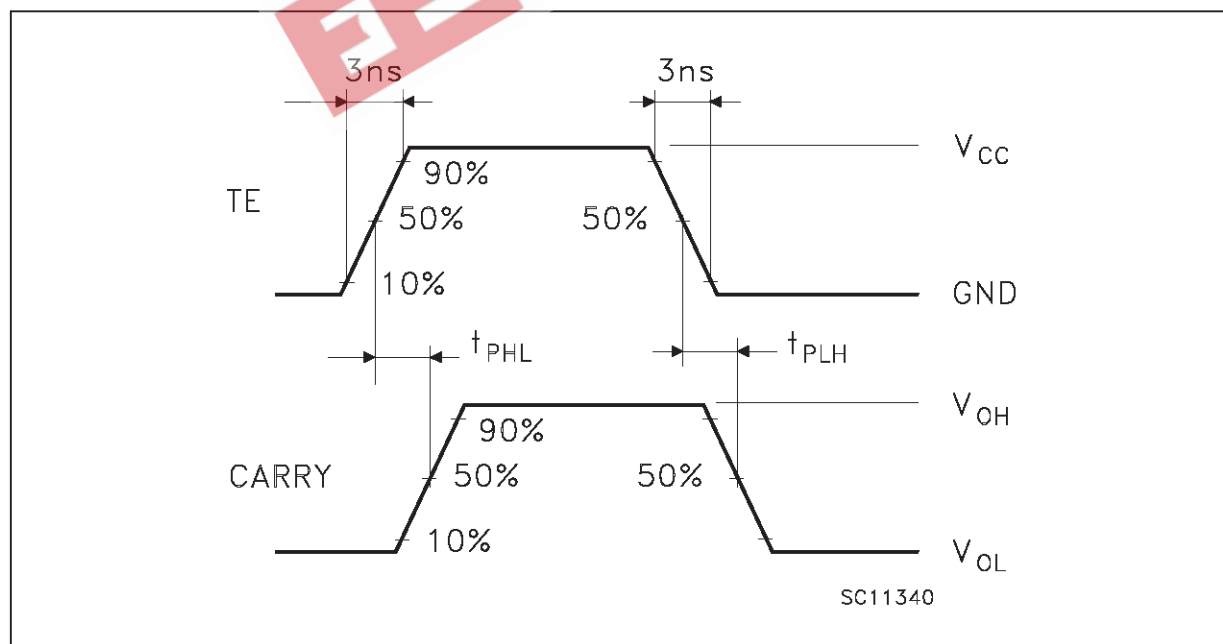
WAVEFORM 1: PROPAGATION DELAYS, COUNT MODE ($f=1$ MHz; 50% duty cycle)

WAVEFORM 2: PROPAGATION DELAYS CLEAR MODE (f=1MHz; 50% duty cycle)



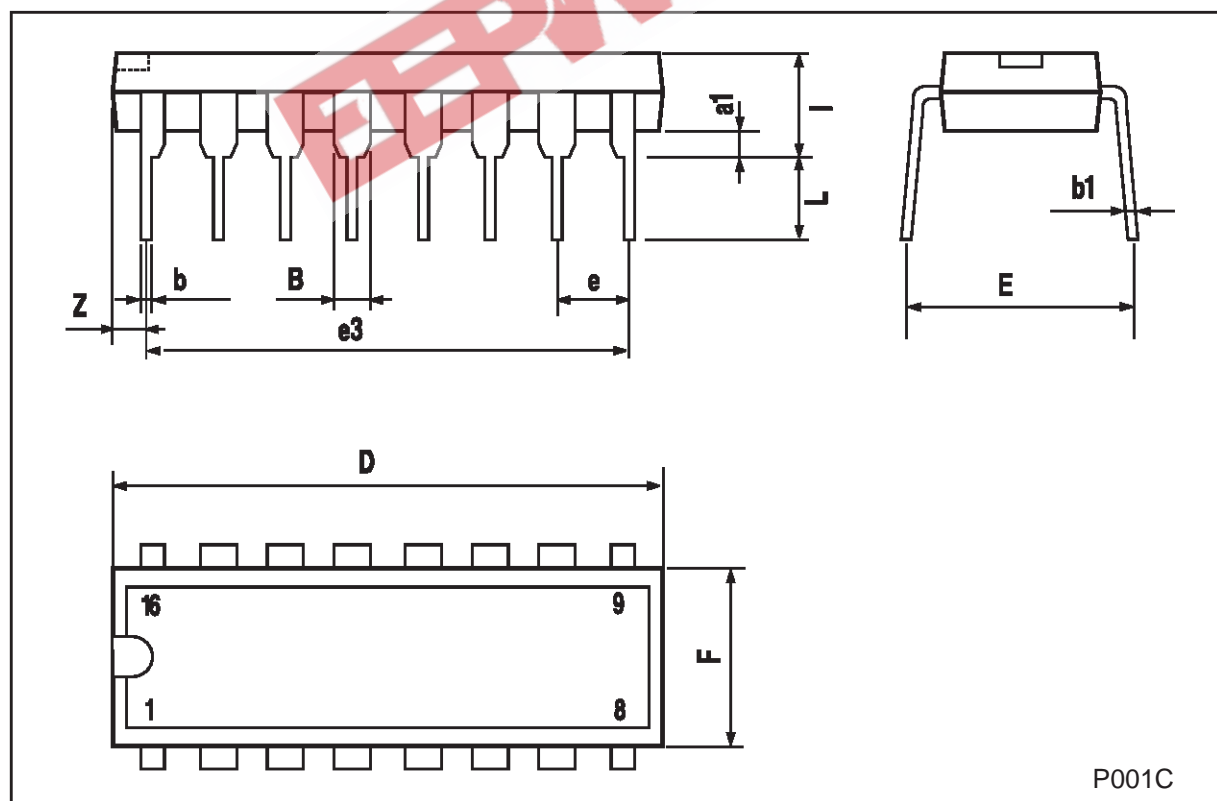
WAVEFORM 3: PROPAGATION DELAYS PRESET MODE (f=1MHz; 50% duty cycle)



WAVEFORM 4: PROPAGATION DELAYS COUNTABLE MODE ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 5: PROPAGATION DELAYS CASCADE MODE** ($f=1\text{MHz}$; 50% duty cycle)

Plastic DIP-16 (0.25) MECHANICAL DATA

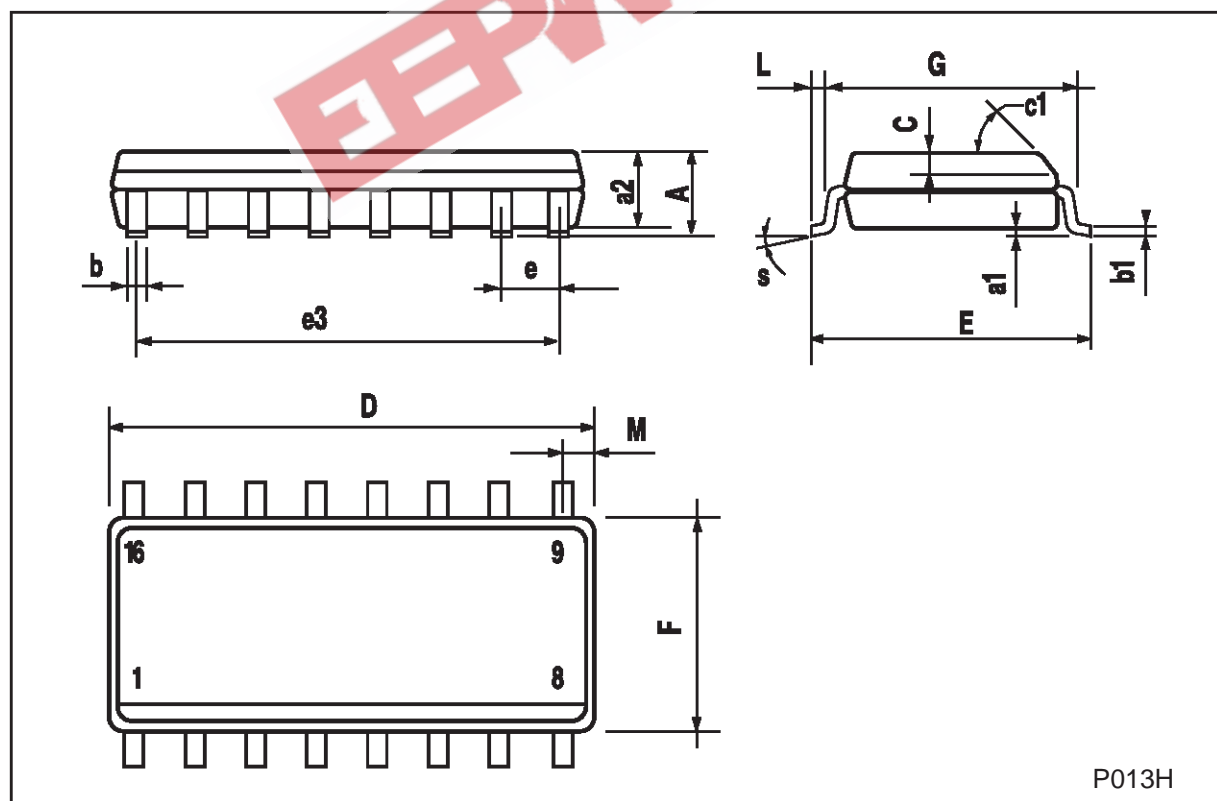
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



P001C

SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					





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