

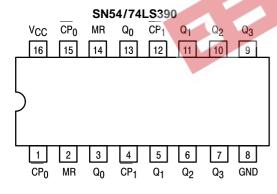
DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

The SN54/74LS390 and SN54/74LS393 each contain a pair of high-speed 4-stage ripple counters. Each half of the LS390 is partitioned into a divide-by-two section and a divide-by five section, with a separate clock input for each section. The two sections can be connected to count in the 8.4.2.1 BCD code or they can count in a biquinary sequence to provide a square wave (50% duty cycle) at the final output.

Each half of the LS393 operates as a Modulo-16 binary divider, with the last three stages triggered in a ripple fashion. In both the LS390 and the LS393, the flip-flops are triggered by a HIGH-to-LOW transition of their CP inputs. Each half of each circuit type has a Master Reset input which responds to a HIGH signal by forcing all four outputs to the LOW state.

- Dual Versions of LS290 and LS293
- LS390 has Separate Clocks Allowing ÷2, ÷2.5, ÷5
- Individual Asynchronous Clear for Each Counter
- Typical Max Count Frequency of 50 MHz
- Input Clamp Diodes Minimize High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



SN54/74LS393 VCC CP MR Q₀ Q₁ Q₂ Q₃ 14 13 12 11 10 9 8 1 2 3 4 5 6 7 CP MR Q₀ Q₁ Q₂ Q₃ GND

NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS390 SN54/74LS393

DUAL DECADE COUNTER; DUAL 4-STAGE BINARY COUNTER

LOW POWER SCHOTTKY



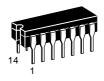
J SUFFIX CERAMIC CASE 620-09



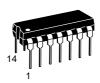
N SUFFIX PLASTIC CASE 648-08



D SUFFIX SOIC CASE 751B-03



J SUFFIX CERAMIC CASE 632-08



N SUFFIX PLASTIC CASE 646-06



D SUFFIX SOIC CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ Ceramic SN74LSXXXN Plastic SN74LSXXXD SOIC

PIN NAME	S	LOADIN	LOADING (Note a)			
		HIGH	LOW			
CP	Clock (Active LOW going edge) Input to +16 (LS393)	0.5 U.L.	1.0 U.L.			
CP ₀	Clock (Active LOW going edge) Input to ÷2 (LS390)	0.5 U.L.	1.0 U.L.			
CP ₁	Clock (Active LOW going edge) Input to ÷5 (LS390)	0.5 U.L.	1.5 U.L.			
MR	Master Reset (Active HIGH) Input	0.5 U.L.	0.25 U.L.			
Q_0-Q_3	Flip-Flop outputs (Note b)	10 U.L.	5 (2.5) U.L.			

NOTES

- a) 1 TTL Unit Load (U.L.) = 40 μ A HIGH/1.6 mA LOW.
- b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

FUNCTIONAL DESCRIPTION

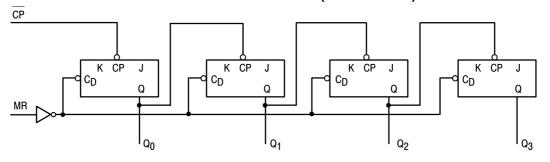
Each half of the SN54/74LS393 operates in the Modulo 16 binary sequence, as indicated in the ÷ 16 Truth Table. The first flip-flop is triggered by HIGH-to-LOW transitions of the CP input signal. Each of the other flip-flops is triggered by a HIGH-to-LOW transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A HIGH signal on MR forces all outputs to the LOW state and prevents counting.

Each half of the LS390 contains a ÷5 section that is independent except for the common MR function. The ÷5

section operates in 4.2.1 binary sequence, as shown in the $\div 5$ Truth Table, with the third stage output exhibiting a 20% duty cycle when the input frequency is constant. To obtain a $\div 10$ function having a 50% duty cycle output, connect the input signal to CP₁ and connect the Q₃ output to the CP₀ input; the Q₀ output provides the desired 50% duty cycle output. If the input frequency is connected to CP₀ and the Q₀ output is connected to CP₁, a decade divider operating in the 8.4.2.1 BCD code is obtained, as shown in the BCD Truth Table. Since the flip-flops change state asynchronously, logic signals derived from combinations of LS390 outputs are also subject to decoding spikes. A HIGH signal on MR forces all outputs LOW and prevents counting.

SN54/74LS390 LOGIC DIAGRAM (one half shown) CP₁ CP₀ Κ CP Κ CP Κ CP K CP J. C_D C_D C_D C_D a O a MR I_{Q_1} ΙQο $\mathsf{I}_{\mathsf{Q}_3}$ Q_2

SN54/74LS393 LOGIC DIAGRAM (one half shown)



SN54/74LS390 BCD TRUT<u>H TABLE</u> (Input on CP₀; Q₀ CP₁)

COUNT	OUTPUTS						
COUNT	Q ₃	Q_2	Q ₁	Q_0			
0	L	Г	L	L	-		
1	L	L	L	Н			
2	L	L	Н	L			
3	L	L	Н	Н	1		
3 4 5	L	Н	L	L	l		
5	L	Н	L	Н			
6	L	Н	Н	L			
7	L	Н	Н	Н			
8	Н	L	L	L	l		
9	Н	L	L	Н	Г		

SN54/74LS390 ÷ 5 TRUTH TABLE (Input on CP₁)

COUNT	Ol	JTPU	TS	
COUNT	Q_3	Q_2	Q ₁	
0	L	L	L	< ¬
1	L	L	Н	
2	L	Н	L	
3	L	Н	Н	
4	Н	L	L	

 $\begin{array}{c} \text{SN54/74LS390} \div \text{10 (50\% @ Q0)} \\ \text{TRUTH TABLE} \\ \text{(Input on CP$_1$, Q$_3$ to CP$_0$)} \end{array}$

(input on of 1, &3 to of 0)								
COUNT	OUTPUTS							
COUNT	Q ₃	Q ₂	Q ₁	Q ₀				
0	L	L	L	L	4			
1	L	L	Н	L ₂₆	. 1			
2	L	Н	L		-			
3	L	. Н.	€H	ЭΓ.				
3 4	H	L	- L	L	7			
5	L	L	L	H				
6	\L	L	H	Н	ĺ			
6 7	L	H	L	Н				
8	L	H	Н	Н				
9	Н	L	L	Н				

SN54/74LS393 TRUTH TABLE

COUNT		OUTF	PUTS		
COUNT	Q_3	Q ₂	Q ₁	Q_0	
0 1 2 3			L H H	LHLH	•
4 5 6 7		HHHH	LLHH	LHLH	
8 9 10 11	H H H H				
12 13 14 15	TTTT	1111			

H = HIGH Voltage Level L = LOW Voltage Level

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Тур	Max	Unit
Vcc	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
IOH	Output Current — High	54, 74			-0.4	mA
lOL	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

				Limits					
Symbol	Parameter		Min	Тур	Max	Unit	Test Conditions		
VIH	Input HIGH Voltage		2.0			V	Guaranteed Input All Inputs	t HIGH Voltage for	
V	Input I OW Voltage	54			0.7	V	Guaranteed Input	t LOW Voltage for	
V _{IL}	Input LOW Voltage	74			0.8]	All Inputs		
VIK	Input Clamp Diode Volta	age		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} =	: –18 mA	
Vau	Output HIGH Voltage	54	2.5	3.5		V	V _{CC} = MIN, I _{OH}	= MAX, V _{IN} = V _{IH}	
VOH	Output HIGH voltage	74	2.7	3.5		V	or V _{IL} per Truth T	āble	
	Output LOW Voltage	54, 74		0.25	0.4	V	I _{OL} = 4.0 mA	$V_{CC} = V_{CC} MIN,$ $V_{IN} = V_{IL} \text{ or } V_{IH}$	
VOL	Output LOW Voltage	74		0.35	0.5	V	I _{OL} = 8.0 mA	per Truth Table	
L	Input HIGH Current				20	μΑ	V _{CC} = MAX, V _{IN}	= 2.7 V	
lН	input HIGH Current				0.1	mA	V _{CC} = MAX, V _{IN}	= 7.0 V	
		MR			-0.4	mA	15		
I _{IL}	Input LOW Current	CP, CP ₀			-1.6	mA	$V_{CC} = MAX$, $V_{IN} = 0.4 V$		
		CP ₁		- 4	-2.4	mA	C		
los	Short Circuit Current (N	ote 1)	-20		-100	mA	V _{CC} = MAX		
Icc	Power Supply Current				26	mA	V _{CC} = MAX		

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

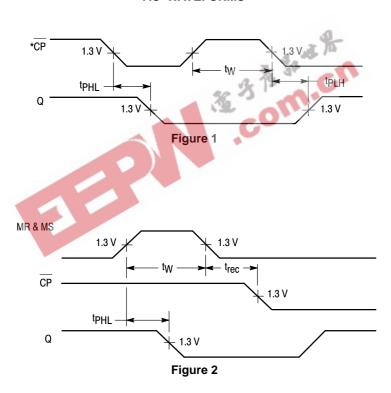
AC CHARACTERISTICS ($T_A = 25^{\circ}C$, $V_{CC} = 5.0 \text{ V}$)

				Limits			
Symbol	Paramete	er	Min	Тур	Max	Unit	Test Conditions
fMAX	Maximum Clock Freq CP ₀ to Q ₀	uency	25	35		MHz	
fMAX	Maximum Clock Freq CP ₁ to Q ₁	uency	20			MHz	
^t PLH ^t PHL	Propagation Delay, CP to Q ₀	LS393		12 13	20 20	ns	
^t PLH ^t PHL	CP ₀ to Q ₀	LS390		12 13	20 20	ns	
^t PLH ^t PHL	CP to Q ₃	LS393		40 40	60 60	ns	C _L = 15 pF
^t PLH ^t PHL	CP ₀ to Q ₂	LS390		37 39	60 60	ns	
^t PLH ^t PHL	CP ₁ to Q ₁	LS390		13 14	21 21	ns	
tPLH tPHL	CP ₁ to Q ₂	LS390		24 26	39 39	ns	
^t PLH ^t PHL	CP ₁ to Q ₃	LS390		13 14	21 21	ns	
^t PHL	MR to Any Output	LS390/393		24	39	ns	

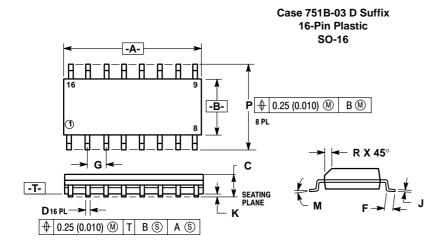
AC SETUP REQUIREMENTS (TA = 25°C, V_{CC} = 5.0 V)

			Limits				
Symbol	Parame	ter	Min	Тур	Max	Unit	Test Conditions
t _W	Clock Pulse Width	LS393	20			ns	
t _W	CP ₀ Pulse Width	LS390	20			ns	
t _W	CP ₁ Pulse Width	LS390	40			ns	V _{CC} = 5.0 V
t _W	MR Pulse Width	LS390/393	20			ns	
t _{rec}	Recovery Time	LS390/393	25			ns	

AC WAVEFORMS



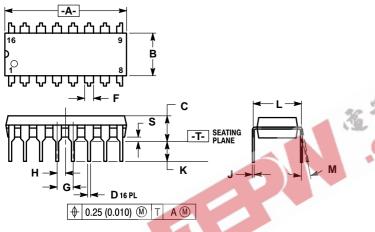
*The number of Clock Pulses required between t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Table.



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A AND B DO NOT INCLUDE MOLD 3. PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 (0.006)
- PER SIDE
- 751B-01 IS OBSOLETE, NEW STANDARD 751B-03.

	MILLIM	ETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	9.80	10.00	0.386	0.393	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050	BSC	
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
P	5.80	6.20	0.229	0.244	
R	0.25	0.50	0.010	0.019	

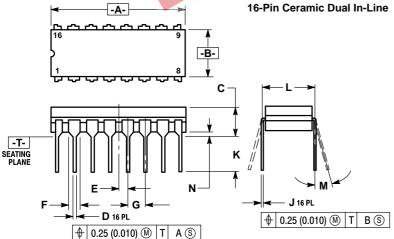
Case 648-08 N Suffix 16-Pin Plastic



NOTES:

Guffix C	2. 3. 4.	DIMENS Y14.5M, CONTR DIMENS FORME DIMENS FLASH. ROUND	1982. OLLING I SION "L" T D PARAL SION "B" I ED CORI	AND TOL DIMENSIO TO CENTI LEL. DOES NO NERS OP TOBSOLE	ON: INCH ER OF LE T INCLUI	ADS WH	EN)
26. 4	-	12	MILLIM	ETERS	INC	HES]
130	u	DIM	MIN	MAX	MIN	MAX	
30 43	-	Α	18.80	19.55	0.740	0.770	
130		В	6.35	6.85	0.250	0.270	
		С	3.69	4.44	0.145	0.175	
		D	0.39	0.53	0.015	0.021	
		F	1.02	1.77	0.040	0.070	
		G	2.54	BSC	0.100	BSC	
M		Н	1.27	BSC	0.050	BSC	
		J	0.21	0.38	0.008	0.015	
		K	2.80	3.30	0.110	0.130	
		L	7.50	7.74	0.295	0.305]
		M	0°	10°	0°	10°	
		S	0.51	1.01	0.020	0.040]

Case 620-09 J Suffix



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 114.3W, 1906.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
 5. 620-01 THRU -08 OBSOLETE, NEW STANDARD

	MILLIM	ETERS	INC	HES		
DIM	MIN	MAX	MIN	MAX		
Α	19.05	19.55	0.750	0.770		
В	6.10	7.36	0.240	0.290		
С	-	4.19	_	0.165		
D	0.39	0.53	0.015 0.02			
E	1.27	BSC	0.050	BSC		
F	1.40	1.77	0.055	0.070		
G	2.54	BSC	0.100	BSC		
J	0.23	0.27	0.009	0.011		
K	_	5.08	_	0.200		
L	7.62	BSC	0.300	BSC		
M	0°	15°	0°	15°		
N	0.39	0.88	0.015	0.035		



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