

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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## 74HC/HCT393

### Dual 4-bit binary ripple counter

Product specification  
File under Integrated Circuits, IC06

December 1990

## Dual 4-bit binary ripple counter

## 74HC/HCT393

## FEATURES

- Two 4-bit binary counters with individual clocks
- Divide-by any binary module up to 28 in one package
- Two master resets to clear each 4-bit counter individually
- Output capability: standard
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT393 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT393 are 4-bit binary ripple counters with separate clocks (1 $\overline{CP}$  and 2 $\overline{CP}$ ) and master reset (1MR and 2MR) inputs to each counter. The operation of each half of the "393" is the same as the "93" except no external clock connections are required.

The counters are triggered by a HIGH-to-LOW transition of the clock inputs. The counter outputs are internally connected to provide clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high-speed address decoding.

The master resets are active-HIGH asynchronous inputs to each 4-bit counter identified by the "1" and "2" in the pin description.

A HIGH level on the nMR input overrides the clock and sets the outputs LOW.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $\overline{nCP}$ to $nQ_0$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	12	20	ns
	$nQ$ to $nQ_{n+1}$		5	6	ns
	$nMR$ to $nQ_n$		11	15	ns
$f_{max}$	maximum clock frequency		99	53	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per counter	notes 1 and 2	23	25	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

## ORDERING INFORMATION

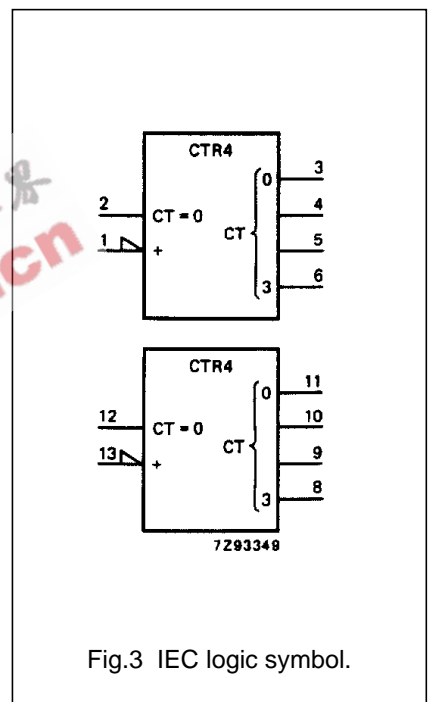
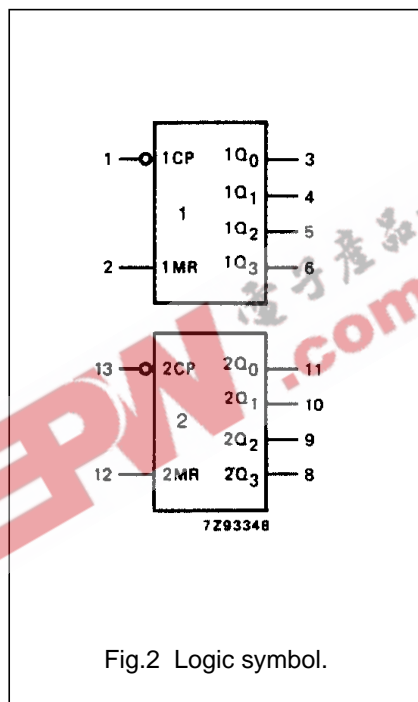
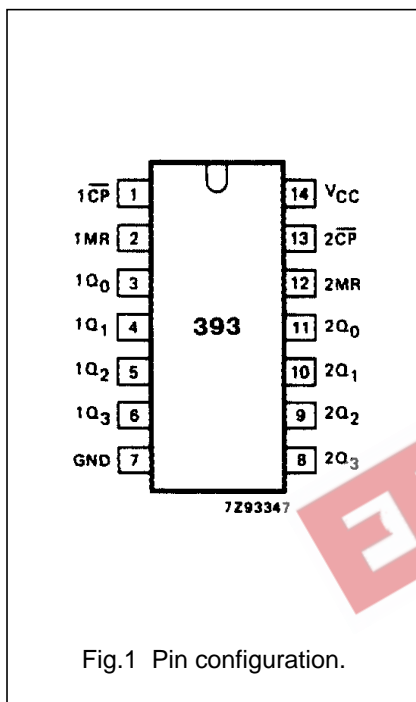
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Dual 4-bit binary ripple counter

74HC/HCT393

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 13	1CP, 2CP	clock inputs (HIGH-to-LOW, edge-triggered)
2, 12	1MR, 2MR	asynchronous master reset inputs (active HIGH)
3, 4, 5, 6, 11, 10, 9, 8	1Q <sub>0</sub> to 1Q <sub>3</sub> , 2Q <sub>0</sub> to 2Q <sub>3</sub>	flip-flop outputs
7	GND	ground (0 V)
14	V <sub>CC</sub>	positive supply voltage



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74HC/HCT393

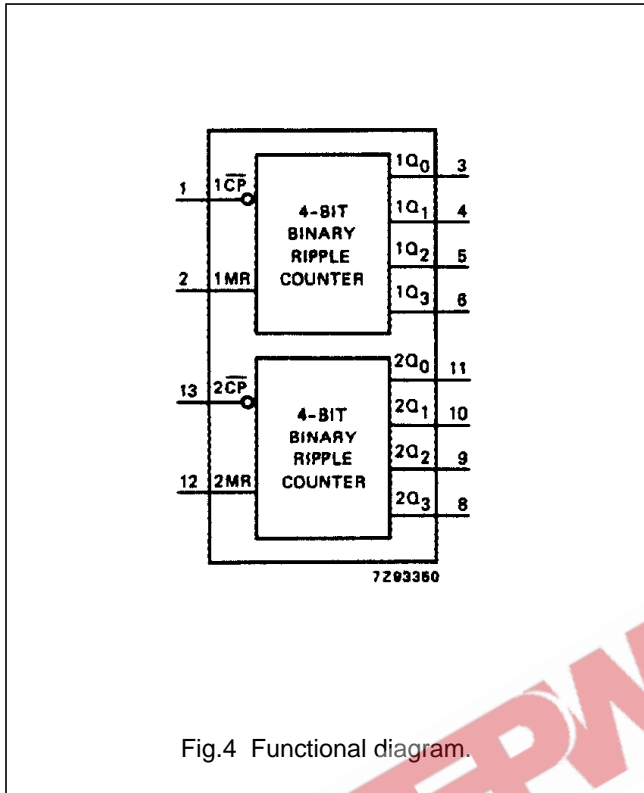


Fig.4 Functional diagram.

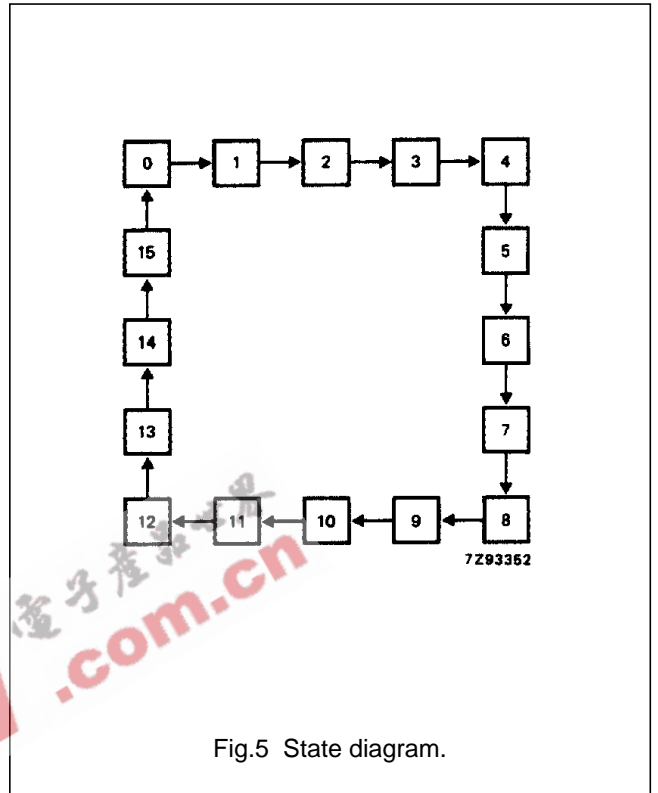


Fig.5 State diagram.

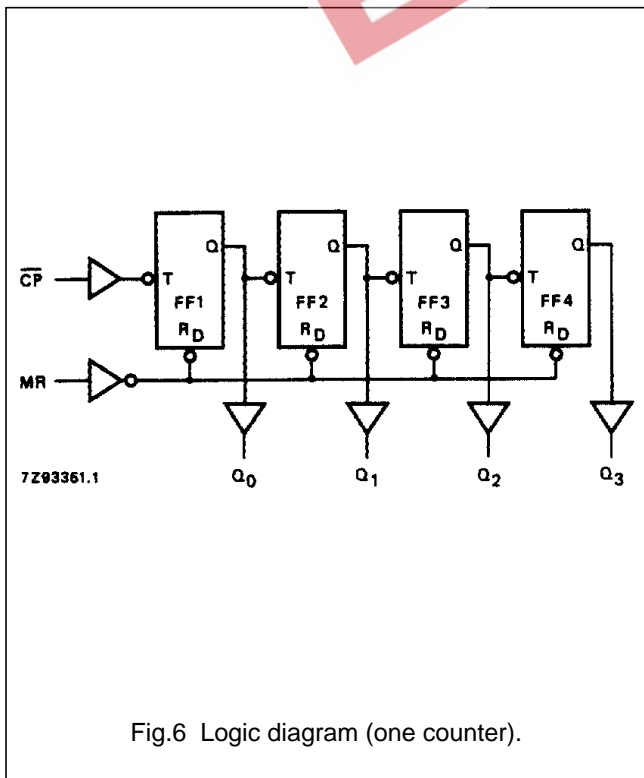


Fig.6 Logic diagram (one counter).

COUNT SEQUENCE FOR 1 COUNTER

COUNT	OUTPUTS			
	Q <sub>0</sub>	Q <sub>1</sub>	Q <sub>2</sub>	Q <sub>3</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Notes

- H = HIGH voltage level  
L = LOW voltage level

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ <sub>0</sub>		41 15 12	125 25 21		155 31 26	190 38 32	ns	2.0 4.5 6.0	Fig.7	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nQ <sub>n</sub> to nQ <sub>n+1</sub>		14 5 4	45 9 8		55 11 9	70 14 12	ns	2.0 4.5 6.0	Fig.7	
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		39 14 11	140 28 24		175 35 30	210 42 36	ns	2.0 4.5 6.0	Fig.8	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16	110 22 19	ns	2.0 4.5 6.0	Fig.7	
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.7	
t <sub>w</sub>	master reset pulse width; HIGH	80 16 14	19 7 6		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.8	
t <sub>rem</sub>	removal time nMR to nCP	5 5 5	3 1 1		5 5 5		5 5 5	ns	2.0 4.5 6.0	Fig.8	
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	30 90 107		5 24 28		4 20 24	MHz	2.0 4.5 6.0	Fig.7	

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## 74HC/HCT393

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1CP	0.4
2CP	0.4
1MR	1.0
2MR	1.0

**AC CHARACTERISTICS FOR 74HCT**

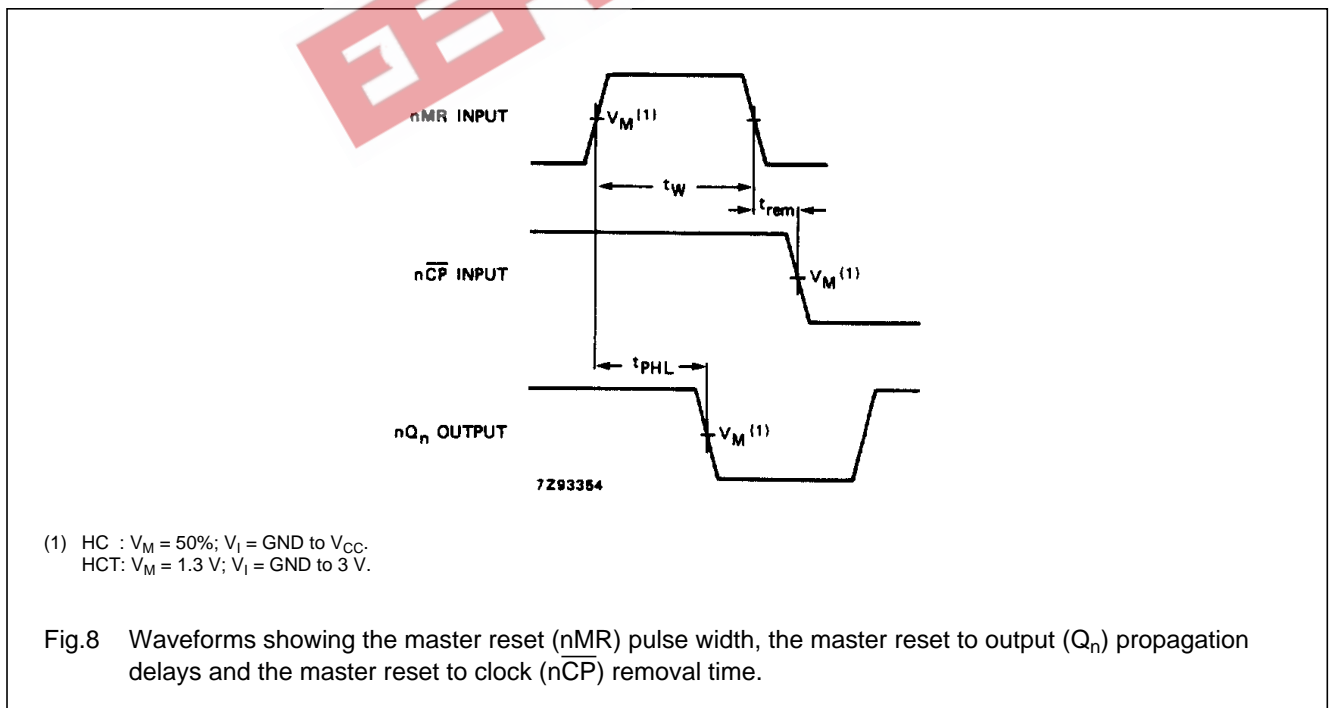
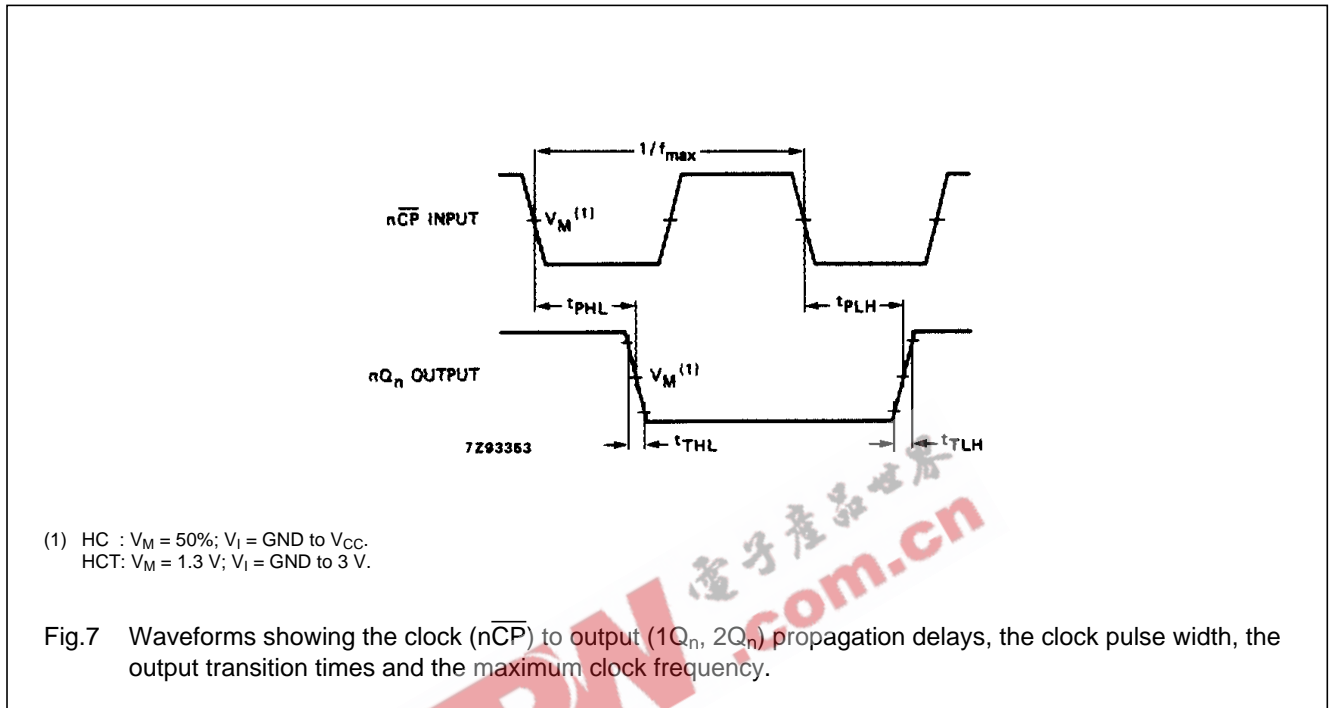
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HCT								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nCP to nQ <sub>0</sub>		15	25		31		38	ns	4.5	Fig.7
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nQ <sub>n</sub> to nQ <sub>n+1</sub>		6	10		13		15	ns	4.5	Fig.7
t <sub>PHL</sub>	propagation delay nMR to nQ <sub>n</sub>		18	32		40		48	ns	4.5	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.7
t <sub>w</sub>	clock pulse width HIGH or LOW	19	11		24		29		ns	4.5	Fig.7
t <sub>w</sub>	master reset pulse width; HIGH	16	6		20		24		ns	4.5	Fig.8
t <sub>rem</sub>	removal time nMR to nCP	5	0		5		5		ns	4.5	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig.7

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".