National *Semiconductor*

54F/74F181
4-Bit Arithmetic Logic Unit

General Description

The 'F181 is a 4-bit Arithmetic logic Unit (ALU) which can perform all the possible 16 logic operations on two variables and a variety of arithmetic operations. It is 40% faster than the Schottky ALU and only consumes 30% as much power.

Features

- Full lookahead for high-speed arithmetic operation on long words
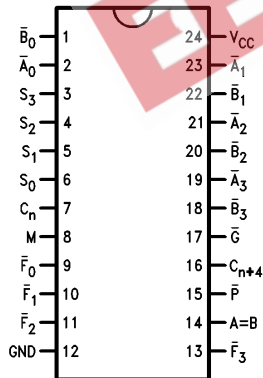- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F181PC		N24A	24-Lead (0.600″ Wide) Molded Dual-In-Line
74F181SPC		N24C	24-Lead (0.300″ Wide) Molded Dual-In-Line
	54F181DM (Note 2)	J24A	24-Lead Ceramic Dual-In-Line
	54F181SDM (Note 2)	J24F	24-Lead (0.300″) Ceramic Dual-In-Line
74F181SC (Note 1)		M24B	24-Lead (0.300″) Molded Small Outline, JEDEC
	54F181FM (Note 2)	W24C	24-Lead Cerpack
	54F181LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier,Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX.

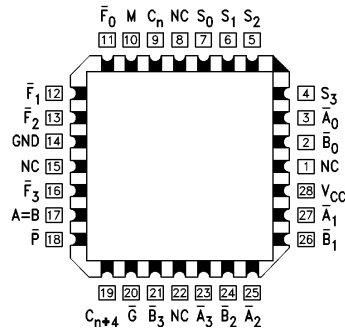**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Connection Diagrams

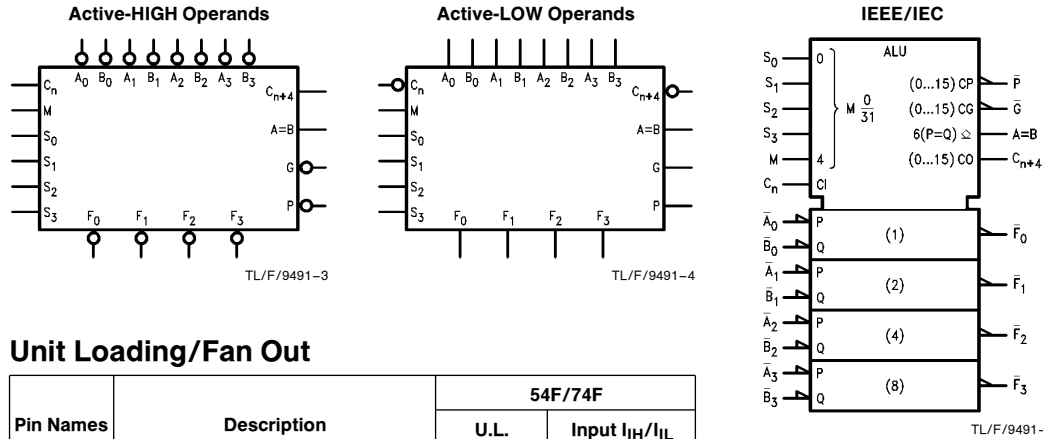**Pin Assignment
for DIP, SOIC and Flatpak**

TL/F/9491–1

**Pin Assignment
for LCC**

TL/F/9491–2

Logic Symbols

Active-HIGH Operands

TL/F/9491–3

Active-LOW Operands

TL/F/9491–4

IEEE/IEC

TL/F/9491–10

Unit Loading/Fan Out

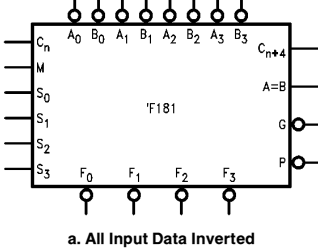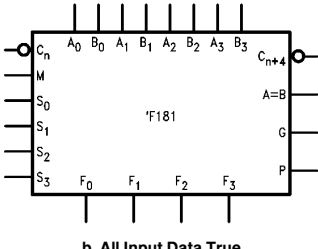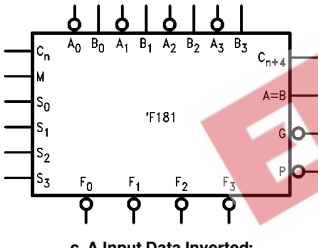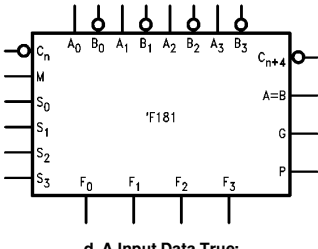| Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{A}_0–\overline{A}_3$	A Operand Inputs (Active LOW)	1.0/3.0	20 µA/−1.8 mA
$\overline{B}_0–\overline{B}_3$	B Operand Inputs (Active LOW)	1.0/3.0	20 µA/−1.8 mA
$S_0–S_3$	Function Select Inputs	1.0/4.0	20 µA/−2.4 mA
M	Mode Control Input	1.0/1.0	20 µA/−0.6 mA
C_n	Carry Input	1.0/5.0	20 µA/−3.0 mA
$\overline{F}_0–\overline{F}_3$	Function Outputs (Active LOW)	50/33.3	−1 mA/20 mA
A = B	Comparator Output	OC*/33.3	*/20 mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	−1 mA/20 mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	−1 mA/20 mA
C_{n+4}	Carry Output	50/33.3	−1 mA/20 mA

*OC-Open Collector

Functional Description

The 'F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0–S_3$) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on Active HIGH or Active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). In the Add mode, $\overline{P}$ indicates that $\overline{F}$ is 15 or more, while $\overline{G}$ indicates that $\overline{F}$ is 16 or more. In the Subtract mode $\overline{P}$ indicates that $\overline{F}$ is zero or less, while $\overline{G}$ indicates that $\overline{F}$ is less than zero. $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed requirements are not stringent, the 'F181 can be used in a simple Ripple Carry mode by connecting the Carry output ($C_n + 4$) signal to the Carry input (C_n) of the next unit. For high speed operation the device is used in conjunction with a carry lookahead circuit. One carry lookahead package is required for each group of four 'F181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the Subtract mode. The A = B output is open collector and can be wired AND with other A = B outputs to give a comparison for more than four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

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'F181 Operation Table

a. All Input Data Inverted

S_0	S_1	S_2	S_3	Logic (M=H)	Arithmetic (M=L, C_0=Inactive)	Arithmetic (M=L, C_0=Active)
L	L	L	L	$\overline{A}$	A minus 1	A
H	L	L	L	$\overline{A}\bullet\overline{B}$	A $\bullet$ B minus 1	A $\bullet$ B
L	H	L	L	$\overline{A}+B$	A $\bullet$ $\overline{B}$ minus 1	A $\bullet$ $\overline{B}$
H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A+\overline{B}}$	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
H	L	H	L	$\overline{B}$	A $\bullet$ B plus (A + $\overline{B}$)	A $\bullet$ B plus (A + $\overline{B}$) plus 1
L	H	H	L	$\overline{A\oplus B}$	A minus B minus 1	A minus B
H	H	H	L	A + $\overline{B}$	A + $\overline{B}$	A + $\overline{B}$ plus 1
L	L	L	H	$\overline{A}\bullet B$	A plus (A + B)	A plus (A + B) plus 1
H	L	L	H	A $\oplus$ B	A plus B	A plus B plus 1
L	H	L	H	B	A $\bullet$ $\overline{B}$ plus (A + B)	A $\bullet$ $\overline{B}$ plus (A + B) plus 1
H	H	L	H	A + B	A + B	A + B plus 1
L	L	H	H	Logic "0"	A plus A ($2 \times$ A)	A plus A ($2 \times$ A) plus 1
H	L	H	H	A $\bullet$ $\overline{B}$	A plus A $\bullet$ B	A plus A $\bullet$ B plus 1
L	H	H	H	A $\bullet$ B	A plus A $\bullet$ $\overline{B}$	A plus A $\bullet$ $\overline{B}$ plus 1
H	H	H	H	A	A	A plus 1

a. All Input Data Inverted

b. All Input Data True

S_0	S_1	S_2	S_3	Logic (M=H)	Arithmetic (M=L, C_0=Inactive)	Arithmetic (M=L, C_0=Active)
L	L	L	L	$\overline{A}$	A	A plus 1
H	L	L	L	$\overline{A + B}$	A + B	A + B plus 1
L	H	L	L	$\overline{A}\bullet B$	A + $\overline{B}$	A + $\overline{B}$ plus 1
H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A}\bullet\overline{B}$	A plus (A $\bullet$ $\overline{B}$)	A plus A $\bullet$ $\overline{B}$ plus 1
H	L	H	L	$\overline{B}$	A $\bullet$ $\overline{B}$ plus (A + B)	A $\bullet$ B plus (A + B) plus 1
L	H	H	L	A $\oplus$ B	A minus B minus 1	A minus B
H	H	H	L	A $\bullet$ $\overline{B}$	A $\bullet$ $\overline{B}$ minus 1	A $\bullet$ $\overline{B}$
L	L	L	H	$\overline{A} + B$	A plus A $\bullet$ B	A plus A $\bullet$ B plus 1
H	L	L	H	$\overline{A\oplus B}$	A plus B	A plus B plus 1
L	H	L	H	B	A $\bullet$ B plus (A + $\overline{B}$)	A $\bullet$ B plus (A + $\overline{B}$) plus 1
H	H	L	H	A $\bullet$ B	A $\bullet$ B minus 1	A $\bullet$ B
L	L	H	H	Logic "1"	A plus A ($2 \times$ A)	A plus A ($2 \times$ A) plus 1
H	L	H	H	A + $\overline{B}$	A plus (A + B)	A plus (A + B) plus 1
L	H	H	H	A + B	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
H	H	H	H	A	A minus 1	A

b. All Input Data True

c. A Input Data Inverted; B Input Data True

S_0	S_1	S_2	S_3	Logic (M=H)	Arithmetic (M=L, C_0=Inactive)	Arithmetic (M=L, C_0=Active)
L	L	L	L	$\overline{A}$	A minus 1	A
H	L	L	L	$\overline{A} + B$	A $\bullet$ $\overline{B}$ minus 1	A $\bullet$ B
L	H	L	L	$\overline{A}\bullet B$	A $\bullet$ B minus 1	A $\bullet$ B
H	H	L	L	Logic "1"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A}\bullet B$	A plus (A + B)	A plus (A + B) plus 1
H	L	H	L	B	A $\bullet$ $\overline{B}$ plus (A + B)	A $\bullet$ $\overline{B}$ plus (A + B) plus 1
L	H	H	L	A $\oplus$ B	A plus B	A plus B plus 1
H	H	H	L	A + B	A + B	A + B plus 1
L	L	L	H	$\overline{A + B}$	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
H	L	L	H	$\overline{A\oplus B}$	A minus B minus 1	A minus B
L	H	L	H	$\overline{B}$	A $\bullet$ B plus (A + $\overline{B}$)	A $\bullet$ B plus (A + $\overline{B}$) plus 1
H	H	L	H	A + $\overline{B}$	A + $\overline{B}$	A + $\overline{B}$ plus 1
L	L	H	H	Logic "0"	A plus A ($2 \times$ A)	A plus A ($2 \times$ A) plus 1
H	L	H	H	A $\bullet$ B	A plus A $\bullet$ $\overline{B}$	A plus A $\bullet$ $\overline{B}$ plus 1
L	H	H	H	A $\bullet$ $\overline{B}$	A plus A $\bullet$ B	A plus A $\bullet$ B plus 1
H	H	H	H	A	A	A plus 1

c. A Input Data Inverted; B Input Data True

d. A Input Data True; B Input Date Inverted

S_0	S_1	S_2	S_3	Logic (M=H)	Arithmetic (M=L, C_0=Inactive)	Arithmetic (M=L, C_0=Active)
L	L	L	L	$\overline{A}$	A	A plus 1
H	L	L	L	$\overline{A}\bullet B$	A + $\overline{B}$	A + $\overline{B}$ plus 1
L	H	L	L	$\overline{A + B}$	A + B	A + B plus 1
H	H	L	L	Logic "0"	minus 1 (2s comp.)	Zero
L	L	H	L	$\overline{A} + B$	A plus A $\bullet$ B	A plus A $\bullet$ B plus 1
H	L	H	L	B	A $\bullet$ B plus (A + $\overline{B}$)	A $\bullet$ $\overline{B}$ plus (A + B) plus 1
L	H	H	L	$\overline{A\oplus B}$	A plus B	A plus B plus 1
H	H	H	L	A $\bullet$ B	A $\bullet$ B minus 1	A $\bullet$ B
L	L	L	H	$\overline{A}\bullet\overline{B}$	A plus A $\bullet$ $\overline{B}$	A plus A $\bullet$ B plus 1
H	L	L	H	A $\oplus$ B	A minus B minus 1	A minus B
L	H	L	H	$\overline{B}$	A $\bullet$ $\overline{B}$ plus (A + B)	A $\bullet$ B plus (A + $\overline{B}$) plus 1
H	H	L	H	A $\bullet$ $\overline{B}$	A $\bullet$ $\overline{B}$ minus 1	A $\bullet$ $\overline{B}$
L	L	H	H	Logic "1"	A plus A ($2 \times$ A)	A plus A ($2 \times$ A) plus 1
H	L	H	H	A + B	A plus (A + $\overline{B}$)	A plus (A + $\overline{B}$) plus 1
L	H	H	H	A + $\overline{B}$	A plus (A + B)	A plus (A + B) plus 1
H	H	H	H	A	A minus 1	A

d. A Input Data True; B Input Date Inverted

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Logic Diagram

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$
V_{CC} Pin Potential to Ground Pin	$-0.5V$ to $+7.0V$
Input Voltage (Note 2)	$-0.5V$ to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA

Voltage Applied to Output
in HIGH State (with $V_{CC} = 0V$)

Standard Output	$-0.5V$ to V_{CC}
TRI-STATE® Output	$-0.5V$ to $+5.5V$

Current Applied to Output
in LOW State (Max)   twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min)   4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature

Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$

Supply Voltage

Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA
		74F 10% V_{CC}	2.5					$I_{OH} = -1$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	$V_{IN} = 2.7V$
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	$V_{IN} = 7.0V$
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	$V_{OUT} = V_{CC}$ ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, C_{n+4})
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9\ \mu$A All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$ (M)
					-1.8			$V_{IN} = 0.5V$ ($\overline{A}_0$, $\overline{A}_1$, $\overline{A}_3$, $\overline{B}_0$, $\overline{B}_1$, $\overline{B}_3$)
					-2.4			$V_{IN} = 0.5V$ (S_n, $\overline{A}_2$, $\overline{B}_2$)
					-3.0			$V_{IN} = 0.5V$ (C_n)
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$ ($\overline{F}_n$, $\overline{G}$, $\overline{P}$, C_{n+4})
I_{OHC}	Open Collector, Output OFF Leakage Test				250	μA	Min	$V_O = V_{CC}$ (A = B)
I_{CCH}	Power Supply Current			43	65.0	mA	Max	$V_O = $ HIGH
I_{CCL}	Power Supply Current			43	65.0	mA	Max	$V_O = $ LOW

AC Electrical Characteristics

Symbol	Parameter		74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units
	Path	Mode	Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_n to C_{n+4}		3.0 3.0	6.4 6.1	8.5 8.0	3.0 3.0	10.0 9.5	3.0 3.0	9.5 9.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	Sum	5.0 4.0	10.0 9.4	13.0 12.0	5.0 3.5	15.5 16.5	5.0 4.0	14.0 13.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to C_{n+4}	Dif	5.0 5.0	10.8 10.0	14.0 13.0	5.0 4.0	17.0 15.0	5.0 5.0	15.0 14.0	ns
t_{PLH} t_{PHL}	Propagation Delay C_n to $\overline{F}$	Any	3.0 3.0	6.7 6.5	8.5 8.5	2.5 2.5	16.0 12.0	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ or $\overline{G}$	Sum	3.0 3.0	5.7 5.8	7.5 7.5	2.5 2.5	9.0 9.5	3.0 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{G}$	Dif	3.0 3.0	6.5 7.3	8.5 9.5	2.5 2.5	11.5 11.0	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	Sum	3.0 3.0	5.0 5.5	7.0 7.5	2.5 3.0	8.5 9.5	3.0 3.0	8.0 8.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{P}$	Dif	3.0 4.0	5.8 6.5	7.5 8.5	2.5 3.0	11.0 11.0	3.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Sum	3.0 3.0	7.0 7.2	9.0 10.0	3.0 3.0	14.5 14.5	3.0 3.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}_i$ or $\overline{B}_i$ to $\overline{F}_i$	Dif	3.0 3.0	8.2 5.0	11.0 11.0	3.0 3.0	17.5 14.5	3.0 3.0	12.0 12.0	ns
t_{PLH} t_{PHL}	Propagation Delay Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Sum	4.0 4.0	8.0 7.8	10.5 10.0	3.5 4.0	16.5 13.5	4.0 4.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation Delay Any $\overline{A}$ or $\overline{B}$ to Any $\overline{F}$	Dif	4.5 3.5	9.4 9.4	12.0 12.0	3.5 3.0	17.5 14.0	4.5 3.5	13.0 13.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to $\overline{F}$	Logic	4.0 4.0	6.0 6.0	9.0 10.0	3.5 3.0	14.5 15.5	4.0 4.0	10.0 11.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{A}$ or $\overline{B}$ to A = B	Dif	11.0 6.0	18.5 9.8	27.0 12.5	8.0 5.5	35.0 21.0	11.0 6.0	29.0 13.5	ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:
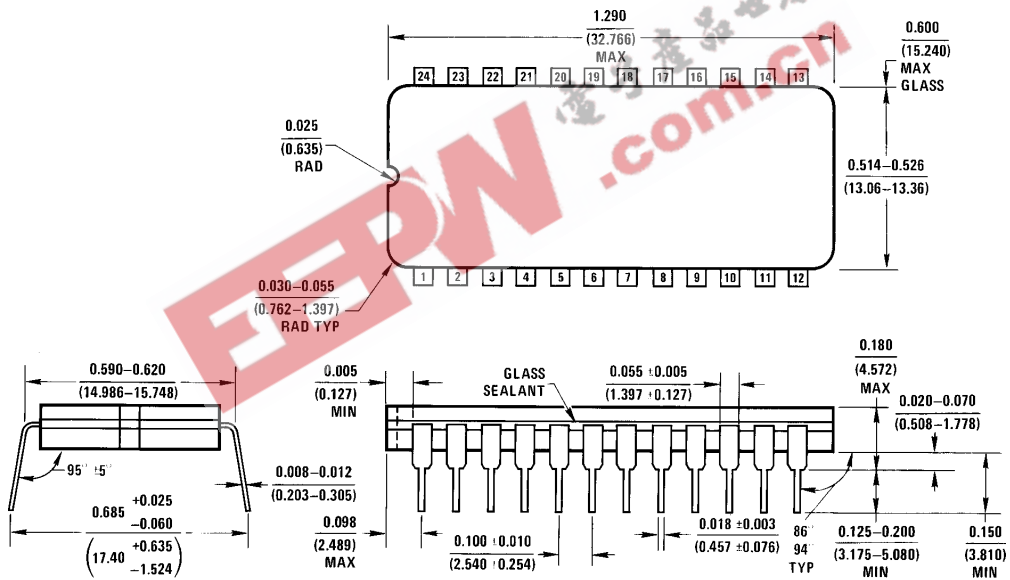
74F   181   P   C

Temperature Range Family
74F = Commercial
54F = Military

Device Type

Package Code
P = Plastic DIP
SP = Slim Plastic DIP
D = Ceramic DIP
SD = Slim Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier (LCC)
S = Small Outline SOIC JEDEC

Special Variations
QB = Military grade device with environmental and burn-in processing

Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)
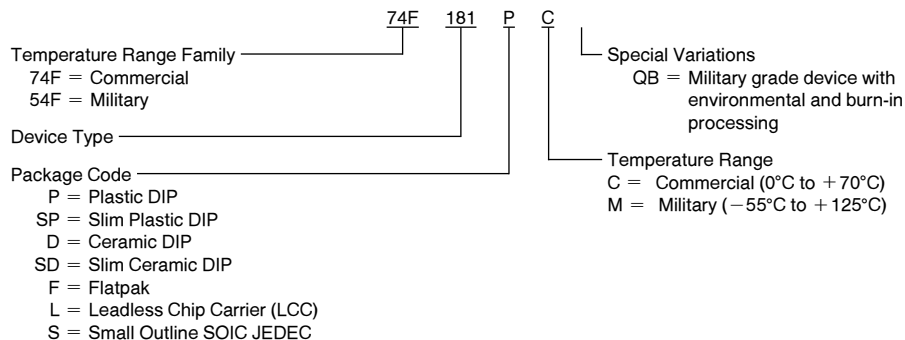
Physical Dimensions inches (millimeters)
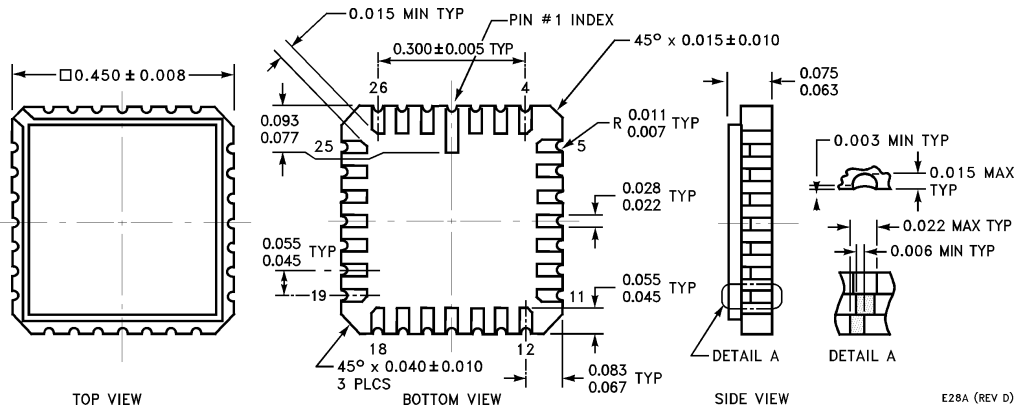
28-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E28A

0.015 MIN TYP

PIN #1 INDEX

45° x 0.015 ± 0.010

□ 0.450 ± 0.008

0.300 ± 0.005 TYP

26   4

25   5

R 0.011 / 0.007 TYP

0.093 / 0.077

0.028 / 0.022 TYP

0.055 / 0.045 TYP

0.055 / 0.045 TYP

19   11

18   12

45° x 0.040 ± 0.010
3 PLCS

0.083 / 0.067 TYP

0.075 / 0.063

0.003 MIN TYP

0.015 MAX TYP

0.022 MAX TYP

0.006 MIN TYP

TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

DETAIL A

E28A (REV D)

24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24A

1.290
(32.766)
MAX

0.600
(15.240)
MAX
GLASS

24 23 22 21 20 19 18 17 16 15 14 13

1 2 3 4 5 6 7 8 9 10 11 12

0.025
(0.635)
RAD

0.514–0.526
(13.06–13.36)

0.030–0.055
(0.762–1.397)
RAD TYP

0.590–0.620
(14.986–15.748)

0.005
(0.127)
MIN

GLASS
SEALANT

0.055 ±0.005
(1.397 ±0.127)

0.180
(4.572)
MAX

0.020–0.070
(0.508–1.778)

95° ±5°

0.685
+0.025
−0.060
(17.40
+0.635
−1.524
)

0.008–0.012
(0.203–0.305)

0.098
(2.489)
MAX

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

86°
94°
TYP

0.125–0.200
(3.175–5.080)
MIN

0.150
(3.810)
MIN

J24A (REV H)

7

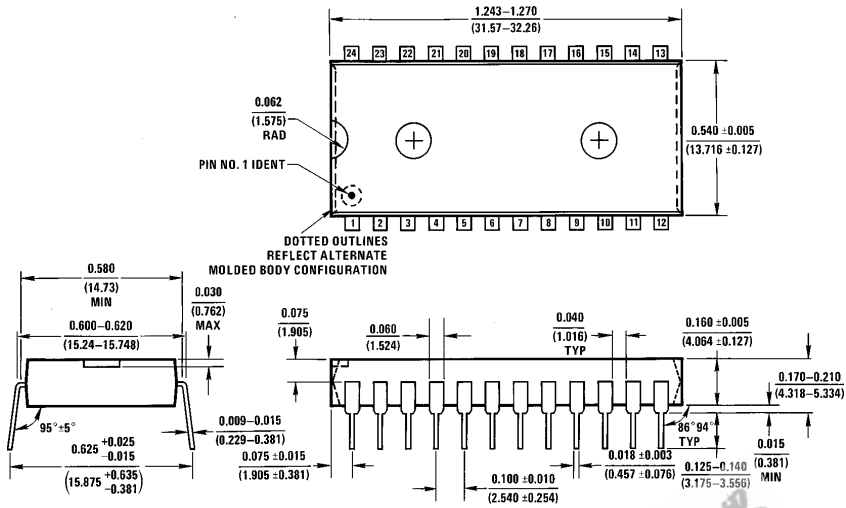## Physical Dimensions inches (millimeters) (Continued)
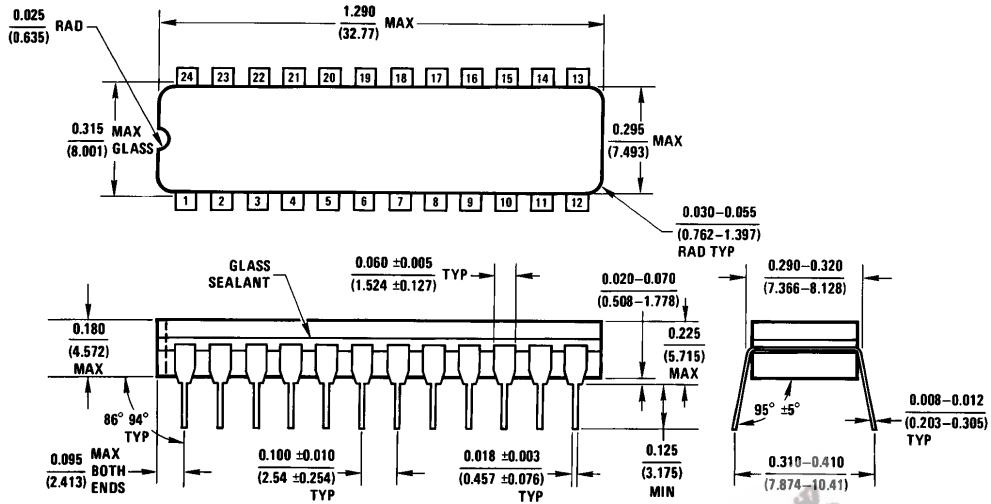
24-Lead (0.300″ Wide) Ceramic Dual-In-Line Package (SD)
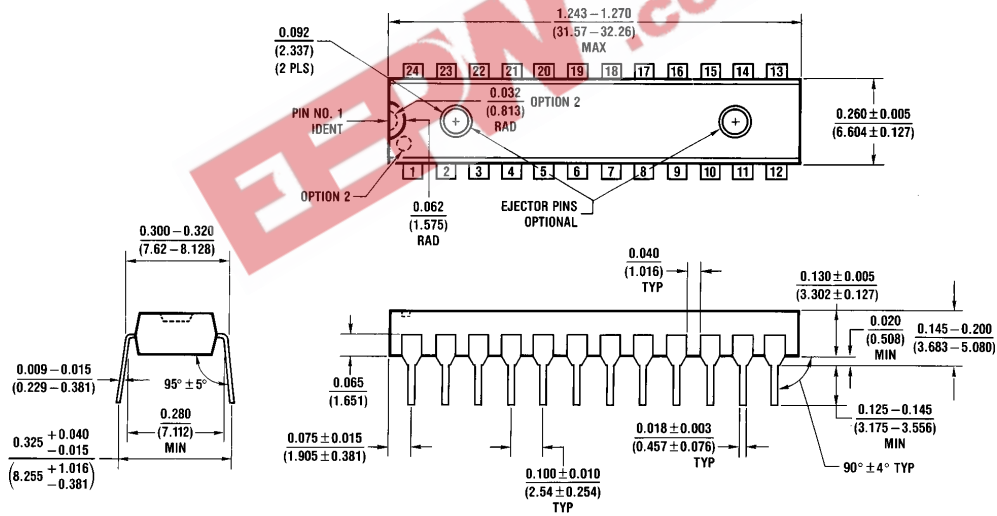**NS Package Number J24F**

J24F(REV G)
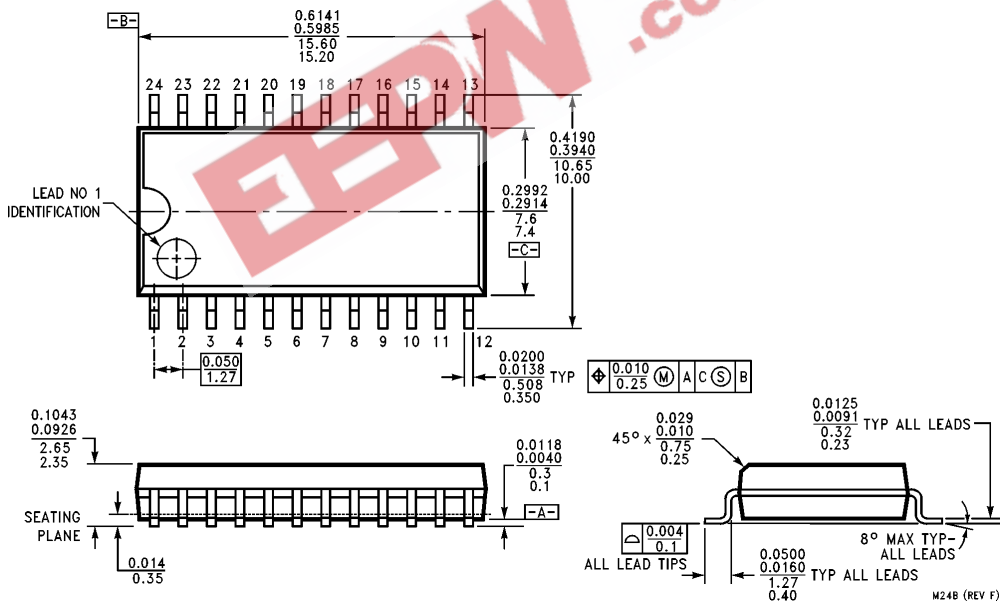
24-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B

M24B (REV F)

Physical Dimensions inches (millimeters) (Continued)

1.243–1.270
(31.57–32.26)

0.062
(1.575)
RAD

PIN NO. 1 IDENT

0.540 ±0.005
(13.716 ±0.127)

DOTTED OUTLINES
REFLECT ALTERNATE
MOLDED BODY CONFIGURATION

0.580
(14.73)
MIN

0.600–0.620
(15.24–15.748)

0.030
(0.762)
MAX

0.075
(1.905)

0.060
(1.524)

0.040
(1.016)
TYP

0.160 ±0.005
(4.064 ±0.127)

0.170–0.210
(4.318–5.334)

95° ±5°

0.625 +0.025 −0.015
(15.875 +0.635 −0.381)

0.009–0.015
(0.229–0.381)

0.075 ±0.015
(1.905 ±0.381)

0.100 ±0.010
(2.540 ±0.254)

0.018 ±0.003
(0.457 ±0.076)

86°94°
TYP

0.125–0.140
(3.175–3.556)

0.015
(0.381)
MIN

N24A (REV E)

24-Lead (0.600″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N24A

1.243 – 1.270
(31.57 – 32.26)
MAX

0.092
(2.337)
(2 PLS)

0.032
(0.813)
RAD
OPTION 2

PIN NO. 1
IDENT

OPTION 2

0.062
(1.575)
RAD

EJECTOR PINS
OPTIONAL

0.260 ± 0.005
(6.604 ± 0.127)

0.300 – 0.320
(7.62 – 8.128)

0.040
(1.016)
TYP

0.130 ± 0.005
(3.302 ± 0.127)

0.020
(0.508)
MIN

0.145 – 0.200
(3.683 – 5.080)

0.009 – 0.015
(0.229 – 0.381)

95° ± 5°

0.280
(7.112)
MIN

0.065
(1.651)

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.075 ± 0.015
(1.905 ± 0.381)

0.100 ± 0.010
(2.54 ± 0.254)
TYP

0.018 ± 0.003
(0.457 ± 0.076)
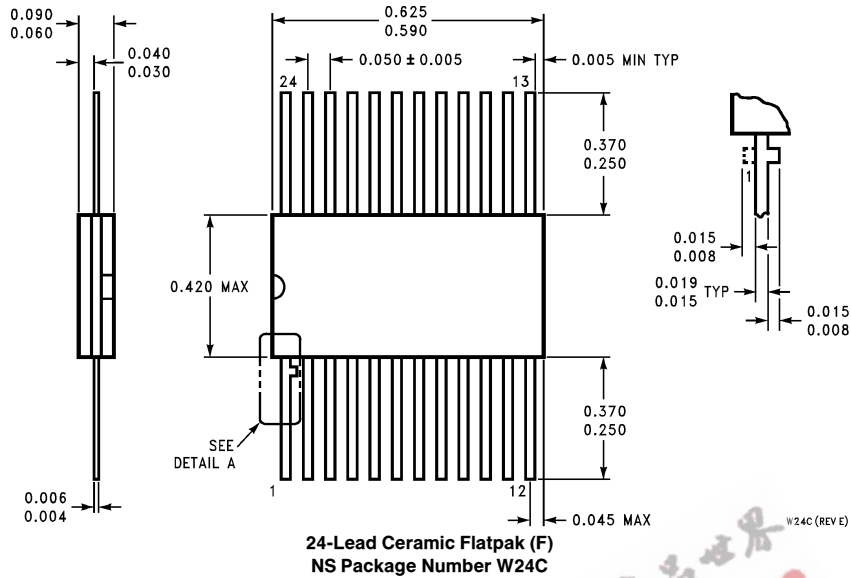TYP

0.125 – 0.145
(3.175 – 3.556)
MIN

90° ± 4° TYP

N24C (REV F)

24-Lead (0.300″ Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)

0.090
0.060

0.040
0.030

0.625
0.590

0.050 ± 0.005

0.005 MIN TYP

24   13

0.370
0.250

0.420 MAX

0.015
0.008

0.019
0.015 TYP

0.015
0.008

0.370
0.250

SEE
DETAIL A

1   12

0.006
0.004

0.045 MAX

W24C (REV E)

24-Lead Ceramic Flatpak (F)
NS Package Number W24C

LIFE SUPPORT POLICY

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.