

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT4515

4-to-16 line decoder/demultiplexer
with input latches; inverting

Product specification
File under Integrated Circuits, IC06

September 1993

4-to-16 line decoder/demultiplexer with input latches; inverting

74HC/HCT4515

FEATURES

- Inverting outputs
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4515 are high-speed Si-gate CMOS devices and are pin compatible with "4515" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4515 are 4-to-16 line decoders/demultiplexers having four binary weighted address inputs (A_0 to A_3) with latches, a latch enable input (LE), and an active LOW enable input ($\bar{E}$). The 16 inverting outputs ($\bar{Q}_0$ to $\bar{Q}_{15}$) are mutually exclusive active LOW. When LE is HIGH, the selected output is determined by the data on A_n . When LE goes LOW, the last data present at A_n are stored in the latches and the outputs remain stable. When $\bar{E}$ is LOW, the selected output, determined by the contents of the latch, is LOW. When $\bar{E}$ is HIGH, all outputs are HIGH. The enable input ($\bar{E}$) does not affect the state of the latch.

When the "4515" is used as a demultiplexer, $\bar{E}$ is the data input and A_0 to A_3 are the address inputs.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to $\bar{Q}_n$	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	25	26	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	LE	latch enable input (active HIGH)
2, 3, 21, 22	A ₀ to A ₃	address inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	$\overline{Q}_0$ to $\overline{Q}_{15}$	multiplexer outputs (active LOW)
12	GND	ground (0 V)
23	$\overline{E}$	enable input (active LOW)
24	V _{CC}	positive supply voltage

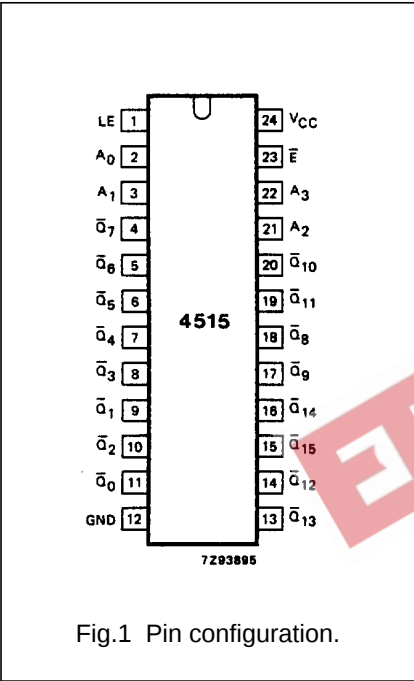


Fig.1 Pin configuration.

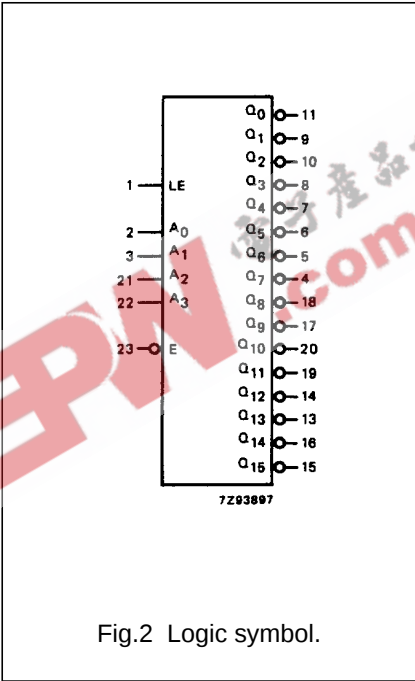


Fig.2 Logic symbol.

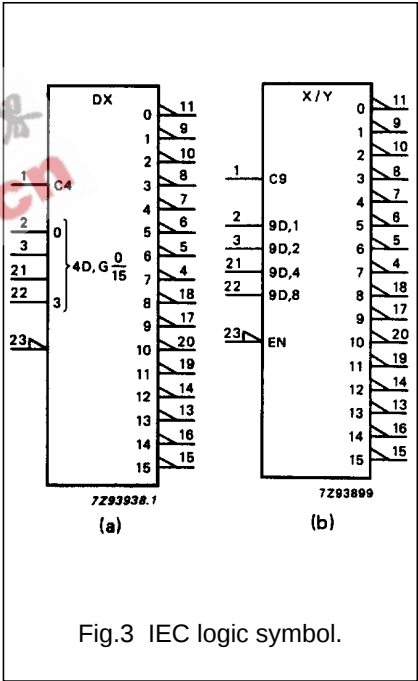
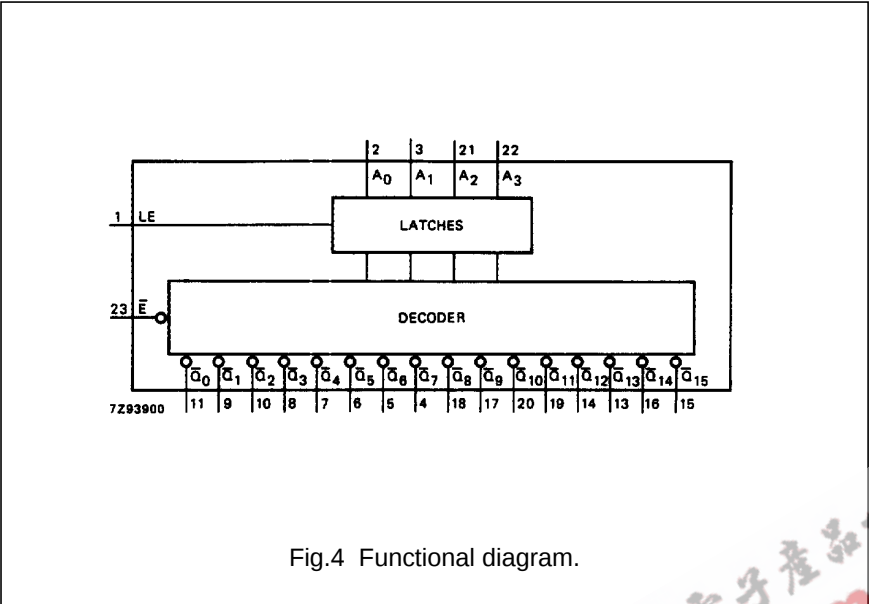


Fig.3 IEC logic symbol.

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APPLICATIONS

- Digital multiplexing
- Address decoding
- Hexadecimal/BCD decoding

FUNCTION TABLE

INPUTS					OUTPUTS															
$\bar{E}$	A ₀	A ₁	A ₂	A ₃	$\bar{Q}_0$	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$	$\bar{Q}_5$	$\bar{Q}_6$	$\bar{Q}_7$	$\bar{Q}_8$	$\bar{Q}_9$	$\bar{Q}_{10}$	$\bar{Q}_{11}$	$\bar{Q}_{12}$	$\bar{Q}_{13}$	$\bar{Q}_{14}$	$\bar{Q}_{15}$
H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

Notes

1. LE = HIGH
H = HIGH voltage level
L = LOW voltage level
X = don't care

4-to-16 line decoder/demultiplexer with
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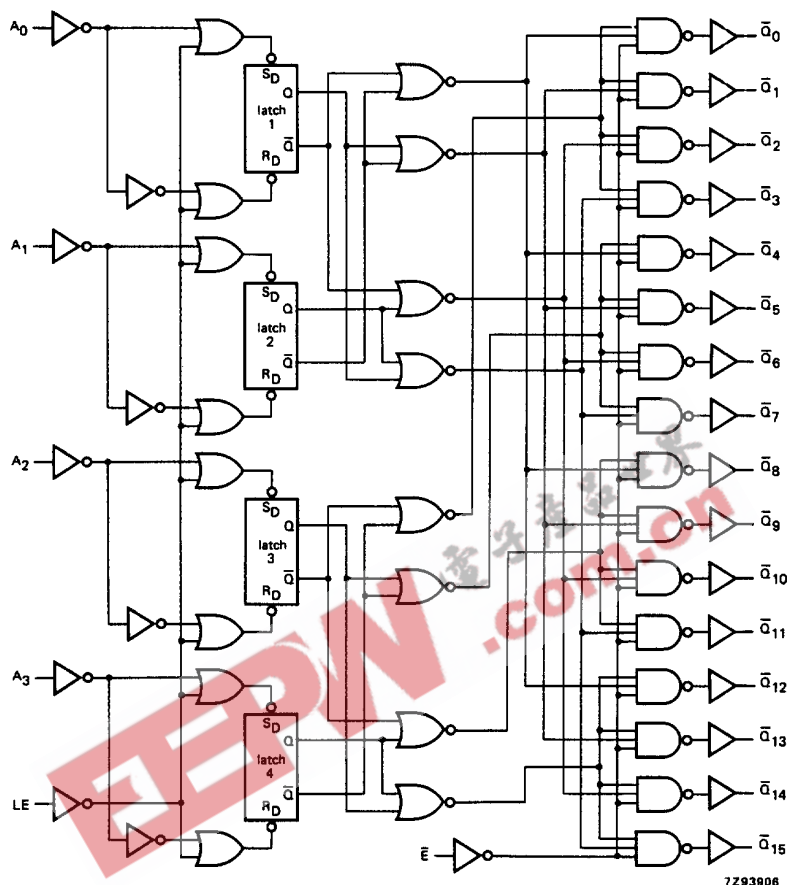


Fig.5 Logic diagram.

4-to-16 line decoder/demultiplexer with input latches; inverting

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to Q _n		80 29 23	250 50 43		315 63 54		375 75 64	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay LE to Q _n		66 24 19	225 45 38		280 56 48		340 68 58	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay E to Q _n		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t _w	latch enable pulse width HIGH	75 15 13	14 5 4		95 19 16		110 22 19		ns	2.0 4.5 6.0	Fig.7
t _{su}	set-up time A _n to LE	90 18 15	28 10 8		115 23 20		135 27 23		ns	2.0 4.5 6.0	Fig.7
t _h	hold time A _n to LE	0 0 0	−11 −4 −3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.7

4-to-16 line decoder/demultiplexer with input latches; inverting

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	0.65
LE	1.40
$\bar{E}$	1.00

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to Q _n		30	55		69		83	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay LE to Q _n		29	50		63		75	ns	4.5	Fig.6
t _{PHL} / t _{PLH}	propagation delay E ₁ to Q _n		18	40		50		60	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6
t _W	latch enable pulse width HIGH	16	3		20		24		ns	4.5	Fig.7
t _{su}	set-up time A _n to LE	18	9		23		27		ns	4.5	Fig.7
t _h	hold time A _n to LE	3	−2		3		3		ns	4.5	Fig.7

4-to-16 line decoder/demultiplexer with input latches; inverting

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AC WAVEFORMS

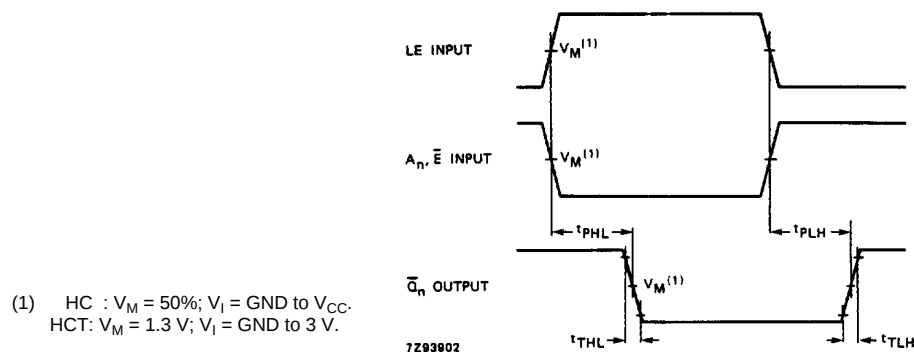


Fig.6 Waveforms showing the input (A_n , LE , $\bar{E}$) to output ($\bar{Q}_n$) propagation delays and the output transition times.

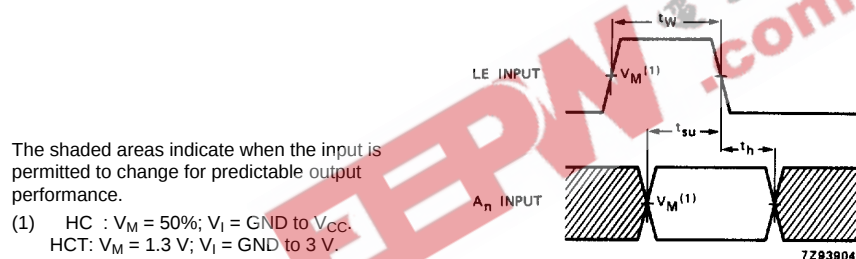


Fig.7 Waveforms showing the minimum pulse width of the latch enable input (LE) and the set-up and hold times for LE to A_n . Set-up and hold times are shown as positive values but may be specified as negative values.

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".