

## 54F/74F169 4-Stage Synchronous Bidirectional Counter

### General Description

The 'F169 is a fully synchronous 4-stage up/down counter. The 'F169 is a modulo-16 binary counter. Features a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

### Features

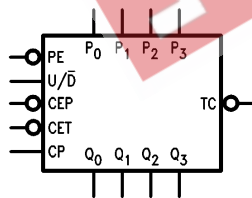
- Asynchronous counting and loading
- Built-in lookahead carry capability
- Presettable for programmable operation

Commercial	Military	Package Number	Package Description
74F169PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F169DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F169SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F169SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ

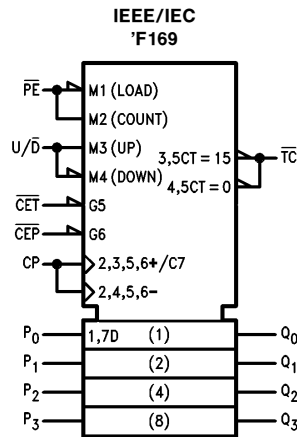
**Note 1:** Devices also available in 13" reel. Use suffix = SCX and SJX.

**Note 2:** Military grade device with environmental and burn-in processing. Use suffix = DMQB.

### Logic Symbols



TL/F/9488-3

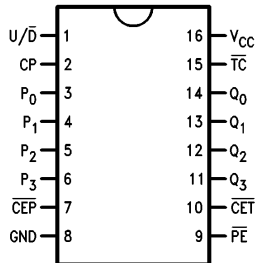


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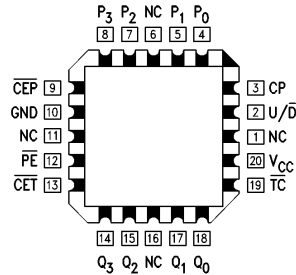
## Connection Diagrams

Pin Assignment for  
DIP, SOIC and Flatpak



TL/F/9488-1

Pin Assignment  
for LCC



TL/F/9488-2

## Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/2.0	20 $\mu$ A/ -1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$P_0-P_3$	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/ -0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ -0.6 mA
$U/\overline{D}$	Up-Down Count Control Input	1.0/1.0	20 $\mu$ A/ -0.6 mA
$Q_0-Q_3$	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	50/33.3	-1 mA/20 mA

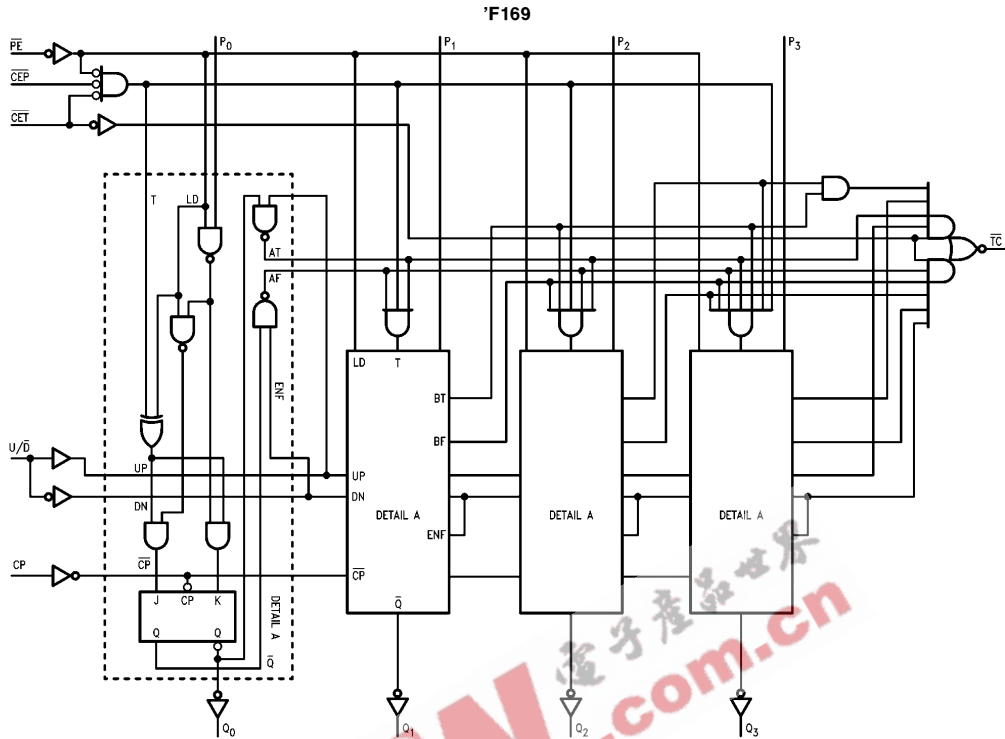
## Functional Description

The 'F169 uses edge-triggered J-K type flip-flops and has no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When  $\overline{PE}$  is LOW, the data on the  $P_0-P_3$  inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both  $\overline{CEP}$  and  $\overline{CET}$  must be LOW and  $\overline{PE}$  must be HIGH; the  $U/\overline{D}$  input then determines the direction of counting. The Terminal Count ( $\overline{TC}$ ) output is normally HIGH and goes LOW, provided that

$\overline{CET}$  is LOW, when a counter reaches zero in the Count Down mode or reaches 15 for the 'F169 in the Count Up mode. The  $\overline{TC}$  output state is not a function of the Count Enable Parallel ( $\overline{CEP}$ ) input level. Since the  $\overline{TC}$  signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on  $\overline{TC}$ . For this reason the use of  $\overline{TC}$  as a clock signal is not recommended (see logic equations below).

- 1) Count Enable =  $\overline{CEP} \cdot \overline{CET} \cdot \overline{PE}$
- 2) Up: ('F169):  $\overline{TC} = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot (Up) \cdot \overline{CET}$
- 3) Down:  $\overline{TC} = \overline{Q_0} \cdot \overline{Q_1} \cdot \overline{Q_2} \cdot \overline{Q_3} \cdot (Down) \cdot \overline{CET}$

## Logic Diagram



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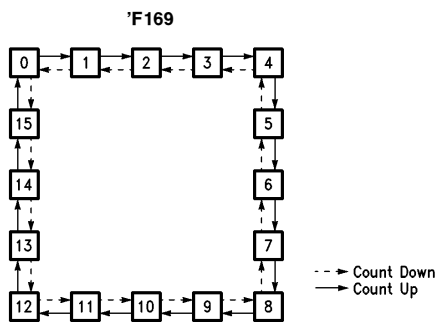
Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$U/\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ( $P_n \rightarrow Q_n$ )
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

## State Diagram



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## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE® Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		74F 10% V <sub>CC</sub>	2.5				I <sub>OH</sub> = -1 mA
		74F 5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub>		0.5	V	Min	I <sub>OL</sub> = 20 mA
		74F 10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current	54F		20.0	μA	Max	V <sub>IN</sub> = 2.7V
		74F		5.0			
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F		100	μA	Max	V <sub>IN</sub> = 7.0V
		74F		7.0			
I <sub>CEX</sub>	Output HIGH Leakage Current	54F		250	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
		74F		50			
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2	mA	Max	V <sub>IN</sub> = 0.5V (except $\overline{CET}$ ) V <sub>IN</sub> = 0.5V ( $\overline{CET}$ )
I <sub>OS</sub>	Output Short-Circuit Current		-60	-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CCL</sub>	Power Supply Current		35	52	mA	Max	V <sub>O</sub> = LOW

'F169

**AC Electrical Characteristics**

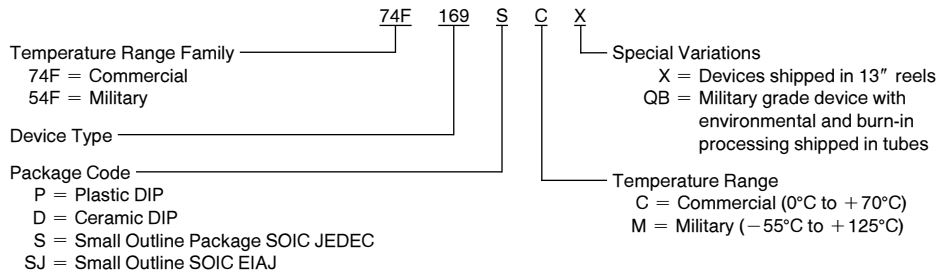
Symbol	Parameter	74F			54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Mil C <sub>L</sub> = 50 pF		T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	Maximum Count Frequency	90			60		70		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q <sub>n</sub> (PE HIGH or LOW)	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	12.0 16.0	3.0 4.0	9.5 13.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to $\overline{TC}$	5.5 4.0	12.0 8.5	15.5 12.5	5.5 4.0	20.0 15.0	5.5 4.0	17.5 13.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{CET}$ to $\overline{TC}$	2.5 2.5	4.5 8.5	6.5 11.0	2.5 2.5	9.0 12.0	2.5 2.5	7.0 12.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay U/ $\overline{D}$ to $\overline{TC}$	3.5 4.0	8.5 8.0	11.5 12.0	3.5 4.0	16.0 14.0	3.5 4.0	12.5 13.0	ns

**AC Operating Requirements**

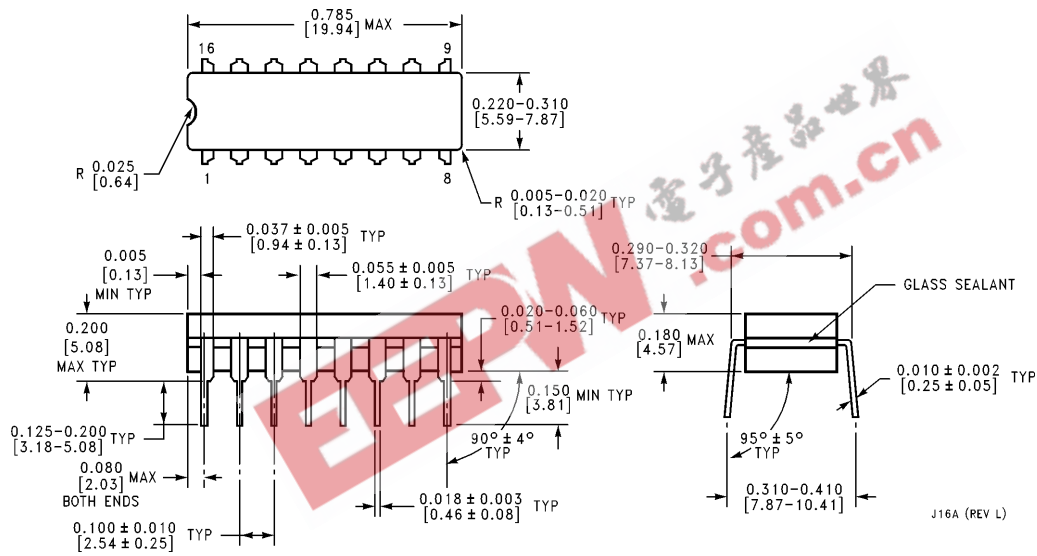
Symbol	Parameter	74F		54F		74F		Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V		T <sub>A</sub> , V <sub>CC</sub> = Mil		T <sub>A</sub> , V <sub>CC</sub> = Com		
		Min	Max	Min	Max	Min	Max	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW P <sub>n</sub> to CP	4.0 4.0		4.5 4.5		4.5 4.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW P <sub>n</sub> to CP	3.0 3.0		3.5 3.5		3.5 3.5		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	7.0 5.0		8.0 8.0		8.0 6.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	0 0.5		0 1.0		0 0.5		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW $\overline{PE}$ to CP	8.0 8.0		10.0 10.0		9.0 9.0		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW $\overline{PE}$ to CP	1.0 0		1.0 0		1.0 0		ns
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup Time, HIGH or LOW U/ $\overline{D}$ to CP	11.0 7.0		14.0 12.0		12.5 8.5		ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold Time, HIGH or LOW U/ $\overline{D}$ to CP	0 0		0 0		0 0		ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CP Pulse Width HIGH or LOW	4.0 7.0		6.0 9.0		4.5 8.0		ns

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

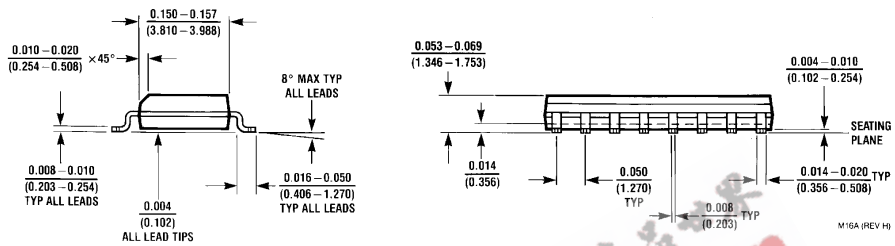
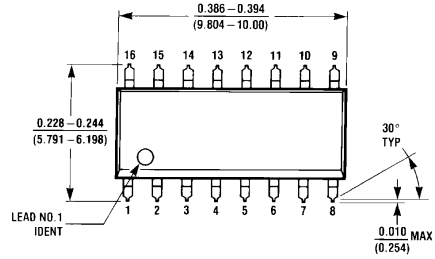


## Physical Dimensions inches (millimeters)

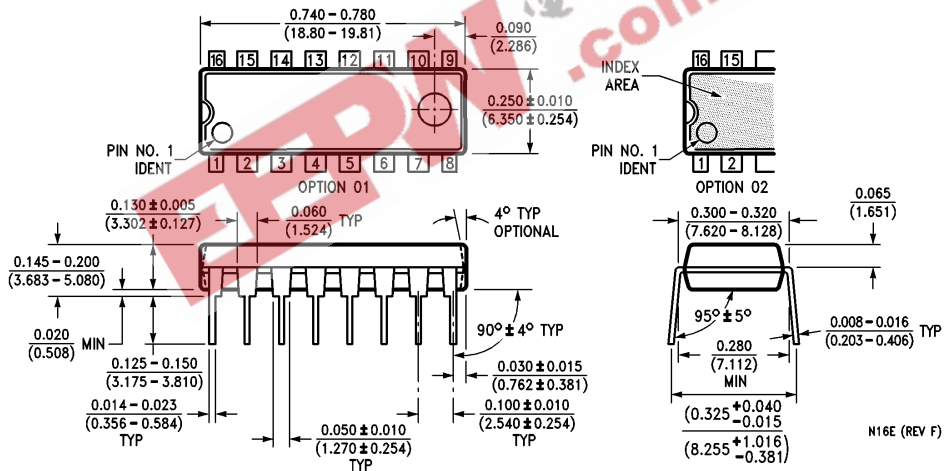


**16-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J16A

**Physical Dimensions** inches (millimeters) (Continued)

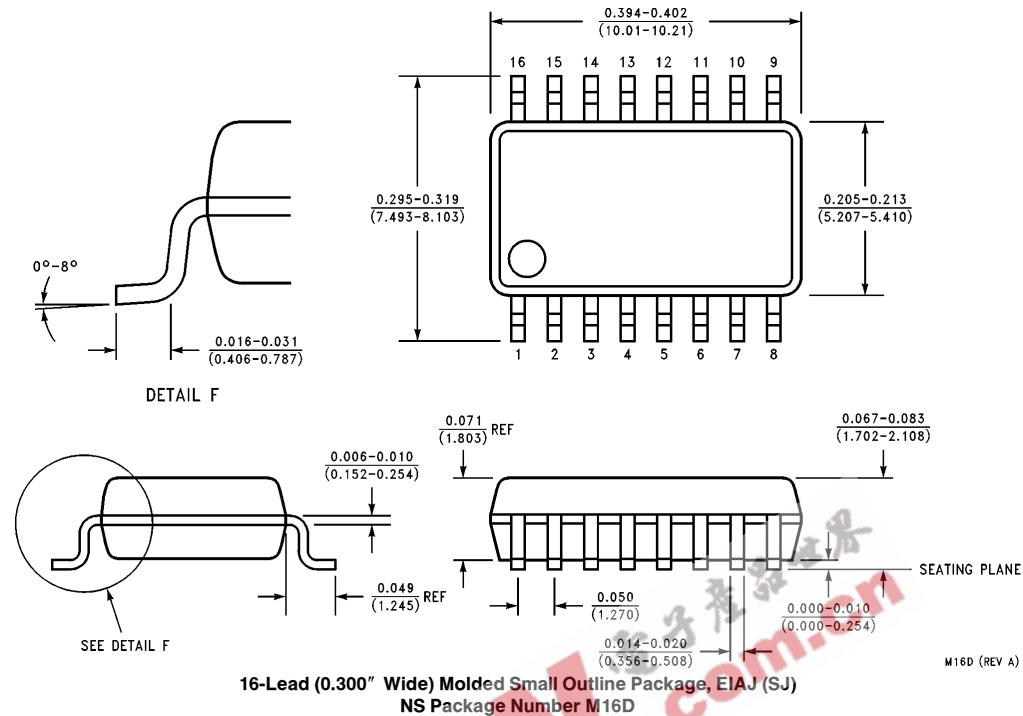


**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)**  
NS Package Number M16A



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)**  
NS Package Number N16E

**Physical Dimensions** inches (millimeters) (Continued)



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