National *Semiconductor*

November 1994

54F/74F283
4-Bit Binary Full Adder with Fast Carry

General Description

The 'F283 high-speed 4-bit binary full adder with internal carry lookahead accepts two 4-bit binary words (A_0–A_3, B_0–B_3) and a Carry input (C_0). It generates the binary Sum outputs (S_0–S_3) and the Carry output (C_4) from the most significant bit. The 'F283 will operate with either active HIGH or active LOW operands (positive or negative logic).

Features

■ Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F283PC		N16E	16-Lead (0.300″ Wide) Molded Dual-In-Line
	54F283DM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F283SC (Note 1)		M16A	16-Lead (0.150″ Wide) Molded Small Outline, JEDEC
74F283SJ (Note 1)		M16D	16-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F283FM (Note 2)	W16A	16-Lead Cerpack
	54F283LL (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

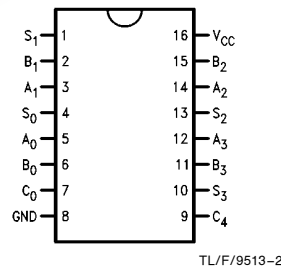**Note 1:** Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

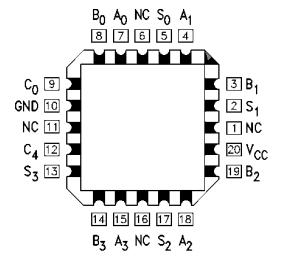

TL/F/9513–1

IEEE/IEC

TL/F/9513–4
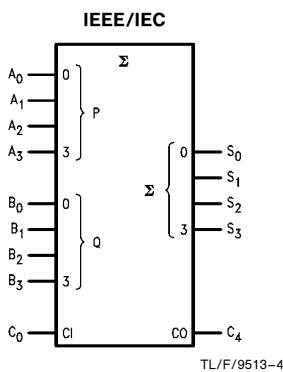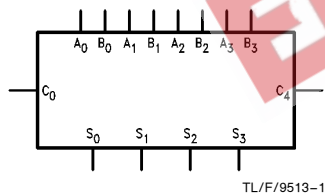
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak

TL/F/9513–2

Pin Assignment for LCC

TL/F/9513–3

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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0-A_3	A Operand Inputs	1.0/2.0	20 $\mu A/-1.2$ mA
B_0-B_3	B Operand Inputs	1.0/2.0	20 $\mu A/-1.2$ mA
C_0	Carry Input	1.0/1.0	20 $\mu A/-0.6$ mA
S_0-S_3	Sum Outputs	50/33.3	-1 mA/20 mA
C_4	Carry Output	50/33.3	-1 mA/20 mA

Functional Description

The 'F283 adds two 4-bit binary words (A plus B) plus the incoming Carry (C_0). The binary sum appears on the Sum (S_0-S_3) and outgoing carry (C_4) outputs. The binary weight of the various inputs and outputs is indicated by the subscript numbers, representing powers of two.

$$2^0 (A_0 + B_0 + C_0) + 2^1 (A_1 + B_1)$$
$$+ 2^2 (A_2 + B_2) + 2^3 (A_3 + B_3)$$
$$= S_0 + 2S_1 + 4S_2 + 8S_3 + 16C_4$$
$$\text{Where } (+) = \text{plus}$$

Interchanging inputs of equal weight does not affect the operation. Thus C_0, A_0, B_0 can be arbitrarily assigned to pins 5, 6 and 7 for DIPS, and 7, 8 and 9 for chip carrier packages. Due to the symmetry of the binary add function, the 'F283 can be used either with all inputs and outputs active HIGH (positive logic) or with all inputs and outputs active LOW (negative logic). See *Figure 1*. Note that if C_0 is not used it must be tied LOW for active HIGH logic or tied HIGH for active LOW logic.

Due to pin limitations, the intermediate carries of the 'F283 are not brought out for use as inputs or outputs. However, other means can be used to effectively insert a carry into, or bring a carry out from, an intermediate stage. *Figure 2* shows how to make a 3-bit adder. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes S_3 dependent only on, and equal to, the carry from the third adder. Using somewhat the same principle, *Figure 3* shows a way of dividing the 'F283 into a 2-bit and a 1-bit adder. The third stage adder (A_2, B_2, S_2) is used merely as a means of getting a carry (C_{10}) signal into the fourth stage (via A_2 and B_2) and bringing out the carry from the second stage on S_2. Note that as long as A_2 and B_2 are the same, whether HIGH or LOW, they do not influence S_2. Similarly, when A_2 and B_2 are the same the carry into the third stage does not influence the carry out of the third stage. *Figure 4* shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs S_0, S_1 and S_2 present a binary number equal to the number of inputs I_1-I_5 that are true. *Figure 5* shows one method of implementing a 5-input majority gate. When three or more of the inputs I_1-I_5 are true, the output M_5 is true.

	C_0	A_0	A_1	A_2	A_3	B_0	B_1	B_2	B_3	S_0	S_1	S_2	S_3	C_4
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

Active HIGH: $0 + 10 + 9 = 3 + 16$ Active LOW: $1 + 5 + 6 = 12 + 0$

FIGURE 1. Active HIGH versus Active LOW Interpretation

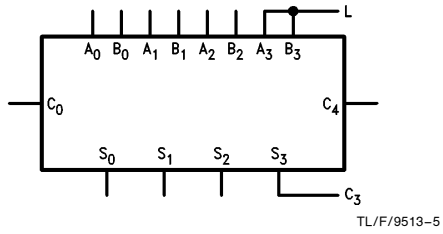2

Functional Description (Continued)

FIGURE 2. 3-Bit Adder
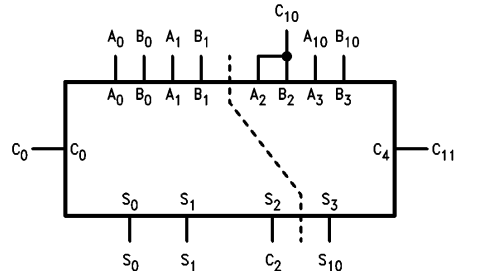
TL/F/9513-5

FIGURE 3. 2-Bit and 1-Bit Adders
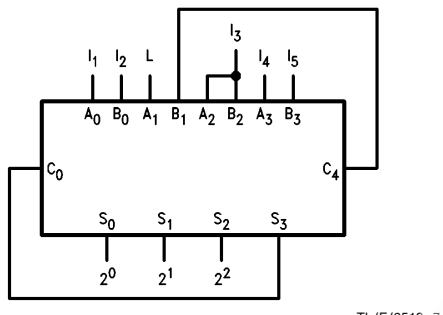
TL/F/9513-6

FIGURE 4. 5-Input Encoder
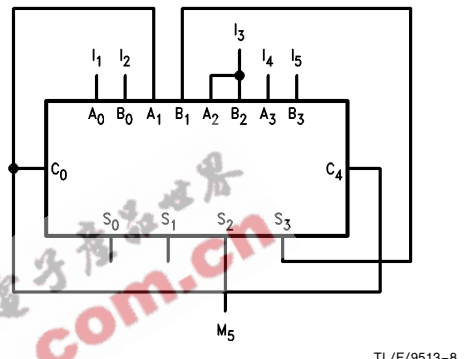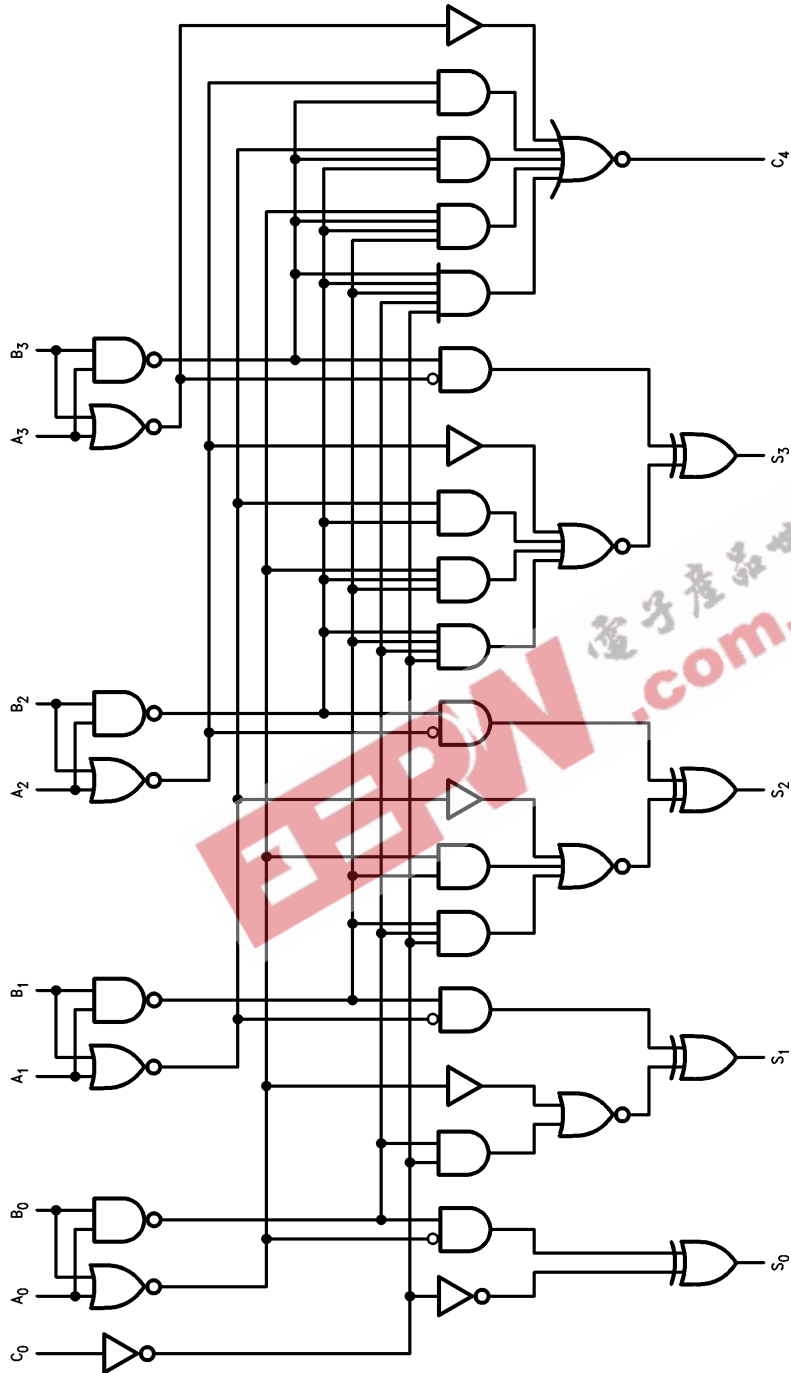
TL/F/9513-7

FIGURE 5. 5-Input Majority Gate

TL/F/9513-8

Logic Diagram

TL/F/9513–9

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	$-65°C$ to $+150°C$
Ambient Temperature under Bias	$-55°C$ to $+125°C$
Junction Temperature under Bias	$-55°C$ to $+175°C$
Plastic	$-55°C$ to $+150°C$
V_{CC} Pin Potential to Ground Pin	$-0.5V$ to $+7.0V$
Input Voltage (Note 2)	$-0.5V$ to $+7.0V$
Input Current (Note 2)	-30 mA to $+5.0$ mA
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)	
Standard Output	$-0.5V$ to V_{CC}
TRI-STATE® Output	$-0.5V$ to $+5.5V$
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	$-55°C$ to $+125°C$
Commercial	$0°C$ to $+70°C$
Supply Voltage	
Military	$+4.5V$ to $+5.5V$
Commercial	$+4.5V$ to $+5.5V$

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	$I_{OH} = -1$ mA
		74F 10% V_{CC}	2.5					$I_{OH} = -1$ mA
		74F 5% V_{CC}	2.7					$I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	$I_{OL} = 20$ mA
		74F 10% V_{CC}			0.5			$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	$V_{IN} = 2.7V$
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	$V_{IN} = 7.0V$
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	$V_{OUT} = V_{CC}$
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	$I_{ID} = 1.9$ μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$ (C_O)
					-1.2			$V_{IN} = 0.5V$ (A_n, B_n)
I_{OS}	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CCH}	Power Supply Current			36	55	mA	Max	$V_O = $ HIGH
I_{CCL}	Power Supply Current			36	55	mA	Max	$V_O = $ LOW

AC Electrical Characteristics

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\,pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\,pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\,pF$		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay C_0 to S_n	3.5 3.0	7.0 7.0	9.5 9.5	3.5 3.0	14.0 14.0	3.5 3.0	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to S_n	3.0 3.0	7.0 7.0	9.5 9.5	3.0 3.0	17.0 14.0	3.0 3.0	13.0 11.5	ns
t_{PLH} t_{PHL}	Propagation Delay C_0 to C_4	3.0 3.0	5.7 5.4	7.5 7.0	3.0 2.5	10.5 10.0	3.0 3.0	8.5 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay A_n or B_n to C_4	3.0 2.5	5.7 5.3	7.5 7.0	3.0 2.5	10.5 10.0	3.0 2.5	8.5 8.0	ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 283 S C X

Temperature Range Family
74F = Commercial
54F = Military

Device Type

Package Code
P = Plastic DIP
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier (LCC)
S = Small Outline SOIC JEDEC
SJ = Small Outline SOIC EIAJ

Special Variations
QB = Military grade device with environmental and burn-in processing
X = Devices shipped in 13″ reel

Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)

6

Physical Dimensions inches (millimeters)

0.350 ± 0.008
(8.890 ± 0.203)

0.063 − 0.075
(1.600 − 1.905)

DETAIL A

Top View

Side View

0.200 ± 0.005
(5.080 ± 0.127)
TYP

45° × 0.015 ± 0.010
(0.381 ± 0.254)

0.015
(0.381)
MIN TYP

0.007 − 0.011
(0.178 − 0.279)
R TYP

0.022 − 0.028
(0.559 − 0.711)
TYP

0.077 − 0.093
(1.959 − 2.362)

PIN #1
INDEX

0.045 − 0.055
(1.143 − 1.397)
TYP

0.067 − 0.083
(1.702 − 2.108)
TYP

0.045 − 0.055
(1.143 − 1.397)
TYP

45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS

Bottom View

0.003
(0.076)
MIN TYP

0.015
(0.381)
MAX TYP

0.022
(0.559)
MAX TYP

0.006
(0.152)
MIN TYP

Detail A

E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

0.785
[19.94] MAX

16   9

0.220−0.310
[5.59−7.87]

R 0.025
[0.64]

1   8

R 0.005−0.020 TYP
[0.13−0.51]

0.037 ± 0.005
[0.94 ± 0.13] TYP

0.005
[0.13]
MIN TYP

0.055 ± 0.005
[1.40 ± 0.13] TYP

0.200
[5.08]
MAX TYP

0.020−0.060 TYP
[0.51−1.52]

0.290−0.320
[7.37−8.13]

GLASS SEALANT

0.180
[4.57] MAX

0.150 MIN TYP
[3.81]

0.010 ± 0.002 TYP
[0.25 ± 0.05]

0.125−0.200 TYP
[3.18−5.08]

90° ± 4°
TYP

95° ± 5°
TYP

0.080 MAX
[2.03]
BOTH ENDS

0.018 ± 0.003 TYP
[0.46 ± 0.08]
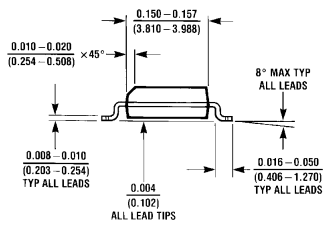
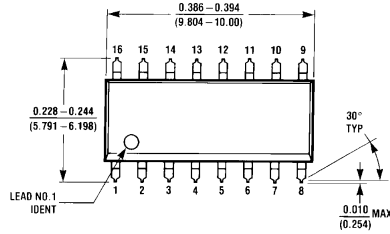0.310−0.410
[7.87−10.41]

J16A (REV L)

0.100 ± 0.010 TYP
[2.54 ± 0.25]
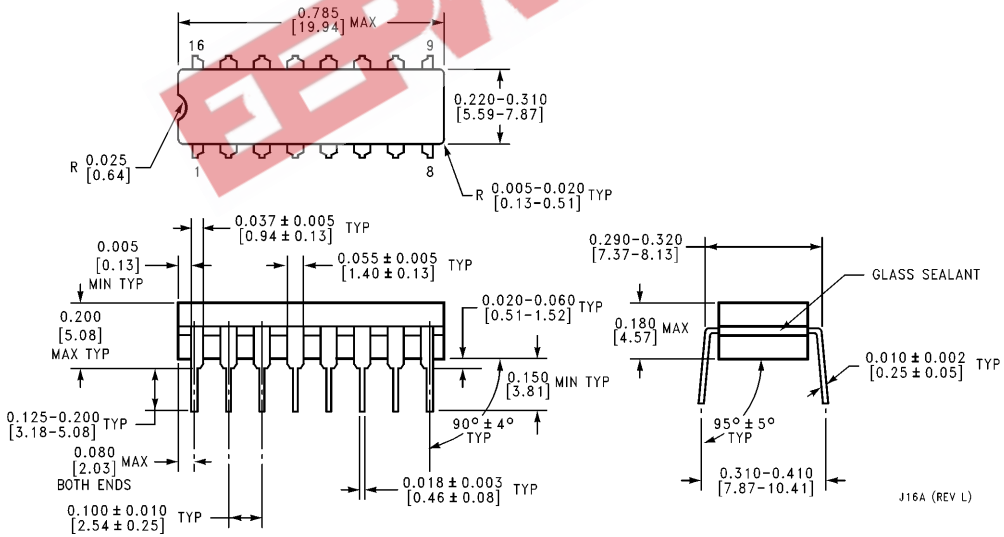
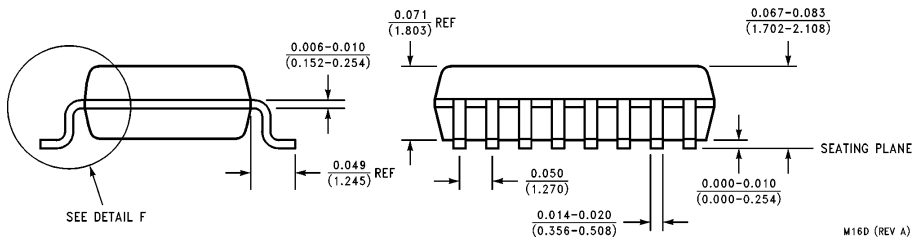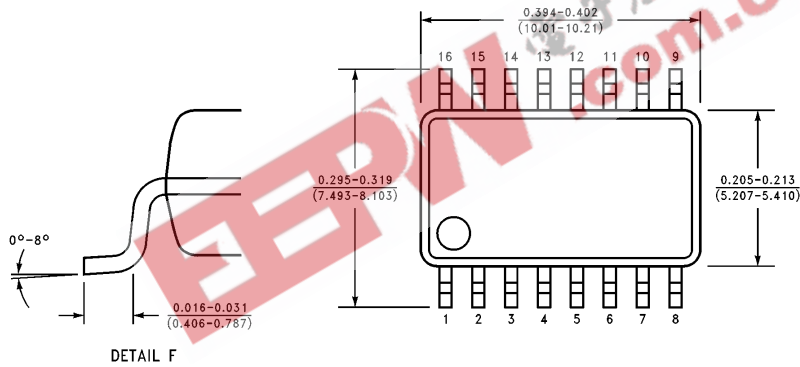**16-Lead Ceramic Dual-In-Line Package (D)**
NS Package Number J16A
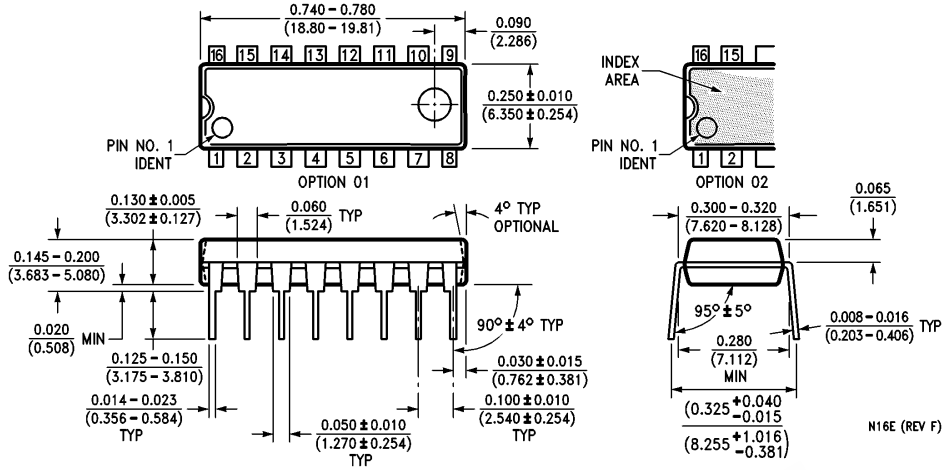
7

Physical Dimensions inches (millimeters) (Continued)

0.386 − 0.394
(9.804 − 10.00)

16 15 14 13 12 11 10 9

0.228 − 0.244
(5.791 − 6.198)

30°
TYP

LEAD NO.1
IDENT

1 2 3 4 5 6 7 8

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) × 45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020
(0.356 − 0.508) TYP

M16A (REV H)
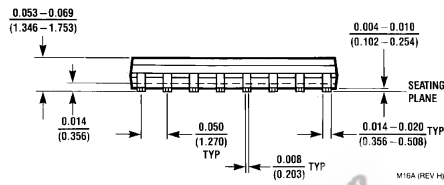
16-Lead (0.150″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

0.394 − 0.402
(10.01 − 10.21)

16 15 14 13 12 11 10 9

0.295 − 0.319
(7.493 − 8.103)

0.205 − 0.213
(5.207 − 5.410)

0° − 8°

0.016 − 0.031
(0.406 − 0.787)

DETAIL F

1 2 3 4 5 6 7 8

0.071
(1.803) REF

0.067 − 0.083
(1.702 − 2.108)

0.006 − 0.010
(0.152 − 0.254)

0.049
(1.245) REF

SEE DETAIL F

0.050
(1.270)

0.014 − 0.020
(0.356 − 0.508)

0.000 − 0.010
(0.000 − 0.254)

SEATING PLANE

M16D (REV A)

16-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

0.740 − 0.780
(18.80 − 19.81)

0.090
(2.286)

INDEX
AREA

16 15 14 13 12 11 10 9

0.250 ± 0.010
(6.350 ± 0.254)

16 15

PIN NO. 1
IDENT

1 2 3 4 5 6 7 8

OPTION 01

PIN NO. 1
IDENT

1 2

OPTION 02

0.065
(1.651)

0.130 ± 0.005
(3.302 ± 0.127)

0.060
(1.524) TYP

4° TYP
OPTIONAL

0.300 − 0.320
(7.620 − 8.128)

0.145 − 0.200
(3.683 − 5.080)

95° ± 5°

0.008 − 0.016
(0.203 − 0.406) TYP

90° ± 4° TYP

0.020
(0.508) MIN

0.125 − 0.150
(3.175 − 3.810)

0.030 ± 0.015
(0.762 ± 0.381)

0.280
(7.112)
MIN

0.014 − 0.023
(0.356 − 0.584)
TYP

0.050 ± 0.010
(1.270 ± 0.254)
TYP

0.100 ± 0.010
(2.540 ± 0.254)
TYP

$(0.325 {+0.040 \atop -0.015})$

$(8.255 {+1.016 \atop -0.381})$

N16E (REV F)

16-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

Physical Dimensions inches (millimeters) (Continued)

$0.050 - 0.080$
$(1.270 - 2.032)$

$\dfrac{0.004 - 0.006}{(0.102 - 0.152)}$ TYP

$\dfrac{0.371 - 0.390}{(9.423 - 9.906)}$

$\dfrac{0.007 - 0.018}{(0.178 - 0.457)}$ TYP

$\dfrac{0.050 \pm 0.005}{(1.270 \pm 0.127)}$ TYP

0.000 MIN TYP

$0.250 - 0.370$
$(6.350 - 9.398)$

16 15 14 13 12 11 10 9

$\dfrac{0.300}{(7.620)}$ MAX GLASS

$0.245 - 0.275$
$(6.223 - 6.985)$

DETAIL A →

2 3 4 5 6 7 8

PIN NO. 1 IDENT

$0.250 - 0.370$
$(6.350 - 9.398)$

1

$0.008 - 0.012$
$(0.203 - 0.305)$

DETAIL A

$\dfrac{0.026 - 0.040}{(0.660 - 1.016)}$ TYP

$\dfrac{0.015 - 0.019}{(0.381 - 0.482)}$ TYP

W16A (REV H)
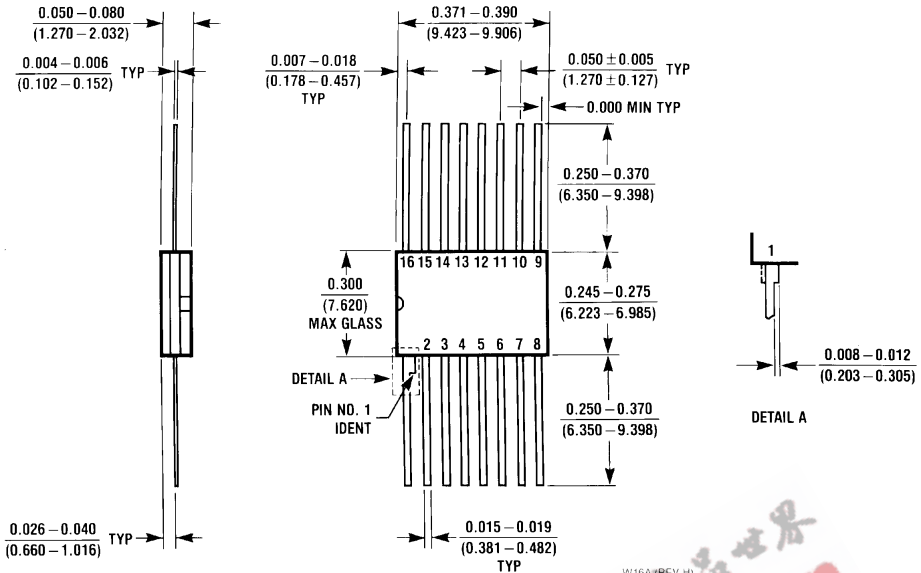
16-Lead Ceramic Flatpak (F)
NS Package Number W16A
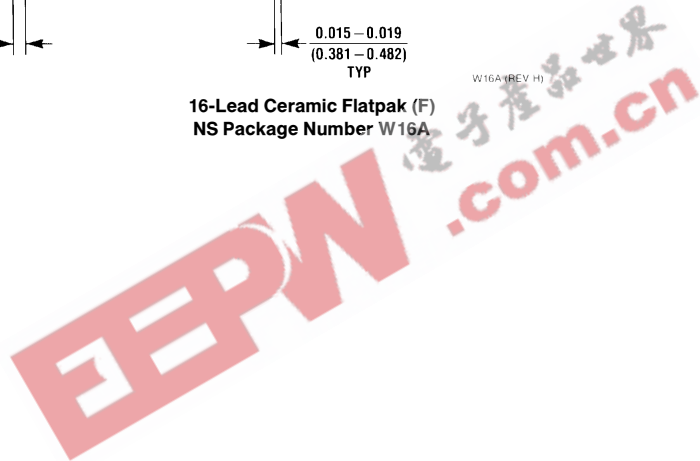
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.