

## 74F194 4-Bit Bidirectional Universal Shift Register

### General Description

The 74F194 is a high-speed 4-bit bidirectional universal shift register. As a high-speed, multifunctional, sequential building block, it is useful in a wide variety of applications. It may be used in serial-serial, shift left, shift right, serial-parallel, parallel-serial, and parallel-parallel data register transfers.

### Features

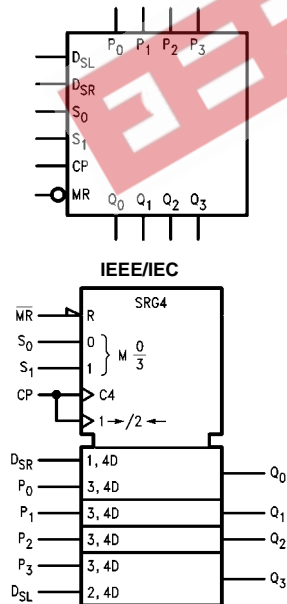
- Typical shift frequency of 150 MHz
- Asynchronous master reset
- Hold (do nothing) mode
- Fully synchronous serial or parallel data transfers

### Ordering Code:

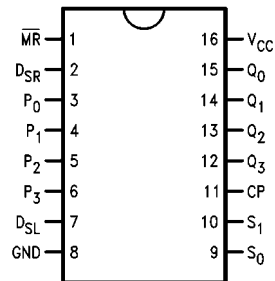
Order Number	Package Number	Package Description
74F194SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F194SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F194PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$S_0, S_1$	Mode Control Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$P_0-P_3$	Parallel Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$D_{SR}$	Serial Data Input (Shift Right)	1.0/1.0	20 $\mu$ A/-0.6 mA
$D_{SL}$	Serial Data Input (Shift Left)	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$Q_0-Q_3$	Parallel Outputs	50/33.3	-1 mA/20 mA

### Functional Description

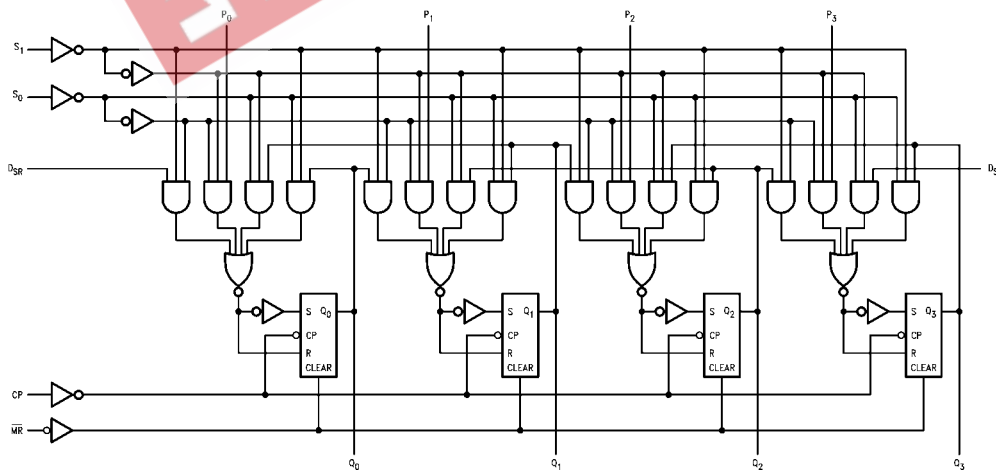
The 74F194 contains four edge-triggered D-type flip-flops and the necessary interstage logic to synchronously perform shift right, shift left, parallel load and hold operations. Signals applied to the Select ( $S_0, S_1$ ) inputs determine the type of operation, as shown in the Mode Select Table. Signals on the Select, Parallel data ( $P_0-P_3$ ) and Serial data ( $D_{SR}, D_{SL}$ ) inputs can change when the clock is in either state, provided only that the recommended setup and hold times, with respect to the clock rising edge, are observed. A LOW signal on Master Reset ( $\overline{MR}$ ) overrides all other inputs and forces the outputs LOW.

### Mode Select Table

Operating Mode	Inputs						Outputs			
	$\overline{MR}$	$S_1$	$S_0$	$D_{SR}$	$D_{SL}$	$P_n$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
Reset	L	X	X	X	X	X	L	L	L	L
Hold	H	l	l	X	X	X	$q_0$	$q_1$	$q_2$	$q_3$
Shift Left	H	h	l	X	l	X	$q_1$	$q_2$	$q_3$	L
	H	h	l	X	h	X	$q_1$	$q_2$	$q_3$	H
Shift Right	H	l	h	l	X	X	L	$q_0$	$q_1$	$q_2$
	H	l	h	h	X	X	H	$q_0$	$q_1$	$q_2$
Parallel Load	H	h	h	X	X	$p_n$	$p_0$	$p_1$	$p_2$	$p_3$

H (h) = HIGH Voltage Level  
 L (l) = LOW Voltage Level  
 $p_n$  ( $q_n$ ) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.  
 X = Immaterial

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

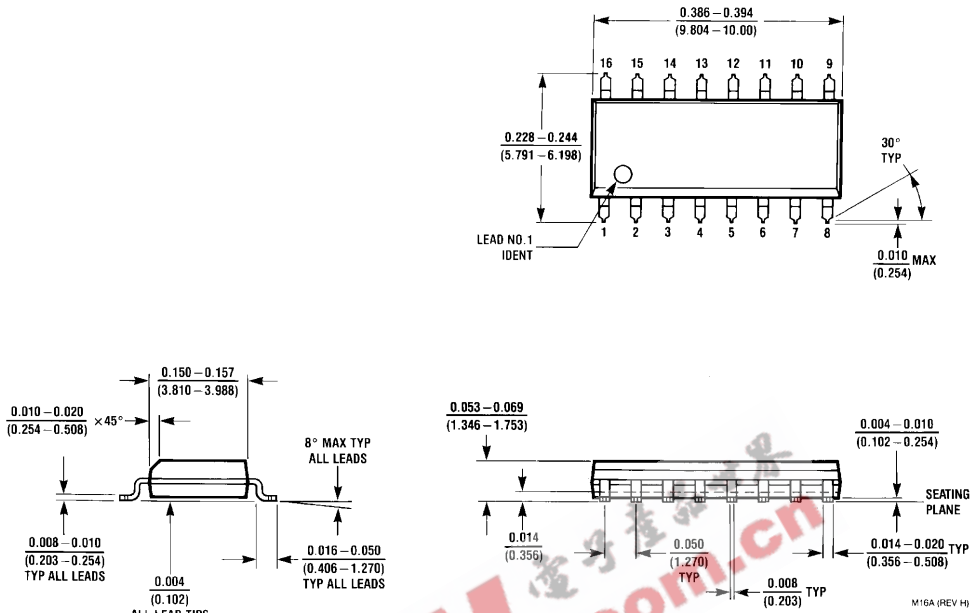
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>		0.5			I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		33	46	mA	Max	

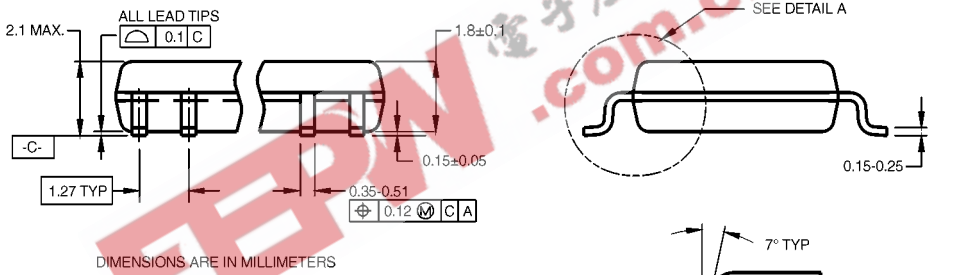
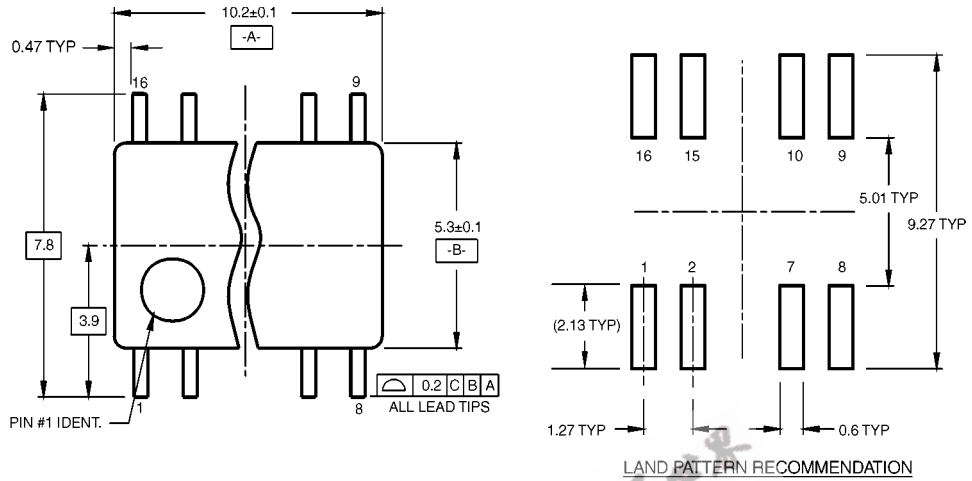
AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
$f_{MAX}$	Maximum Shift Frequency	105	150		90		90		MHz
$t_{PLH}$	Propagation Delay	3.5	5.2	7.0	3.0	8.5	3.5	8.0	ns
$t_{PHL}$	CP to $Q_n$	3.5	5.5	7.0	3.0	8.5	3.5	8.0	
$t_{PHL}$	Propagation Delay $\overline{MR}$ to $Q_n$	4.5	8.6	12.0	4.5	14.5	4.5	14.0	ns
AC Operating Requirements									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		Units	
		Min	Max	Min	Max	Min	Max		
$t_S(H)$	Setup Time, HIGH or LOW	4.0		6.0		4.0		ns	
$t_S(L)$	$P_n$ or $D_{SR}$ or $D_{SL}$ to CP	4.0		4.0		4.0			
$t_H(H)$	Hold Time, HIGH or LOW	1.0		1.5		1.0		ns	
$t_H(L)$	$P_n$ or $D_{SR}$ or $D_{SL}$ to CP	0		1.0		1.0			
$t_S(H)$	Setup Time, HIGH or LOW	10.0		10.5		11.0		ns	
$t_S(L)$	$S_n$ to CP	8.0		8.0		8.0			
$t_H(H)$	Hold Time, HIGH or LOW	0		0		0		ns	
$t_H(L)$	$S_n$ to CP	0		0		0			
$t_W(H)$	CP Pulse Width, HIGH	5.0		5.5		5.5		ns	
$t_W(L)$	$\overline{MR}$ Pulse Width, LOW	5.0		5.0		5.0		ns	
$t_{REC}$	Recovery Time $\overline{MR}$ to CP	9.0		9.0		11.0		ns	

**Physical Dimensions** inches (millimeters) unless otherwise noted



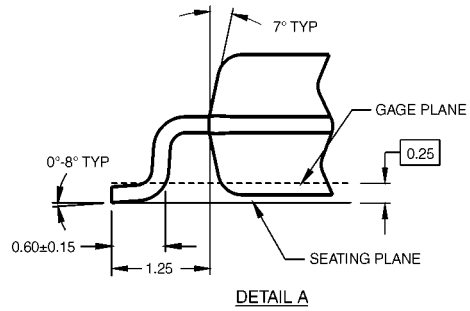
**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow**  
**Package Number M16A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



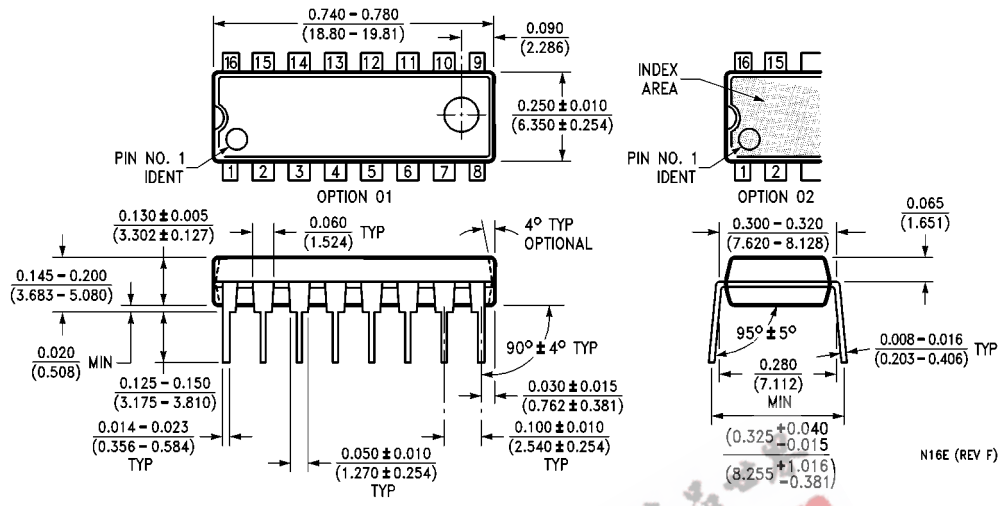
- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRRevB1



**16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide  
Package Number N16E

N16E (REV F)

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