HD74LS195A● 4-bit Parallel-Access Shift Registers

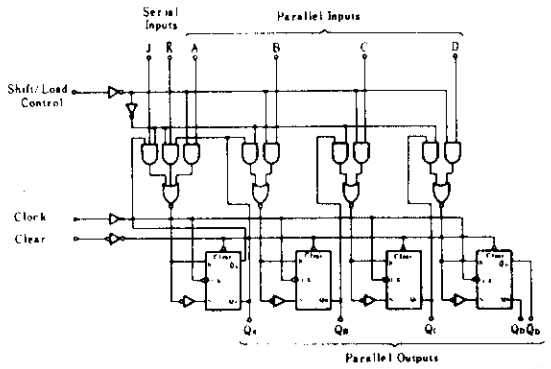
This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

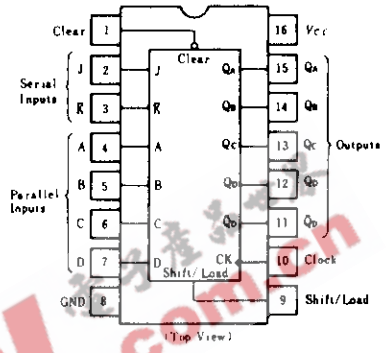
Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■RECOMMENDED OPERATING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	–	30	MHz
Clock pulse width		$t_{w(CK)}$	16	–	–	ns
Clear pulse width		$t_{w(CLR)}$	12	–	–	ns
Setup time	Shift/load	t_{su}	25	–	–	ns
	Seiral and parallel data		15	–	–	
	Clear inactive-state		25	–	–	
Release time		$t_{release}$	–	–	5	ns
Hold time		t_h	0	–	–	ns

■FUNCTION TABLE

Inputs									Outputs				
Clear	Shift/Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	×	×	×	×	×	×	×	×	L	L	L	L	H
H	L	↑	×	×	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	×	×	×	×	×	×	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	×	×	×	×	Q_{A0}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	×	×	×	×	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	×	×	×	×	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	×	×	×	×	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. ↓; transition from high to low level
4. a~d; the level of steady-state input at inputs A,B,C, or D, respectively
5. Q_{A0}~Q_{D0}; the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
6. Q_{An}~Q_{Dn}; the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↑ transition of the clock.

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
			$I_{OL}=8mA$	–	–	0.5	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
Short-circuit output current	I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current**	I_{CC}	$V_{CC}=5.25V$		–	14	21	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

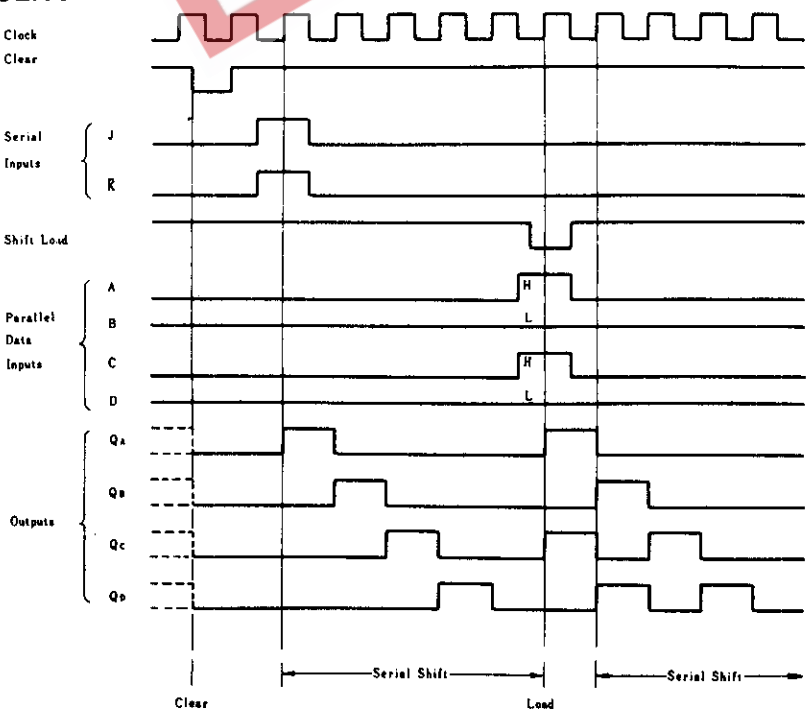
* $V_{CC}=5V$, $Ta=25°C$

** With all outputs open, shift/load grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V, to clear and then applying a momentary ground, followed by 4.5V, to clock.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

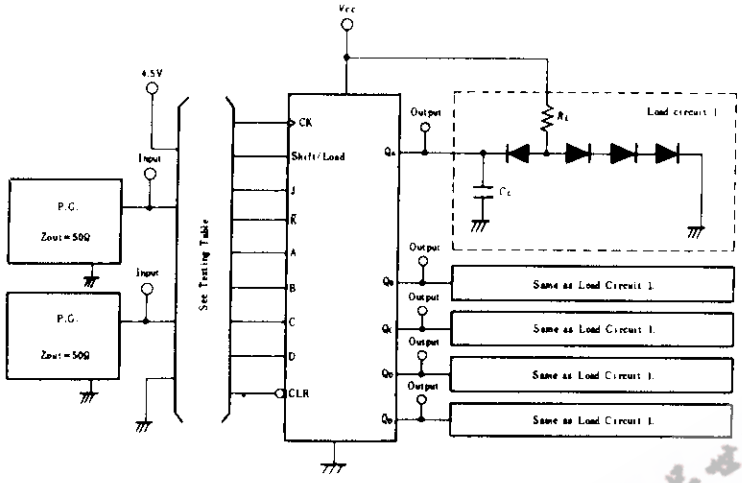
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$	$C_L=15pF$, $R_L=2k\Omega$	30	39	–	MHz
Propagation delay time	t_{PHL}	Clear	$Q_A \sim Q_D$		–	19	30	ns
	t_{PLH}	Clock	$Q_A \sim Q_D$, $\overline{Q}_D$		–	14	22	ns
	t_{PHL}				–	17	26	ns

■COUNT SEQUENCE



■TESTING METHOD

1) Test Circuit

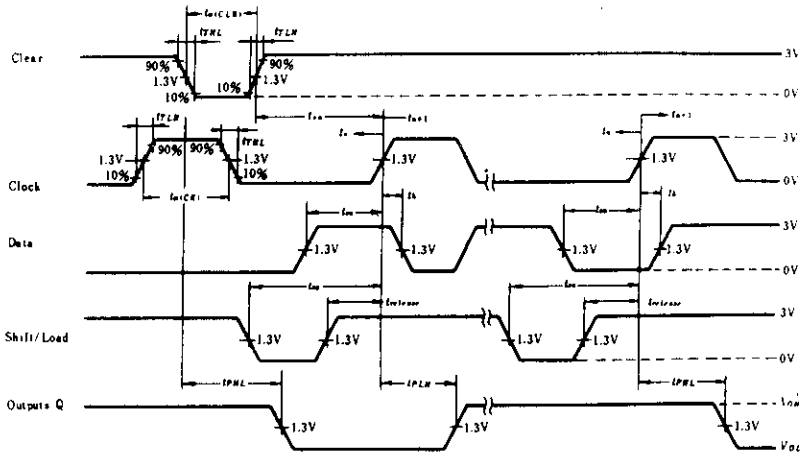


Notes) 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074 (H).

2) Testing Table

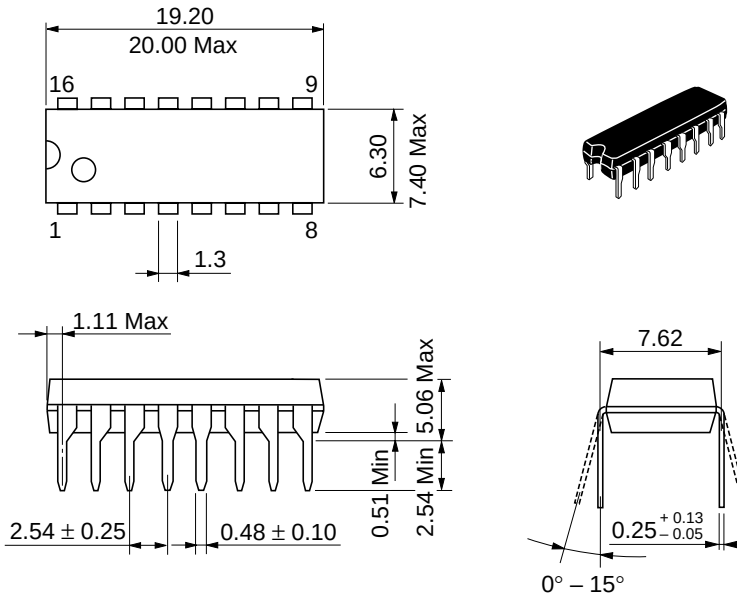
Item	From input to output	Inputs									Outputs				
		CLR	Shift/Load	J	$\overline{K}$	CK	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
f_{max}		4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	OUT
t_{PHL}	Clear→ Q_A~Q_D	IN	GND	4.5V	4.5V	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	—
t_{PLH}	Clock→ Q_A~Q_D, $\overline{Q}_D$	4.5V	4.5V	4.5V	GND	IN	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	OUT
t_{PHL}		4.5V	GND	4.5V	4.5V	IN	IN	IN	IN	IN	OUT	OUT	OUT	OUT	OUT

Waveform



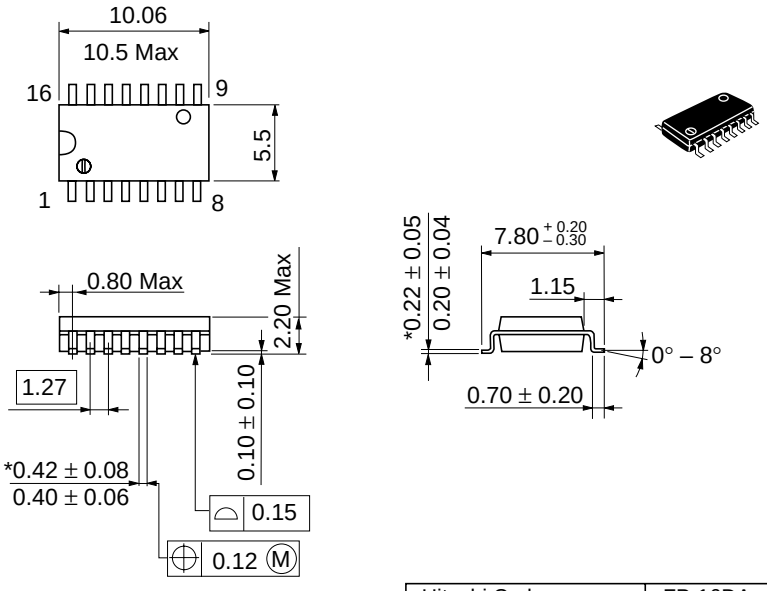
Notes) 1. Input pulse; $t_{TLH} \leqq 15$ns, $t_{THL} \leqq 6$ns, PRR=1MHz, duty cycle 50%
2. A clear pulse is applied prior to each test.
3. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
4. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
5. t_n; bit time before clocking transition.
6. t_{n+1}; bit time after one clocking transition.
7. t_{n+4}; bit time after four clocking transition.

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

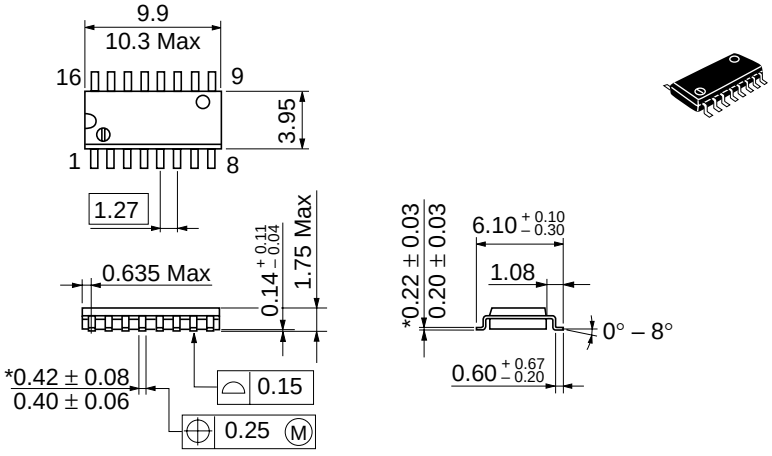
Unit: mm



Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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