FAIRCHILD SEMICONDUCTOR™

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74F169
4-Stage Synchronous Bidirectional Counter

General Description

The 74F169 is a fully synchronous 4-stage up/down counter. The 74F169 is a modulo-16 binary counter. Features a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the clock.

Features

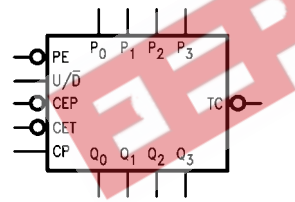
- Asynchronous counting and loading
- Built-in lookahead carry capability
- Presettable for programmable operation

Ordering Code:

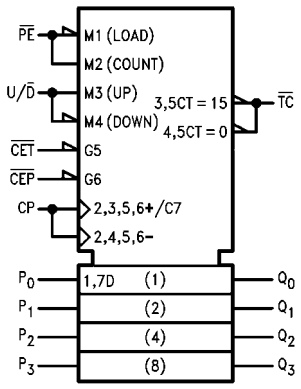
Order Number	Package Number	Package Description
74F169SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74F169SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F169PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

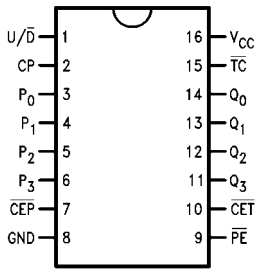
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{CEP}$	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{CET}$	Count Enable Trickle Input (Active LOW)	1.0/2.0	20 µA/–1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
P_0–P_3	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
$\overline{PE}$	Parallel Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
U/$\overline{D}$	Up-Down Count Control Input	1.0/1.0	20 µA/–0.6 mA
Q_0–Q_3	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
$\overline{TC}$	Terminal Count Output (Active LOW)	50/33.3	–1 mA/20 mA

Functional Description

The 74F169 uses edge-triggered J-K type flip-flops and has no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0–P_3 inputs enters the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 15 for the 74F169 in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

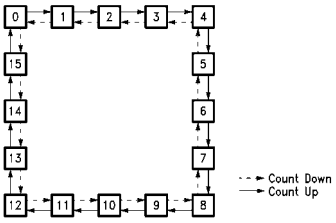
1. Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$
2. Up: (74F169): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet$ (Up) $\bullet \overline{CET}$
3. Down: $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet$ (Down) $\bullet \overline{CET}$

Mode Select Table

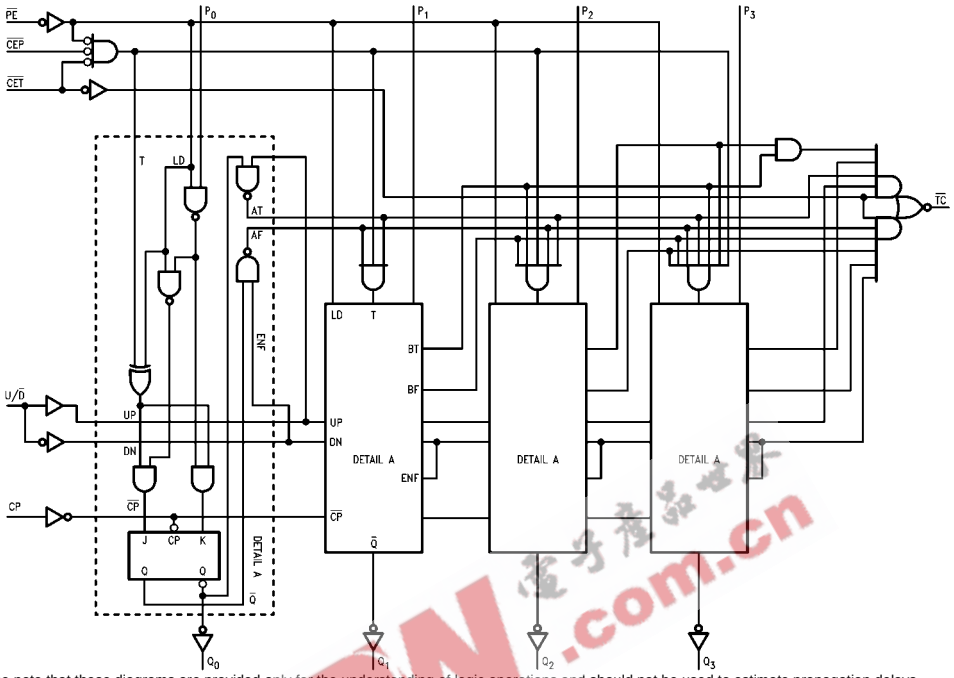
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load ($P_n \rightarrow Q_n$)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		5% V_{CC}	2.7					I_{OH} = −1 mA
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (except $\overline{CET}$)
					−1.2			V_{IN} = 0.5V ($\overline{CET}$)
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{CCL}	Power Supply Current			35	52	mA	Max	V_O = LOW

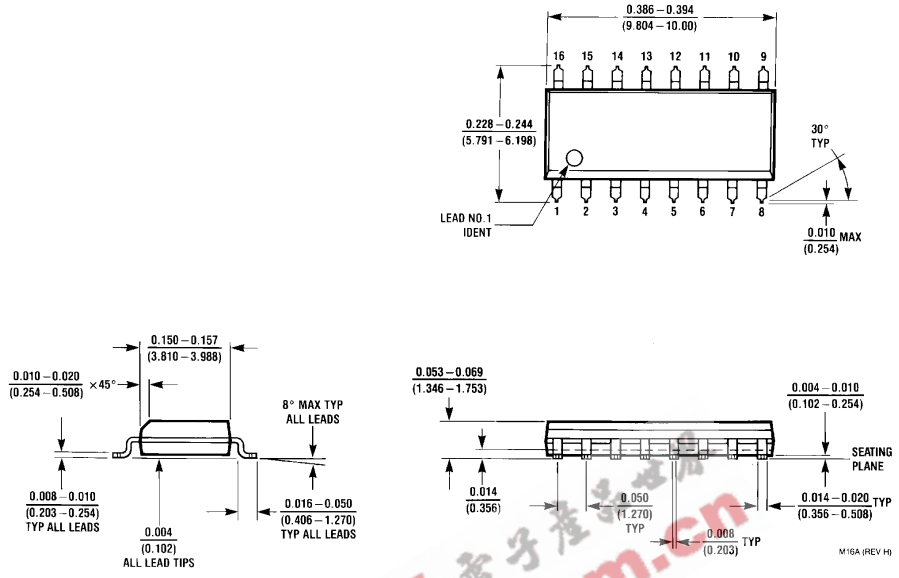
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
f_{MAX}	Maximum Count Frequency	90			60		70		MHz
t_{PLH}	Propagation Delay	3.0	6.5	8.5	3.0	12.0	3.0	9.5	ns
t_{PHL}	CP to Q_n ($\overline{PE}$ HIGH or LOW)	4.0	9.0	11.5	4.0	16.0	4.0	13.0	
t_{PLH}	Propagation Delay	5.5	12.0	15.5	5.5	20.0	5.5	17.5	ns
t_{PHL}	CP to $\overline{TC}$	4.0	8.5	12.5	4.0	15.0	4.0	13.0	
t_{PLH}	Propagation Delay	2.5	4.5	6.5	2.5	9.0	2.5	7.0	ns
t_{PHL}	$\overline{CET}$ to $\overline{TC}$	2.5	8.5	11.0	2.5	12.0	2.5	12.0	
t_{PLH}	Propagation Delay	3.5	8.5	11.5	3.5	16.0	3.5	12.5	ns
t_{PHL}	U/$\overline{D}$ to $\overline{TC}$	4.0	8.0	12.0	4.0	14.0	4.0	13.0	

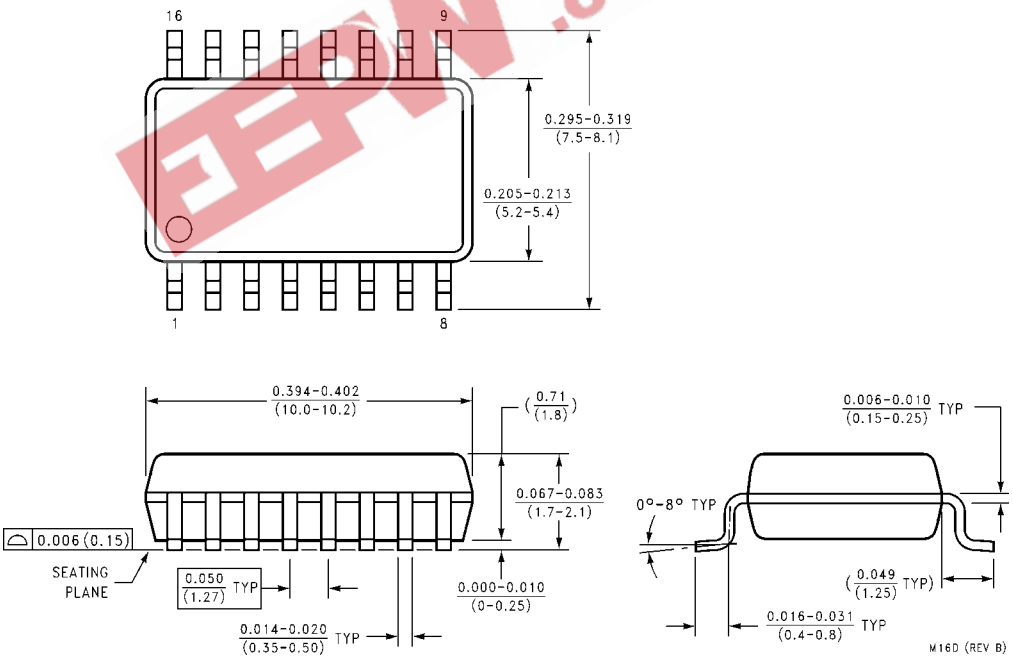
AC Operating Requirements

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = -55°C$ to $+125°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	4.0		4.5		4.5		ns
$t_S(L)$	P_n to CP	4.0		4.5		4.5		
$t_H(H)$	Hold Time, HIGH or LOW	3.0		3.5		3.5		
$t_H(L)$	P_n to CP	3.0		3.5		3.5		
$t_S(H)$	Setup Time, HIGH or LOW	7.0		8.0		8.0		ns
$t_S(L)$	$\overline{CEP}$ or $\overline{CET}$ to CP	5.0		8.0		6.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		0		
$t_H(L)$	$\overline{CEP}$ or $\overline{CET}$ to CP	0.5		1.0		0.5		
$t_S(H)$	Setup Time, HIGH or LOW	8.0		10.0		9.0		ns
$t_S(L)$	$\overline{PE}$ to CP	8.0		10.0		9.0		
$t_H(H)$	Hold Time, HIGH or LOW	1.0		1.0		1.0		
$t_H(L)$	$\overline{PE}$ to CP	0		0		0		
$t_S(H)$	Setup Time, HIGH or LOW	11.0		14.0		12.5		ns
$t_S(L)$	U/$\overline{D}$ to CP	7.0		12.0		8.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		0		
$t_H(L)$	U/$\overline{D}$ to CP	0		0		0		
$t_W(H)$	CP Pulse Width	4.0		6.0		4.5		ns
$t_W(L)$	HIGH or LOW	7.0		9.0		8.0		

Physical Dimensions inches (millimeters) unless otherwise noted

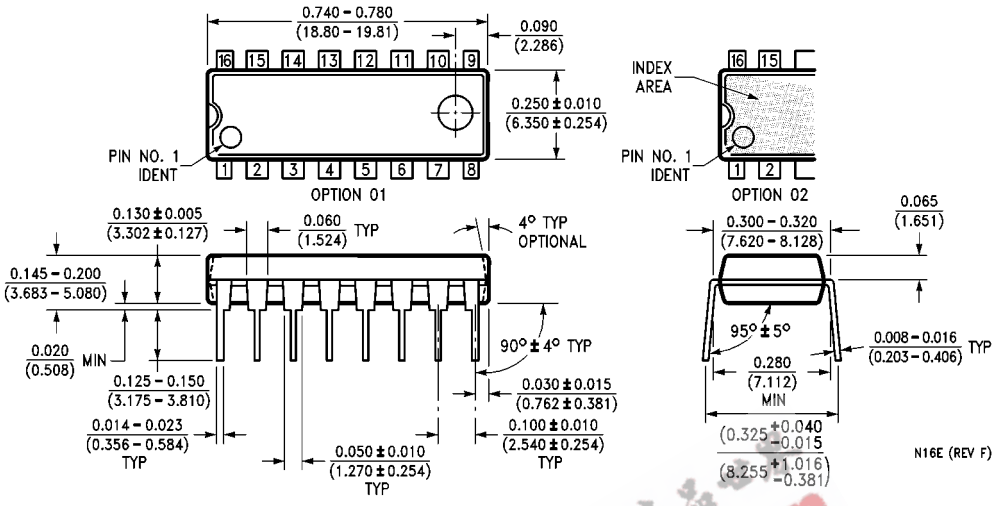


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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