

74ACTQ153 Quiet Series Dual 4-Input Multiplexer

General Description

The ACTQ153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the ACTQ153 can act as a function generator and generate any two functions of three variables.

Features

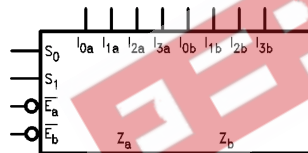
- Outputs source/sink 24 mA
- ACTQ153 has TTL-compatible inputs
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Improved latch-up immunity

Ordering Code:

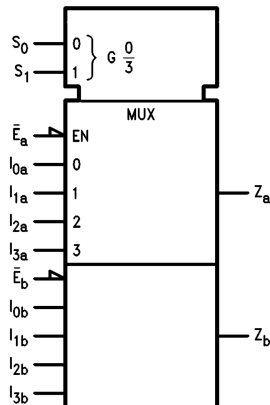
Order Number	Package Number	Package Description
74ACTQ153SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
74ACTQ153PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

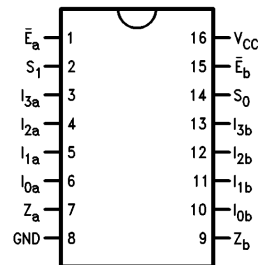
Logic Symbols



IEEE/IEC



Connection Diagram



Pin Descriptions

Pin Names	Description
I _{0a} - I _{3a}	Side A Data Inputs
I _{0b} - I _{3b}	Side B Data Inputs
S ₀ , S ₁	Common Select Inputs
\bar{E}_a	Side A Enable Input
\bar{E}_b	Side B Enable Input
Z _a	Side A Output
Z _b	Side B Output

FACT™, FACT Quiet Series™, and GTO™ are trademarks of Fairchild Semiconductor Corporation.

Functional Description

The ACTQ153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active-LOW Enables (\bar{E}_a , \bar{E}_b) which can be used to strobe the outputs independently. When the Enables (\bar{E}_a , \bar{E}_b) are HIGH, the corresponding outputs (Z_a , Z_b) are forced LOW. The ACTQ153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \bar{E}_a \cdot (I_{0a} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1a} \cdot \bar{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \bar{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

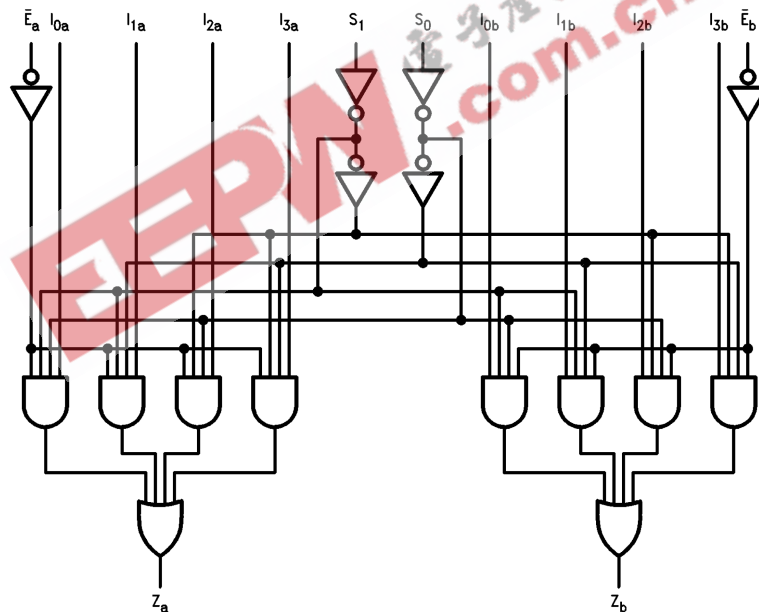
$$Z_b = \bar{E}_b \cdot (I_{0b} \cdot \bar{S}_1 \cdot \bar{S}_0 + I_{1b} \cdot \bar{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \bar{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

Truth Table

Select Inputs		Inputs (a or b)					Outputs
S_0	S_1	\bar{E}	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
DC Latch-Up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate $\Delta V/\Delta t$	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Typ	Guaranteed Limits				
V_{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	2.0	2.0			
V_{IL}	Maximum LOW Level Input Voltage	4.5	1.5	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		5.5	1.5	0.8	0.8			
V_{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu\text{A}$	
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76			V
5.5		4.86	4.76					
V_{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$	
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44			V
5.5		0.36	0.44					
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}, \text{ GND}$	
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	μA	$V_I = V_{CC} - 2.1V$	
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	$V_{OLD} = 1.65V \text{ Max}$	
I_{OHD}	Output Current (Note 3)	5.5			-75	mA	$V_{OHD} = 3.85V \text{ Min}$	
I_{CC}	Maximum Quiescent Supply Current	5.5		8.0	80.0	μA	$V_{IN} = V_{CC}$ or GND	
V_{OLP}	Maximum HIGH Level Output Noise	5.0	1.1	1.5		V	Figures 1, 2 (Note 4)(Note 5)	
V_{OLV}	Maximum LOW Level Output Noise	5.0	-0.6	-1.2		V	Figures 1, 2	
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	1.9	2.2		V	(Note 4)(Note 6)	
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	1.2	0.8		V	(Note 4)(Note 6)	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: Worst case package.

Note 5: Max number of outputs defined as (n). Data Inputs are driven 0V to 5V. One Data Input @ $V_{IN} = \text{GND}$.

Note 6: Max number of Data Inputs (n) switching. (n-1) inputs switching 0V to 5V. Input-under-test switching: 5V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), $f = 1 \text{ MHz}$.

AC Electrical Characteristics								
Symbol	Parameter	V _{CC} (V) (Note 7)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay S _n to Z _n	5.0	3.0	7.0	11.5	2.0	13.5	ns
t _{PHL}	Propagation Delay S _n to Z _n	5.0	3.0	7.0	11.5	2.5	13.5	ns
t _{PLH}	Propagation Delay E _n to Z _n	5.0	2.0	6.5	10.5	2.0	12.5	ns
t _{PHL}	Propagation Delay E _n to Z _n	5.0	3.0	6.0	9.5	2.5	11.0	ns
t _{PLH}	Propagation Delay I _n to Z _n	5.0	2.5	5.5	9.5	2.0	11.0	ns
t _{PHL}	Propagation Delay I _n to Z _n	5.0	2.0	5.5	9.5	2.0	11.0	ns

Note 7: Voltage Range 5.0 is 5.0V ± 0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	65.0	pF	V _{CC} = 5.0V

FACT Noise Characteristics

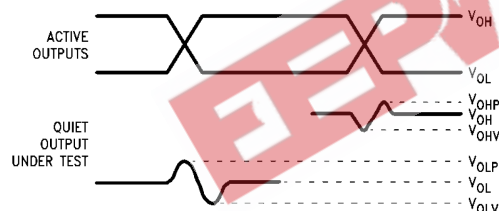
The setup of a noise characteristics measurement is critical to the accuracy and repeatability of the tests. The following is a brief description of the setup used to measure the noise characteristics of FACT.

Equipment:

Hewlett Packard Model 8180A Word Generator
PC-163A Test Fixture
Tektronics Model 7854 Oscilloscope

Procedure:

1. Verify Test Fixture Loading: Standard Load 50 pF, 500Ω.
2. Deskew the HFS generator so that no two channels have greater than 150 ps skew between them. This requires that the oscilloscope be deskewed first. It is important to deskew the HFS generator channels before testing. This will ensure that the outputs switch simultaneously.
3. Terminate all inputs and outputs to ensure proper loading of the outputs and that the input levels are at the correct voltage.
4. Set the HFS generator to toggle all but one output at a frequency of 1 MHz. Greater frequencies will increase DUT heating and effect the results of the measurement.
5. Set the HFS generator input levels at 0V LOW and 3V HIGH for ACT devices and 0V LOW and 5V HIGH for AC devices. Verify levels with an oscilloscope.



Note 8: V_{OHV} and V_{OLP} are measured with respect to ground reference.

Note 9: Input pulses have the following characteristics: $f = 1$ MHz, $t_r = 3$ ns, $t_f = 3$ ns, skew < 150 ps.

FIGURE 1. Quiet Output Noise Voltage Waveforms

V_{OLP}/V_{OLV} and V_{OHP}/V_{OHV} :

- Determine the quiet output pin that demonstrates the greatest noise levels. The worst case pin will usually be the furthest from the ground pin. Monitor the output voltages using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- Measure V_{OLP} and V_{OLV} on the quiet output during the worst case transition for active and enable. Measure V_{OHP} and V_{OHV} on the quiet output during the worst case active and enable transition.
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

V_{ILD} and V_{IHD} :

- Monitor one of the switching outputs using a 50Ω coaxial cable plugged into a standard SMB type connector on the test fixture. Do not use an active FET probe.
- First increase the input LOW voltage level, V_{IL} , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input LOW voltage level at which oscillation occurs is defined as V_{ILD} .
- Next decrease the input HIGH voltage level, V_{IH} , until the output begins to oscillate or steps out a min of 2 ns. Oscillation is defined as noise on the output LOW level that exceeds V_{IL} limits, or on output HIGH levels that exceed V_{IH} limits. The input HIGH voltage level at which oscillation occurs is defined as V_{IHD} .
- Verify that the GND reference recorded on the oscilloscope has not drifted to ensure the accuracy and repeatability of the measurements.

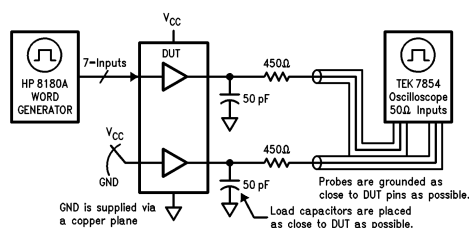
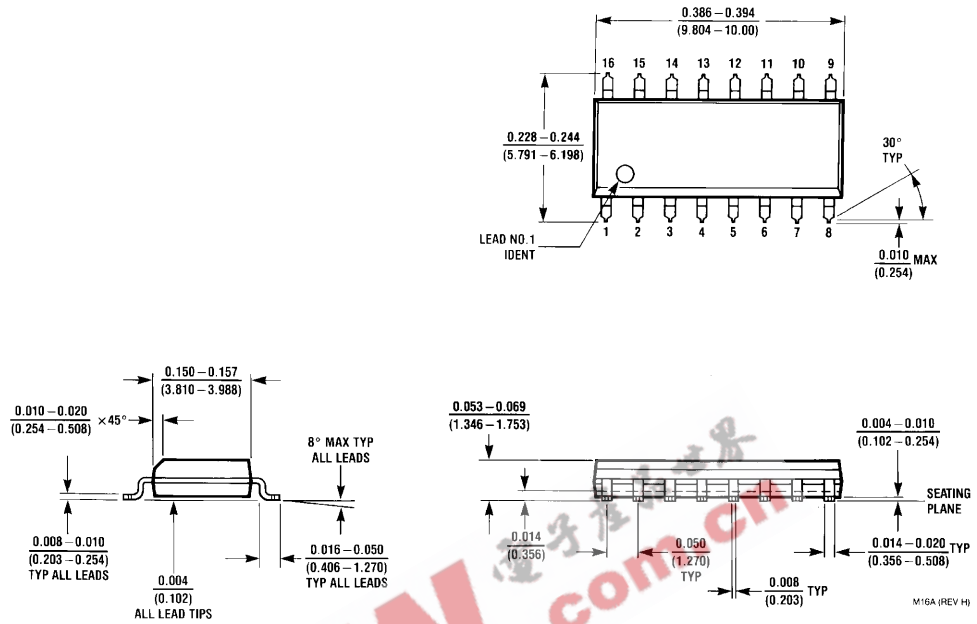


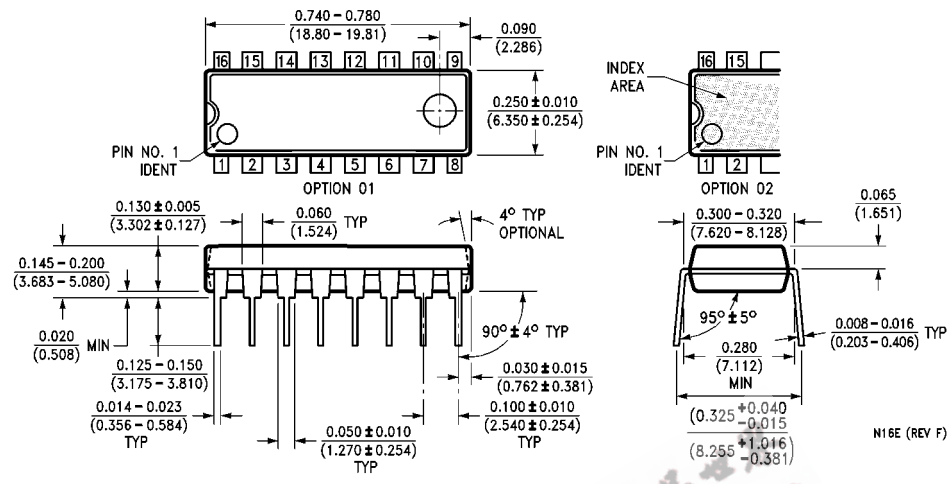
FIGURE 2. Simultaneous Switching Test Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M16A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N16E



Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com