

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT191

Presettable synchronous 4-bit
binary up/down counter

Product specification
File under Integrated Circuits, IC06

December 1990

Presettable synchronous 4-bit binary up/down counter

74HC/HCT191

FEATURES

- Synchronous reversible counting
- Asynchronous parallel load
- Count enable control for synchronous expansion
- Single up/down control input
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT191 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT191 are asynchronously presettable 4-bit binary up/down counters. They contain four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation.

Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs when the parallel load (\overline{PL}) input is LOW. As indicated in the function table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the count enable (\overline{CE}) input. When \overline{CE} is LOW internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The up/down ($\overline{U/D}$) input signal determines the direction of counting as indicated in the function table. The \overline{CE} input may go LOW when the clock is in either state, however, the LOW-to-HIGH \overline{CE} transition must occur only when the clock is HIGH. Also, the $\overline{U/D}$ input should be changed only when either \overline{CE} or CP is HIGH.

Overflow/underflow indications are provided by two types of outputs, the terminal count (TC) and ripple clock (\overline{RC}). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "15" in the count-up-mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U/D}$ is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes. The TC signal is used internally to enable the \overline{RC} output. When TC is HIGH and \overline{CE} is LOW, the \overline{RC} output follows the clock pulse (CP). This feature simplifies the design of multistage counters as shown in Figs 5 and 6.

In Fig.5, each \overline{RC} output is used as the clock input to the next higher stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH on \overline{CE} inhibits the \overline{RC} output pulse as indicated in the function table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This can be a disadvantage of this configuration in some applications.

Fig.6 shows a method of causing state changes to occur simultaneously in all stages. The \overline{RC} outputs propagate the carry/borrow signals in ripple fashion and all clock inputs are driven in parallel. In this configuration the duration of the clock LOW state must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the \overline{RC} output of any package goes HIGH shortly after its CP input goes HIGH there is no such restriction on the HIGH-state duration of the clock.

In Fig.7, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the \overline{CE} input for a given stage. An enable must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own \overline{CE} signal therefore the simple inhibit scheme of Figs 5 and 6 does not apply.

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QUICK REFERENCE DATAGND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|--|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay CP to Q_n | $C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$ | 22 | 22 | ns |
| f_{max} | maximum clock frequency | | 36 | 36 | MHz |
| C_I | input capacitance | | 3.5 | 3.5 | pF |
| C_{PD} | power dissipation capacitance per package | notes 1 and 2 | 31 | 33 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_I = \text{GND to } V_{CC}$
For HCT the condition is $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

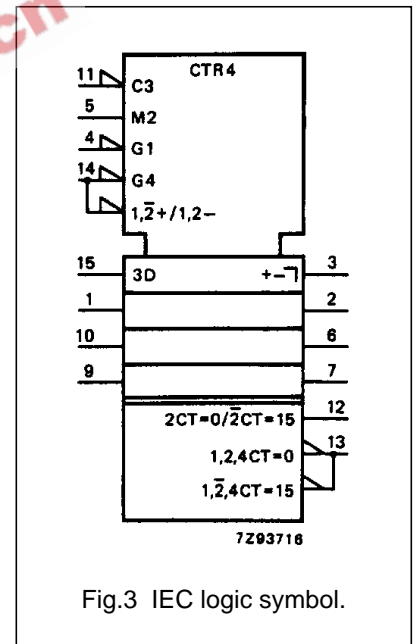
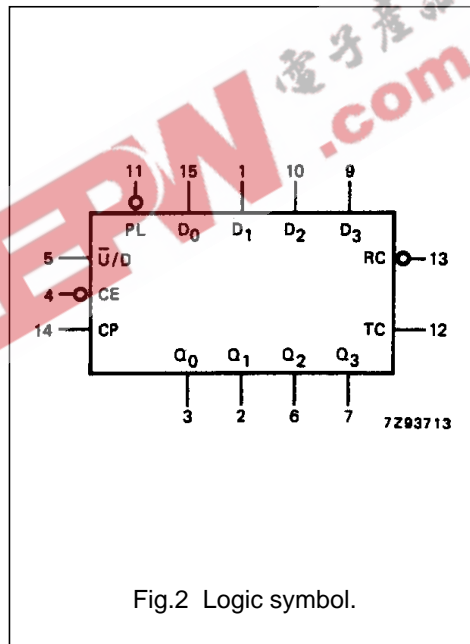
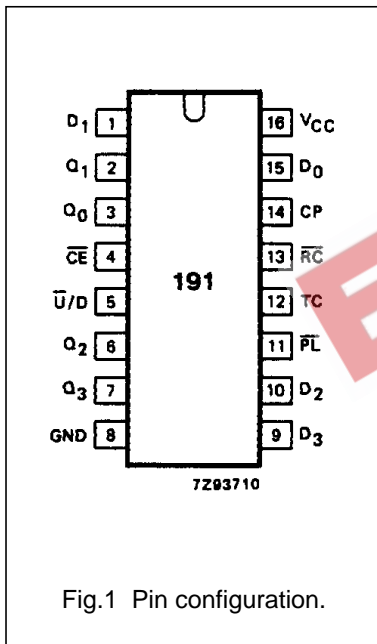
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------|----------------------------------|---|
| 3, 2, 6, 7 | Q ₀ to Q ₃ | flip-flop outputs |
| 4 | \overline{CE} | count enable input (active LOW) |
| 5 | $\overline{U/D}$ | up/down input |
| 8 | GND | ground (0 V) |
| 11 | \overline{PL} | parallel load input (active LOW) |
| 12 | TC | terminal count output |
| 13 | \overline{RC} | ripple clock output (active LOW) |
| 14 | CP | clock input (LOW-to-HIGH, edge triggered) |
| 15, 1, 10, 9 | D ₀ to D ₃ | data inputs |
| 16 | V _{CC} | positive supply voltage |



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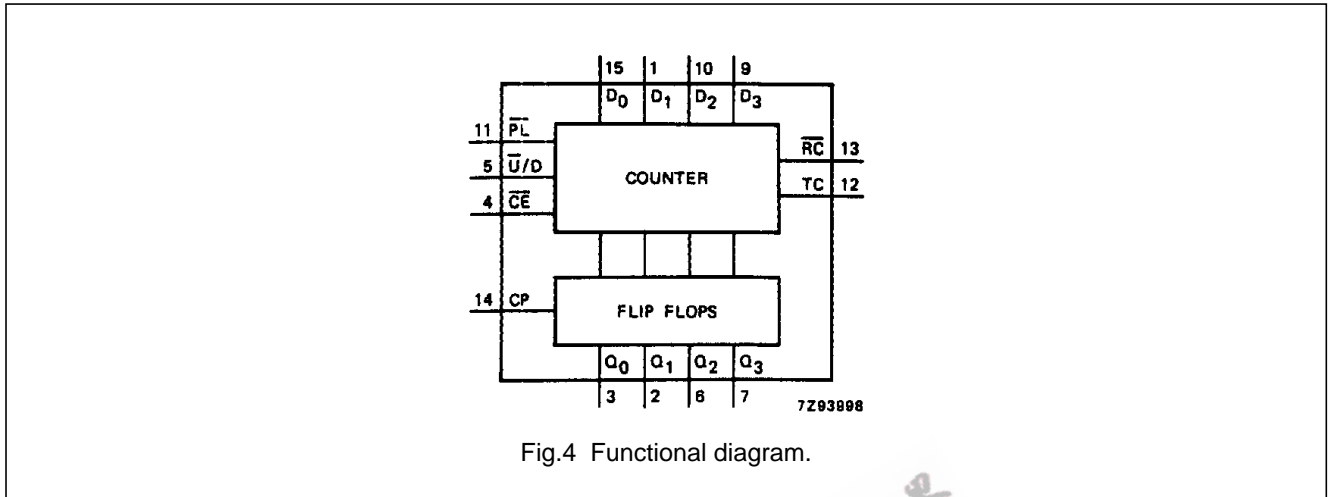


Fig.4 Functional diagram.

FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | | D _n | Q _n |
|-------------------|--------|-----|----|----|----------------|----------------|----------------|
| | PL | U/D | CE | CP | D _n | | |
| parallel load | L | X | X | X | L | L | |
| | L | X | X | X | H | H | |
| count up | H | L | I | ↑ | X | count up | |
| count down | H | H | I | ↑ | X | count down | |
| hold (do nothing) | H | X | H | X | X | no change | |

TC AND RC FUNCTION TABLE

| INPUTS | | | TERMINAL COUNT STATE | | | | OUTPUTS | |
|--------|----|----|----------------------|----------------|----------------|----------------|---------|----|
| U/D | CE | CP | Q ₀ | Q ₁ | Q ₂ | Q ₃ | TC | RC |
| H | H | X | H | H | H | H | L | H |
| L | H | X | H | H | H | H | H | H |
| L | L | ⌊ | H | H | H | H | ⌊ | ⌊ |
| L | H | X | L | L | L | L | L | H |
| H | H | X | L | L | L | L | H | H |
| H | L | ⌊ | L | L | L | L | ⌊ | ⌊ |

Notes

- H = HIGH voltage level
 L = LOW voltage level
 I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
 X = don't care
 ↑ = LOW-to-HIGH CP transition
 ⌊ = one LOW level pulse
 ⌊ = TC goes LOW on a LOW-to-HIGH CP transition

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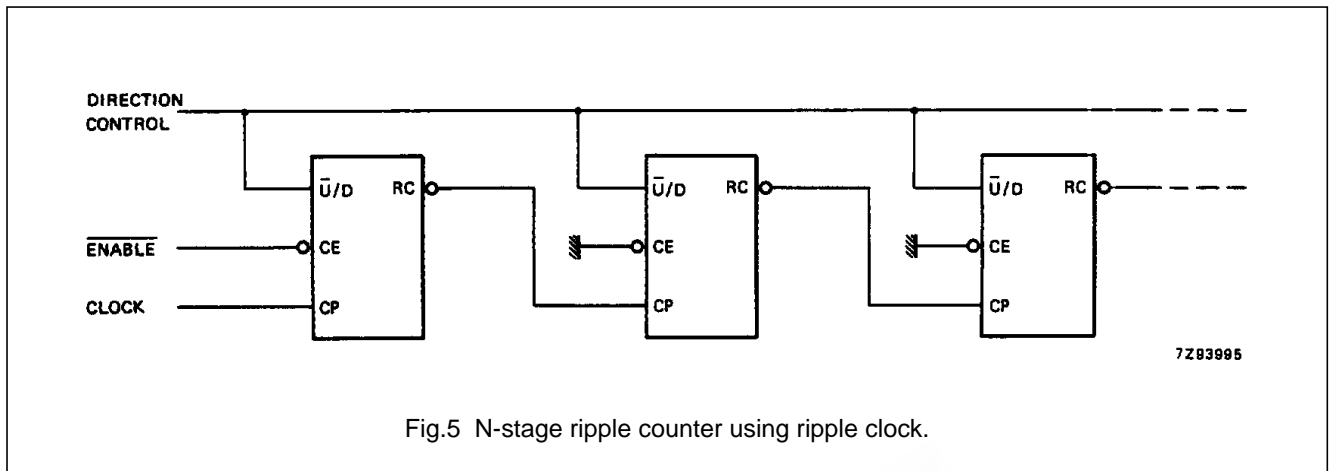


Fig.5 N-stage ripple counter using ripple clock.

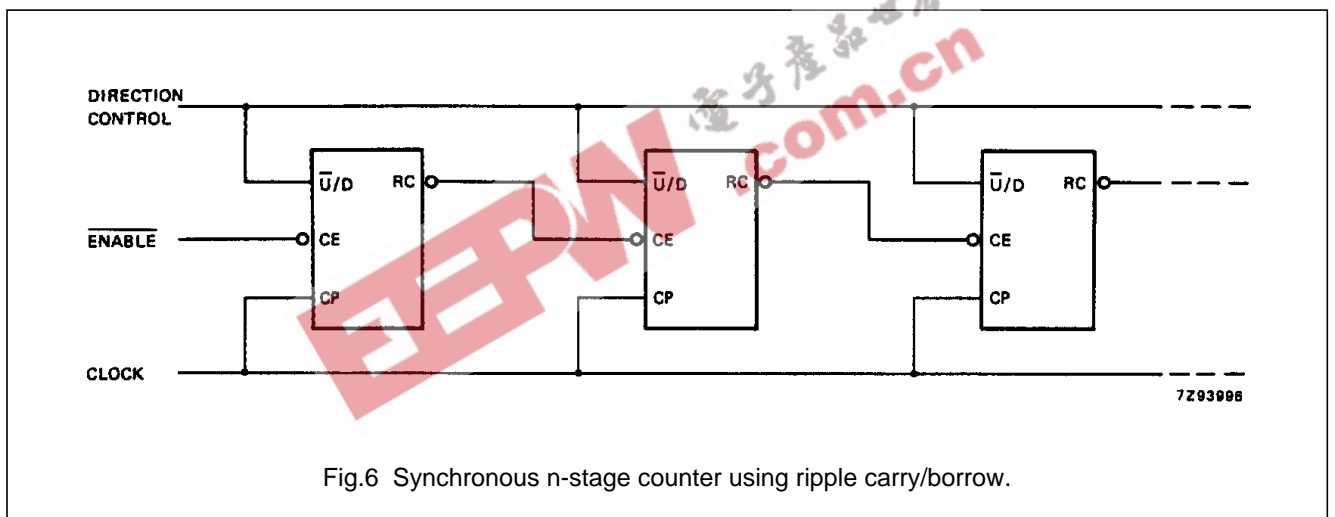


Fig.6 Synchronous n-stage counter using ripple carry/borrow.

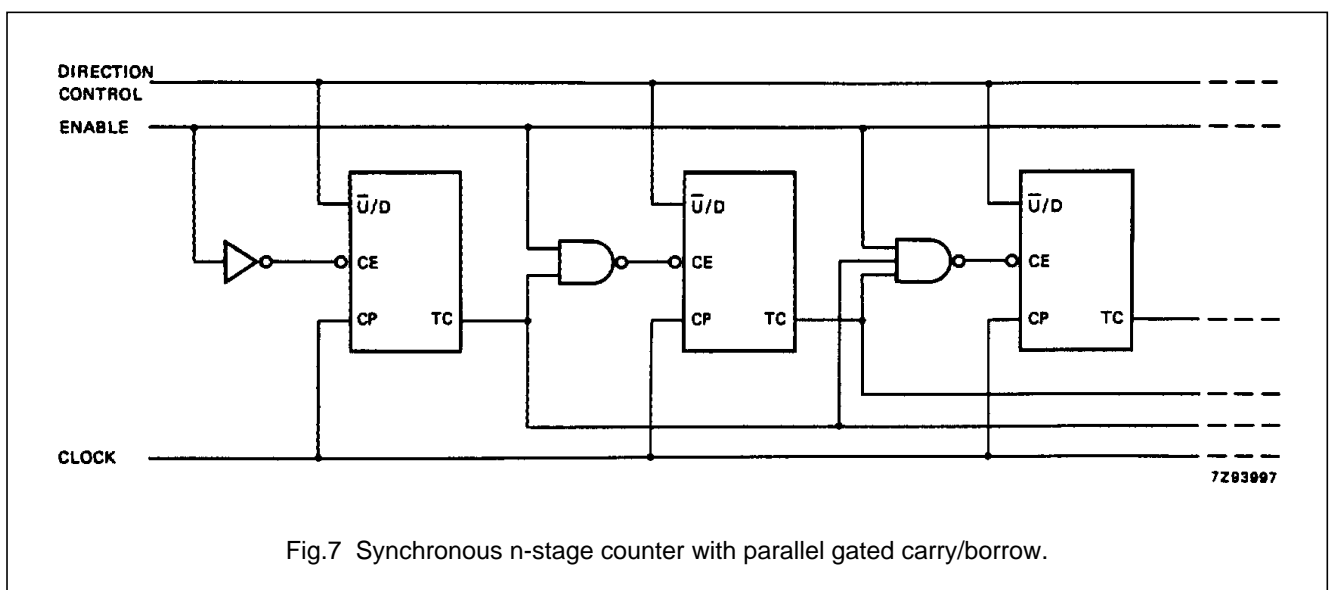


Fig.7 Synchronous n-stage counter with parallel gated carry/borrow.

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Sequence

Load (preset) to binary thirteen;
 count up to fourteen, fifteen,
 zero, one and two;
 inhibit;
 count down to one, zero, fifteen,
 fourteen and thirteen.

Fig.8 Typical load, count and inhibit sequence.

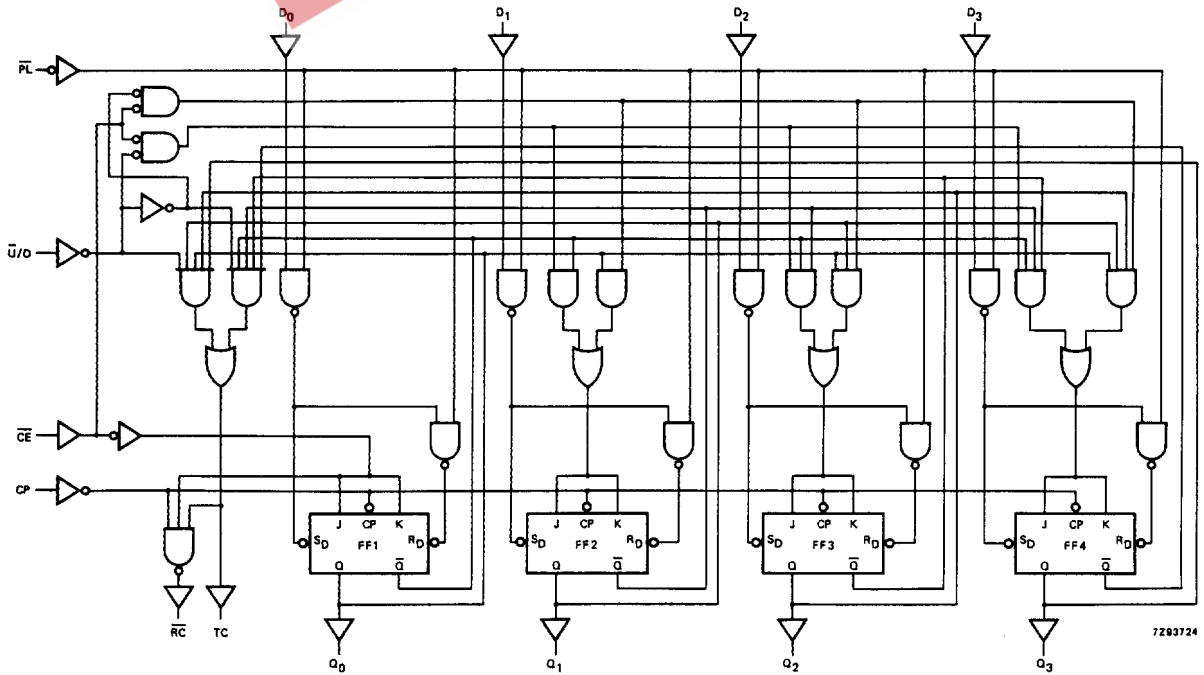
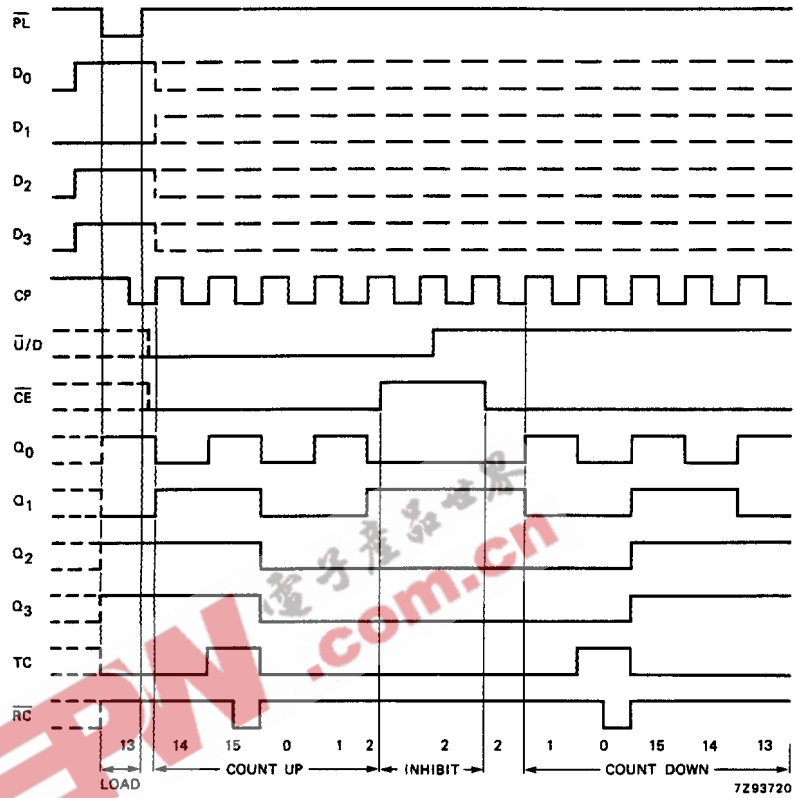


Fig.9 Logic diagram.

Presetable synchronous 4-bit binary up/down counter

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|--|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | |
| | | min. | typ. | max. | min. | max. | min. | | | |
| t _{PHL} / t _{PLH} | propagation delay CP to Q _n | | 72 26 21 | 220 44 37 | | 275 55 47 | 330 66 56 | ns | 2.0 4.5 6.0 | Fig.10 |
| t _{PHL} / t _{PLH} | propagation delay CP to TC | | 83 30 24 | 255 51 43 | | 320 64 54 | 395 77 65 | ns | 2.0 4.5 6.0 | Fig.10 |
| t _{PHL} / t _{PLH} | propagation delay CP to \overline{RC} | | 47 17 14 | 150 30 26 | | 190 38 33 | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.11 |
| t _{PHL} / t _{PLH} | propagation delay CE to RC | | 33 12 10 | 130 26 22 | | 165 33 28 | 195 39 33 | ns | 2.0 4.5 6.0 | Fig.11 |
| t _{PHL} / t _{PLH} | propagation delay D _n to Q _n | | 61 22 18 | 220 44 37 | | 275 55 47 | 330 66 56 | ns | 2.0 4.5 6.0 | Fig.12 |
| t _{PHL} / t _{PLH} | propagation delay \overline{PL} to Q _n | | 61 22 18 | 220 44 37 | | 275 55 47 | 330 66 56 | ns | 2.0 4.5 6.0 | Fig.13 |
| t _{PHL} / t _{PLH} | propagation delay U/D to TC | | 44 16 13 | 190 38 32 | | 240 48 41 | 285 57 48 | ns | 2.0 4.5 6.0 | Fig.14 |
| t _{PHL} / t _{PLH} | propagation delay $\overline{U/D}$ to \overline{RC} | | 50 18 14 | 210 42 36 | | 265 53 45 | 315 63 54 | ns | 2.0 4.5 6.0 | Fig.14 |
| t _{THL} / t _{TLH} | output transition time | | 19 7 6 | 75 15 13 | | 95 19 16 | 110 22 19 | ns | 2.0 4.5 6.0 | Fig.15 |
| t _w | clock pulse width HIGH or LOW | 125 25 21 | 28 10 8 | | 155 31 26 | | 195 39 33 | ns | 2.0 4.5 6.0 | Fig.10 |
| t _w | parallel load pulse width LOW | 100 20 17 | 22 8 6 | | 125 25 21 | | 150 30 26 | ns | 2.0 4.5 6.0 | Fig.15 |

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| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | UNIT | TEST CONDITIONS | |
|------------------|--|-----------------------|-------------------|------|-----------------|------|-----------------|------|------|------------------------|-----------|
| | | 74HC | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | |
| t _{rem} | removal time \overline{PL} to CP | 35 7 6 | 8 3 2 | | 45 9 8 | | 55 11 9 | | ns | 2.0 4.5 6.0 | Fig.15 |
| t _{su} | set-up time $\overline{U/D}$ to CP | 205 41 35 | 50 18 14 | | 255 51 43 | | 310 62 53 | | ns | 2.0 4.5 6.0 | Fig.17 |
| t _{su} | set-up time D _n to \overline{PL} | 100 20 17 | 19 7 6 | | 125 25 21 | | 150 30 26 | | ns | 2.0 4.5 6.0 | Fig.16 |
| t _{su} | set-up time \overline{CE} to CP | 140 28 24 | 44 16 13 | | 175 35 30 | | 210 42 36 | | ns | 2.0 4.5 6.0 | Fig.17 |
| t _h | hold time $\overline{U/D}$ to CP | 0 0 0 | -39 -14 -11 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Fig.17 |
| t _h | hold time D _n to \overline{PL} | 0 0 0 | -11 -4 -3 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Fig.16 |
| t _h | hold time \overline{CE} to CP | 0 0 0 | -28 -10 -8 | | 0 0 0 | | 0 0 0 | | ns | 2.0 4.5 6.0 | Fig.17 |
| f _{max} | maximum clock pulse frequency | 4.0 20 24 | 11 33 39 | | 3.2 16 19 | | 2.6 13 15 | | MHz | 2.0 4.5 6.0 | Fig.10 |

**Presettable synchronous 4-bit binary
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74HC/HCT191**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|--------------------------------|-----------------------|
| D _n | 0.5 |
| CP | 0.65 |
| $\overline{U/D}$ | 1.15 |
| $\overline{CE}, \overline{PL}$ | 1.5 |

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AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------|--|----------------|------|------|------------|------|-------------|------|-----------------|-----------|--------|
| | | 74HC | | | | | | | V_{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t_{PHL}/t_{PLH} | propagation delay CP to Q_n | | 26 | 48 | | 60 | | 72 | ns | 4.5 | Fig.10 |
| t_{PHL}/t_{PLH} | propagation delay CP to TC | | 32 | 51 | | 64 | | 77 | ns | 4.5 | Fig.10 |
| t_{PHL}/t_{PLH} | propagation delay CP to \overline{RC} | | 19 | 35 | | 44 | | 53 | ns | 4.5 | Fig.11 |
| t_{PHL}/t_{PLH} | propagation delay CE to \overline{RC} | | 19 | 33 | | 41 | | 50 | ns | 4.5 | Fig.11 |
| t_{PHL}/t_{PLH} | propagation delay D_n to Q_n | | 22 | 44 | | 55 | | 66 | ns | 4.5 | Fig.12 |
| t_{PHL}/t_{PLH} | propagation delay PL to Q_n | | 27 | 46 | | 58 | | 69 | ns | 4.5 | Fig.13 |
| t_{PHL}/t_{PLH} | propagation delay $\overline{U/D}$ to TC | | 23 | 45 | | 56 | | 68 | ns | 4.5 | Fig.14 |
| t_{PHL}/t_{PLH} | propagation delay $\overline{U/D}$ to \overline{RC} | | 24 | 45 | | 56 | | 68 | ns | 4.5 | Fig.14 |
| t_{THL}/t_{TLH} | output transition time | | 7 | 15 | | 19 | | 22 | ns | 4.5 | Fig.15 |
| t_W | clock pulse width HIGH or LOW | 16 | 9 | | 20 | | 24 | | ns | 4.5 | Fig.10 |
| t_W | parallel load pulse width LOW | 22 | 11 | | 28 | | 33 | | ns | 4.5 | Fig.15 |
| t_{rem} | removal time \overline{PL} to CP | 7 | 1 | | 9 | | 11 | | ns | 4.5 | Fig.15 |
| t_{su} | set-up time $\overline{U/D}$ to CP | 41 | 20 | | 51 | | 62 | | ns | 4.5 | Fig.17 |
| t_{su} | set-up time D_n to \overline{PL} | 20 | 9 | | 25 | | 30 | | ns | 4.5 | Fig.16 |
| t_{su} | set-up time \overline{CE} to CP | 30 | 18 | | 38 | | 45 | | ns | 4.5 | Fig.17 |
| t_h | hold time $\overline{U/D}$ to CP | 0 | -18 | | 0 | | 0 | | ns | 4.5 | Fig.17 |
| t_h | hold time D_n to \overline{PL} | 0 | -5 | | 0 | | 0 | | ns | 4.5 | Fig.16 |
| t_h | hold time CE to CP | 0 | -10 | | 0 | | 0 | | ns | 4.5 | Fig.17 |
| f_{max} | maximum clock pulse frequency | 20 | 33 | | 16 | | 13 | | MHz | 4.5 | Fig.10 |

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AC WAVEFORMS

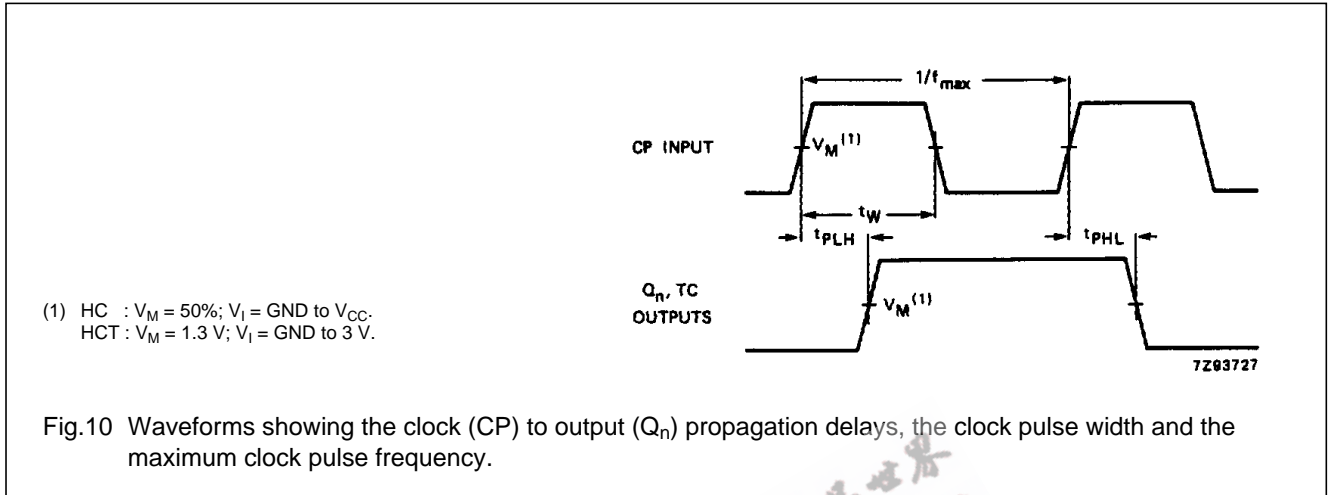


Fig.10 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.

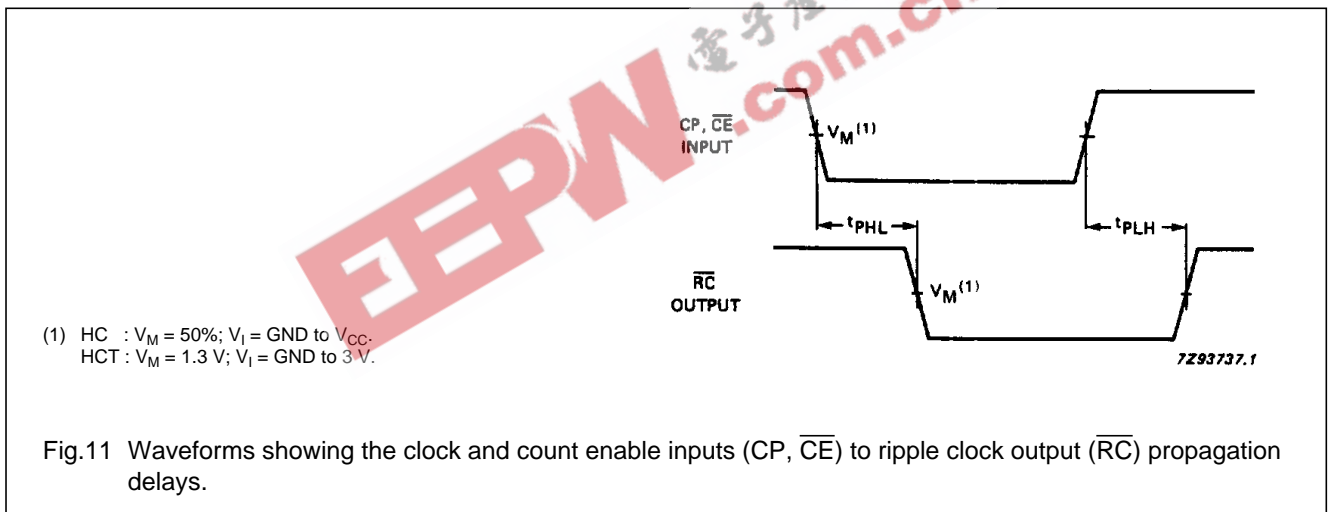


Fig.11 Waveforms showing the clock and count enable inputs (CP, \overline{CE}) to ripple clock output (\overline{RC}) propagation delays.

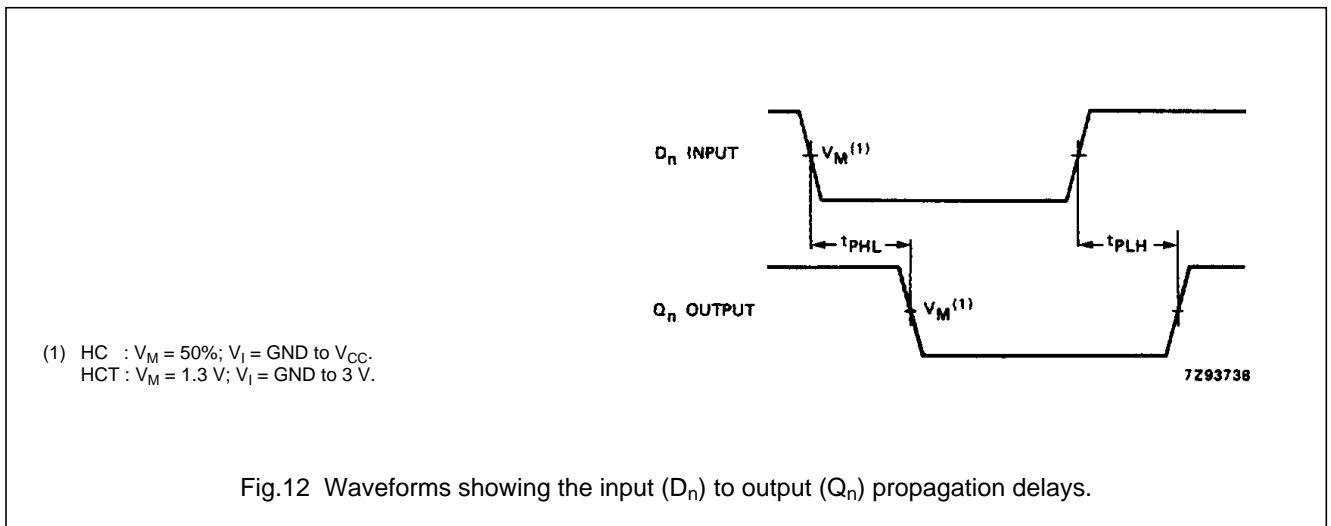


Fig.12 Waveforms showing the input (D_n) to output (Q_n) propagation delays.

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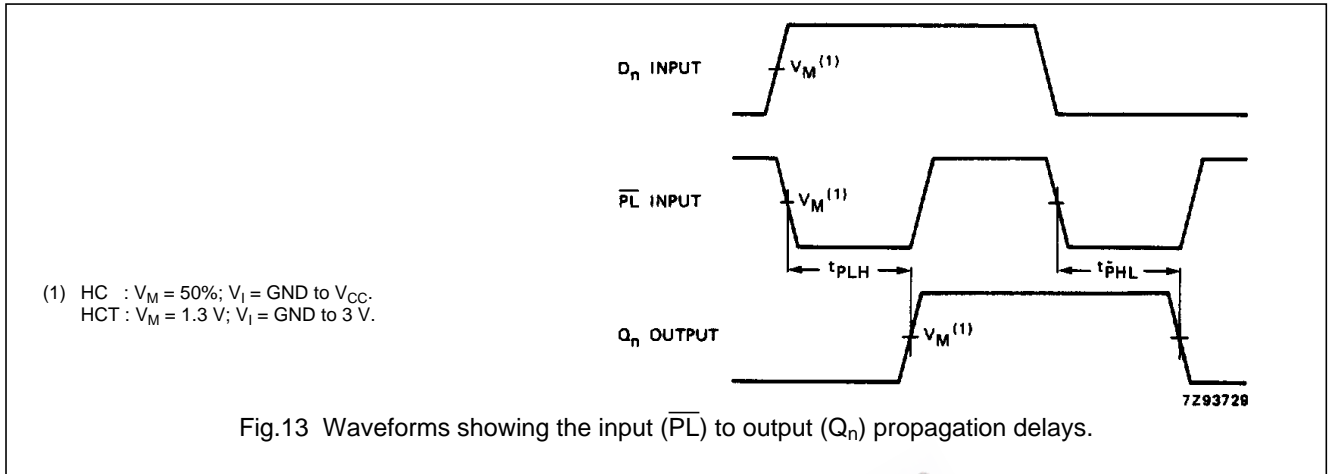


Fig.13 Waveforms showing the input (\overline{PL}) to output (Q_n) propagation delays.

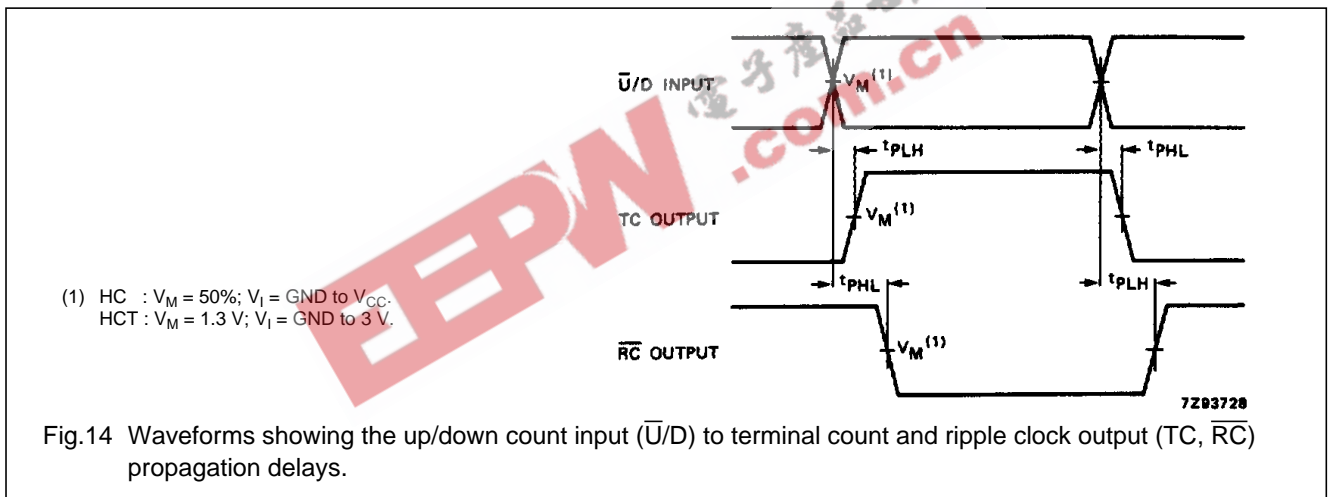


Fig.14 Waveforms showing the up/down count input ($\overline{U/D}$) to terminal count and ripple clock output (TC, \overline{RC}) propagation delays.

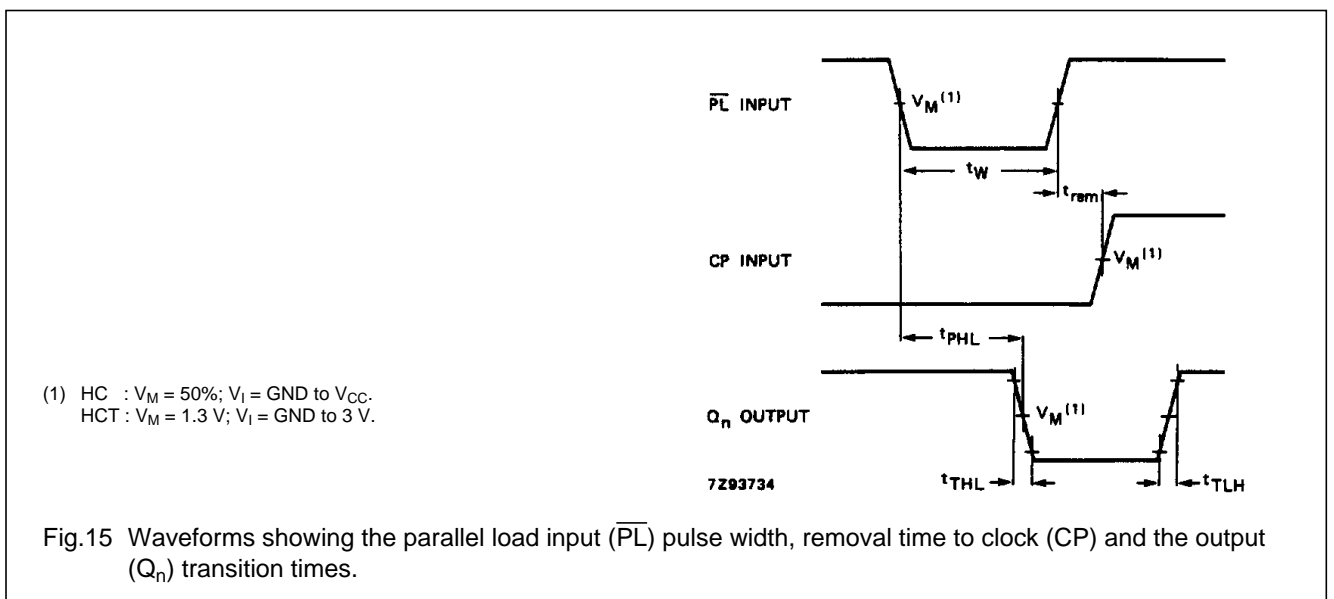


Fig.15 Waveforms showing the parallel load input (\overline{PL}) pulse width, removal time to clock (CP) and the output (Q_n) transition times.

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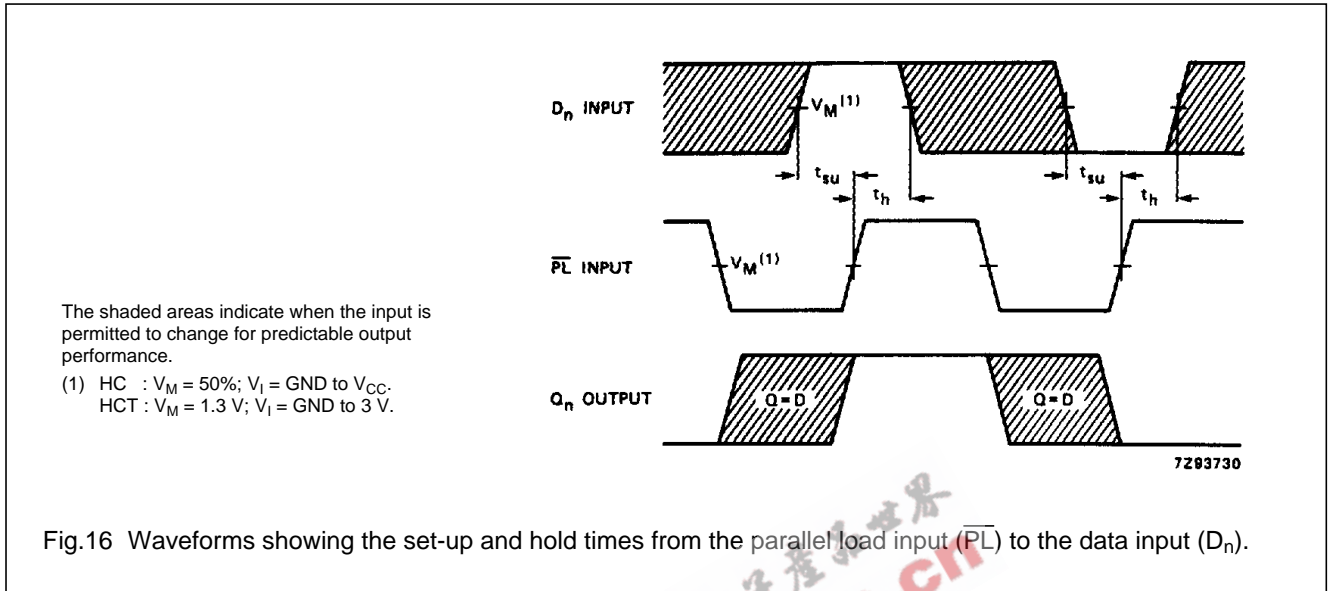


Fig.16 Waveforms showing the set-up and hold times from the parallel load input ($\overline{\text{PL}}$) to the data input (D_n).

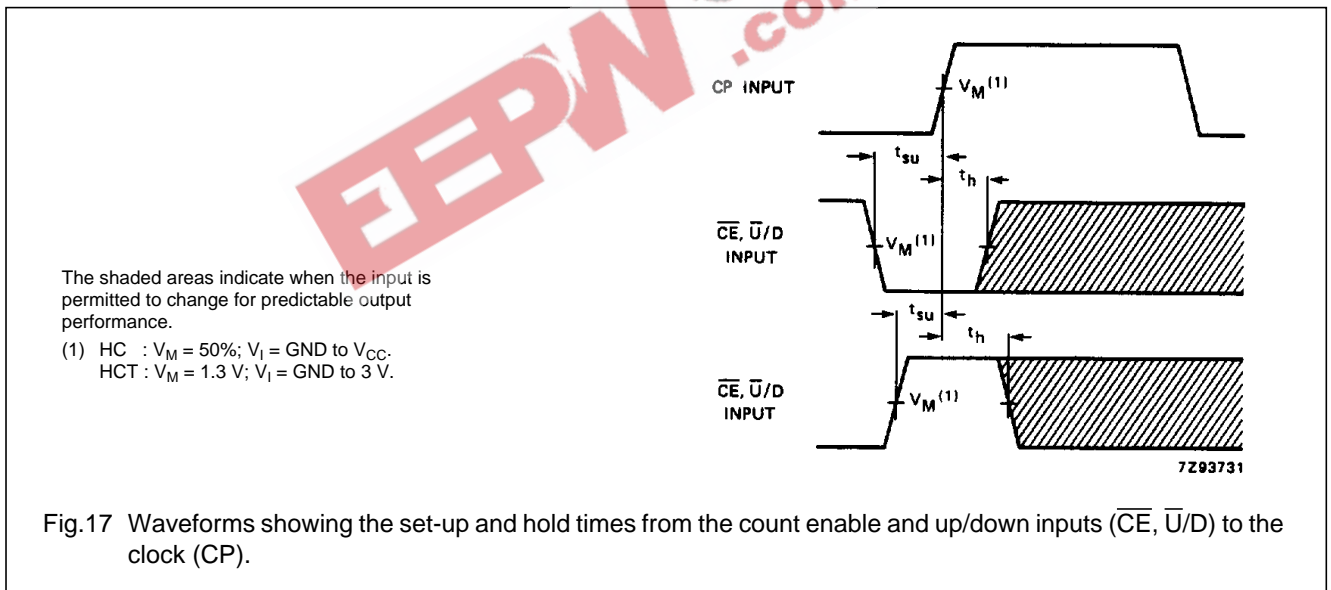


Fig.17 Waveforms showing the set-up and hold times from the count enable and up/down inputs ($\overline{\text{CE}}$, $\overline{\text{U/D}}$) to the clock (CP).

PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".