

Presettable Synchronous 4-Bit Binary Up/Down Counter

October 1998 - Revised May 2000

Features

- **Buffered Inputs**
- **Typical Propagation Delay**
 - 12.8ns at $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 50pF$
- **Exceeds 2kV ESD Protection MIL-STD-883, Method 3015**
- **SCR-Latchup-Resistant CMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption**
- **Balanced Propagation Delays**
- **AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply**
- **±24mA Output Drive Current**
 - Fanout to 15 FAST™ ICs
 - Drives 50Ω Transmission Lines

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54AC191F3A	-55 to 125	16 Ld CERDIP
CD54ACT191F3A	-55 to 125	16 Ld CERDIP

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local TI sales office or customer service for ordering information.

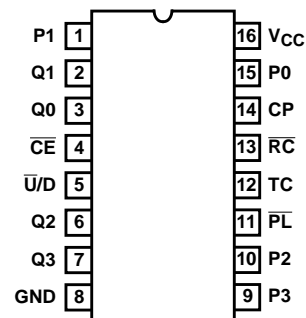
Description

The CD54AC191 and CD54ACT191 are asynchronously presettable binary up/down synchronous counters that utilize Advanced CMOS Logic technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by setting LOW the asynchronous parallel load input (PL). Counting occurs when PL is HIGH, Count Enable (\overline{CE}) is LOW, and the Up/Down ($\overline{U/D}$) input is either LOW for up-counting or HIGH for down-counting. The counter is incremented or decremented synchronously with the LOW-to-HIGH transition of the clock.

When an overflow or underflow of the counter occurs, the Terminal Count (TC) output, which is LOW during counting, goes HIGH and remains HIGH for one clock cycle. This output can be used for look-ahead carry in high-speed cascading (see Figure 12). The TC output also initiates the Ripple Clock (RC) output which, normally HIGH, goes LOW and remains LOW for the low-level cascaded using the Ripple Count output.

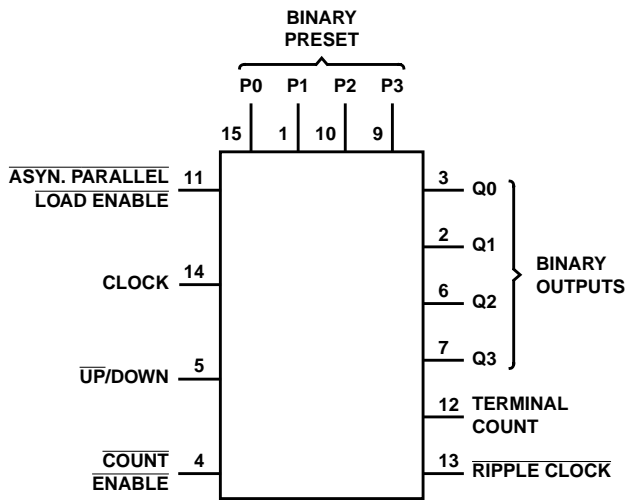
Pinout

CD54AC191, CD54ACT191
(CERDIP)
TOP VIEW



CD54AC191, CD54ACT191

Functional Diagram



TRUTH TABLE

INPUTS				FUNCTION
PL	CE	U/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Asynchronous Preset
H	H	X	X	No Change

U/D or CE should be changed only when clock is high.
 X = Don't Care
 ↑ = Low-to-High clock transition.

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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 6V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 50mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3)	$\pm 100mA$

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} ($^{\circ}C/W$)
PDIP Package	—
SOIC Package	—
Maximum Junction Temperature (Hermetic Package or Die) . . .	$175^{\circ}C$
Maximum Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	$300^{\circ}C$

Operating Conditions

Temperature Range, T_A	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, V_{CC} (Note 4)	
AC Types	1.5V to 5.5V
ACT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv	
AC Types, 1.5V to 3V	50ns (Max)
AC Types, 3.6V to 5.5V	20ns (Max)
ACT Types, 4.5V to 5.5V	10ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$		-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
AC TYPES											
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	2.1	-	V
				5.5	3.85	-	3.85	-	3.85	-	V
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	-	0.9	V
				5.5	-	1.65	-	1.65	-	1.65	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	3	2.58	-	2.48	-	2.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V

CD54AC191, CD54ACT191

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Quiescent Supply Current MSI	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μA
ACT TYPES											
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Quiescent Supply Current MSI	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

ACT Input Load Table

INPUT	UNIT LOAD
P0-P3, PL	0.75
CL, U/D, CE	0.85

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

CD54AC191, CD54ACT191

Prerequisite For Switching Function

PARAMETER	SYMBOL	V _{CC} (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
AC TYPES							
Max. Frequency	f _{MAX} (Note 10)	1.5	5.5	-	4.8	-	MHz
		3.3 (Note 8)	49	-	43	-	MHz
		5 (Note 9)	68	-	60	-	MHz
CP Pulse Width	t _W	1.5	91	-	104	-	ns
		3.3	10.5	-	11.6	-	ns
		5	7.3	-	8.3	-	ns
P _L Pulse Width	t _W	1.5	66	-	75	-	ns
		3.3	7.4	-	8.4	-	ns
		5	5.3	-	6	-	ns
Recovery Time	t _{REC}	1.5	71	-	81	-	ns
		3.3	8	-	9.1	-	ns
		5	5.7	-	6.5	-	ns
Set-Up Time, P _n to P _L	t _{SU}	1.5	44	-	50	-	ns
		3.3	4.9	-	5.6	-	ns
		5	3.5	-	4	-	ns
Set-Up Time, C _E to CP	t _{SU}	1.5	115	-	131	-	ns
		3.3	12.9	-	14.7	-	ns
		5	9.2	-	10.5	-	ns
Set-Up Time, U/D to CP	t _{SU}	1.5	132	-	150	-	ns
		3.3	14.7	-	16.8	-	ns
		5	10.5	-	12	-	ns
Hold Time, P _n to P _L	t _H	1.5	22	-	25	-	ns
		3.3	2.5	-	2.8	-	ns
		5	2	-	2	-	ns
Hold Time, C _E to CP	t _H	1.5	0	-	0	-	ns
		3.3	0	-	0	-	ns
		5	0	-	0	-	ns
Hold Time, U/D to CP	t _H	1.5	0	-	0	-	ns
		3.3	0	-	0	-	ns
		5	0	-	0	-	ns
ACT TYPES							
Max. Frequency	f _{MAX} (Note 10)	5 (Note 9)	68	-	60	-	MHz
CP Pulse Width	t _W	5	7.3	-	8.3	-	ns
P _L Pulse Width	t _W	5	5.3	-	6	-	ns
Recovery Time	t _{REC}	5	5.7	-	6.5	-	ns
Set-Up Time, P _n to P _L	t _{SU}	5	3.5	-	4	-	ns

CD54AC191, CD54ACT191

Prerequisite For Switching Function (Continued)

PARAMETER	SYMBOL	V _{CC} (V)	-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	
Set-Up Time, \overline{CE} to CP	t _{SU}	5	9.2	-	10.5	-	ns
Set-Up Time, $\overline{U/D}$ to CP	t _{SU}	5	10.5	-	12	-	ns
Hold Time, Pn to \overline{PL}	t _H	5	2	-	2	-	ns
Hold Time, \overline{CE} to CP	t _H	5	0	-	0	-	ns
Hold Time, $\overline{U/D}$ to CP	t _H	5	0	-	0	-	ns

NOTES:

8. 3.3V Min is at 3V.
9. 5V Min is at 4.5V.
10. Applies to non-cascaded operation only. With cascaded counters clock-to-terminal count propagation delays, count enable (\overline{CE})-to-clock set-up times, and count enable (\overline{CE})-to-clock hold times determine max clock frequency. For example, with these AC devices at 85°C and V_{CC} = 5V:.

$$f_{MAX} (CP) = \frac{1}{CP\text{-to-TC prop. delay} + CE\text{-to-CP setup} + CE\text{-to-CP Hold}} = \frac{1}{18.2 + 9.2 + 0} \approx 36\text{MHz}$$

Switching Specifications Input t_r, t_f = 3ns, C_L = 50pF (Worst Case)

PARAMETER	SYMBOL	V _{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay PL to Qn	t _{PLH} , t _{PHL}	1.5	-	-	171	-	-	188	ns
		3.3 (Note 12)	5.4	-	19.1	5.3	-	21	ns
		5 (Note 13)	3.9	-	13.6	3.8	-	15	ns
Propagation Delay Pn to Qn	t _{PLH} , t _{PHL}	1.5	-	-	173	-	-	190	ns
		3.3	5.4	-	19.4	5.3	-	21.3	ns
		5	3.9	-	13.8	3.8	-	15.2	ns
Propagation Delay CP to Qn	t _{PLH} , t _{PHL}	1.5	-	-	182	-	-	200	ns
		3.3	5.8	-	20.4	5.6	-	22.4	ns
		5	4.1	-	14.5	4	-	16	ns
Propagation Delay CP to \overline{RC}	t _{PLH} , t _{PHL}	1.5	-	-	136	-	-	150	ns
		3.3	4.3	-	15.3	4.2	-	16.8	ns
		5	3.1	-	11	3	-	12	ns
Propagation Delay CP to TC	t _{PLH} , t _{PHL}	1.5	-	-	227	-	-	250	ns
		3.3	7.2	-	25.5	7	-	28	ns
		5	5.2	-	18.2	5	-	20	ns
Propagation Delay $\overline{U/D}$ to \overline{RC}	t _{PLH} , t _{PHL}	1.5	-	-	246	-	-	271	ns
		3.3	7.8	-	27.6	7.6	-	30.4	ns
		5	5.6	-	19.7	5.4	-	21.7	ns
Propagation Delay $\overline{U/D}$ to TC	t _{PLH} , t _{PHL}	1.5	-	-	160	-	-	176	ns
		3.3	5.1	-	17.9	4.9	-	19.7	ns
		5	3.6	-	12.8	3.5	-	14.1	ns

CD54AC191, CD54ACT191

Switching Specifications Input t_r , $t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case) (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay CE to RC	t_{PLH} , t_{PHL}	1.5	-	-	137	-	-	151	ns
		3.3	4.4	-	15.4	4.2	-	16.9	ns
		5	3.1	-	11	3	-	12.1	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 14)	-	-	96	-	-	96	-	pF
ACT TYPES									
Propagation Delay \overline{PL} to Qn	t_{PLH} , t_{PHL}	5 (Note 13)	4.2	-	14.8	4.1	-	16.3	ns
Propagation Delay Pn to Qn	t_{PLH} , t_{PHL}	5	3.9	-	13.8	3.8	-	15.2	ns
Propagation Delay CP to Qn	t_{PLH} , t_{PHL}	5	4.1	-	14.5	4	-	16	ns
Propagation Delay CP to RC	t_{PLH} , t_{PHL}	5	3.1	-	10.9	3	-	12	ns
Propagation Delay CP to TC	t_{PLH} , t_{PHL}	5	5.2	-	18.2	5	-	20	ns
Propagation Delay $\overline{U/D}$ to RC	t_{PLH} , t_{PHL}	5	5.6	-	19.7	5.4	-	21.7	ns
Propagation Delay $\overline{U/D}$ to TC	t_{PLH} , t_{PHL}	5	3.8	-	13.5	3.7	-	14.9	ns
Propagation Delay CE to RC	t_{PLH} , t_{PHL}	5	3.3	-	11.5	3.2	-	12.7	ns
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 14)	-	-	96	-	-	96	-	pF

NOTES:

11. Limits tested 100%.
12. 3.3V Min is at 3.6V, Max is at 3V.
13. 5V Min is at 5.5V, Max is at 4.5V
14. C_{PD} is used to determine the dynamic power consumption per package.
 $P_D = C_{PD}V_{CC}^2 f_i + (C_L + V_{CC}^2 f_o)$ where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, V_{CC} = supply voltage.

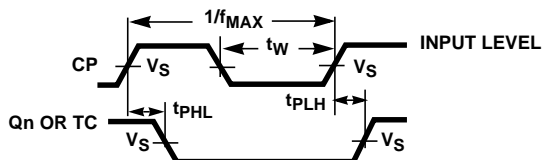


FIGURE 1.

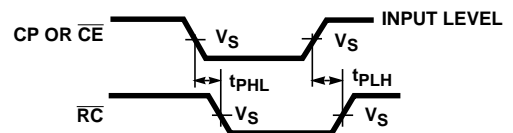


FIGURE 2.

CD54AC191, CD54ACT191

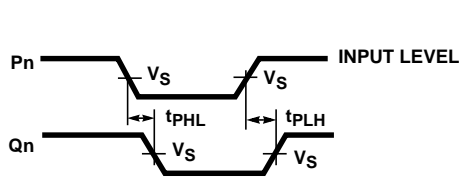


FIGURE 3.

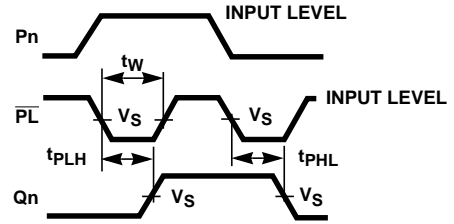


FIGURE 4.

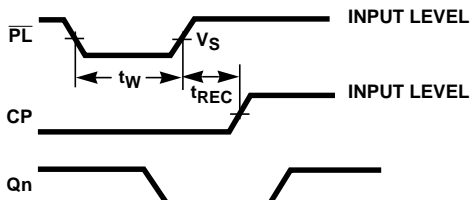
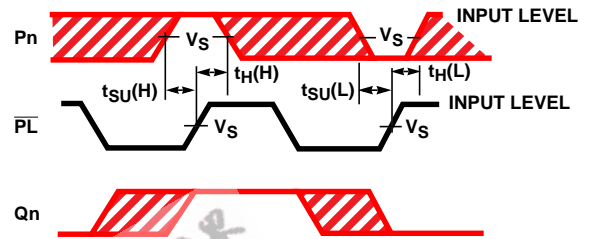


FIGURE 5.



The shaded areas indicate when the input is permitted to change for predictable output performance.

FIGURE 6.

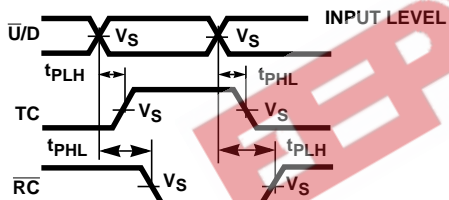


FIGURE 7.

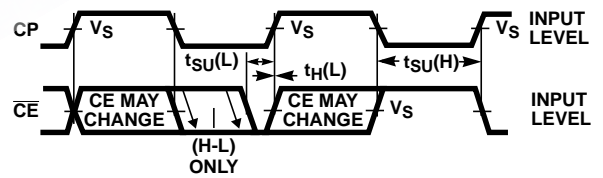
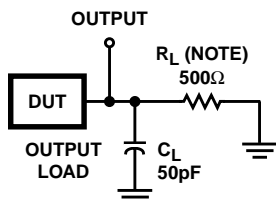


FIGURE 8.

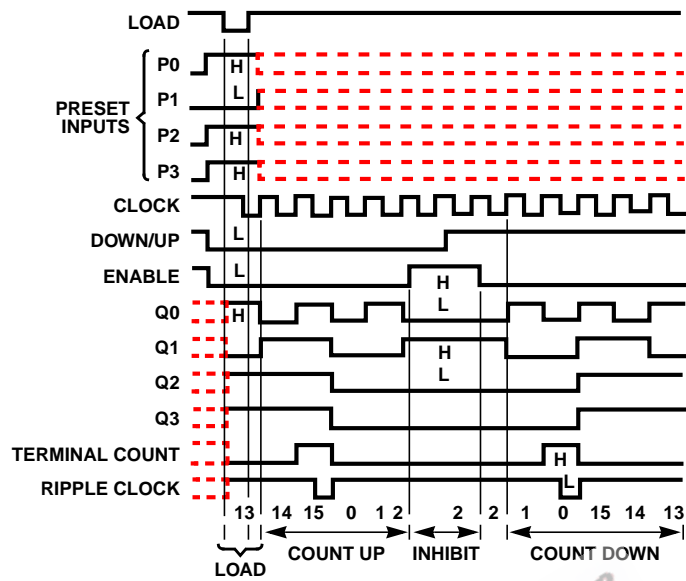


NOTE: For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

	AC	ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

FIGURE 9. PROPAGATION DELAY TIMES

CD54AC191, CD54ACT191



Sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen, zero, one, and two.
3. Inhibit.
4. Count down to one, zero, fifteen, fourteen, and thirteen.

FIGURE 10. CD54AC191 DECODE COUNTERS TYPICAL LOAD, COUNT, AND INHIBIT SEQUENCES

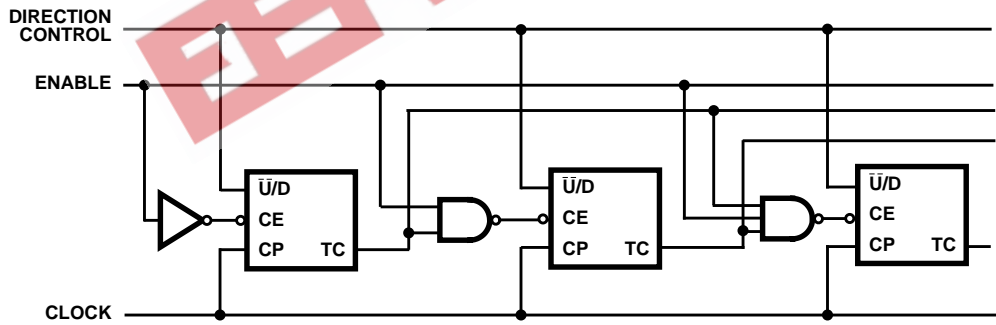


FIGURE 11. SYNCHRONOUS N-STAGE COUNTER WITH PARALLEL GATED TC/RC

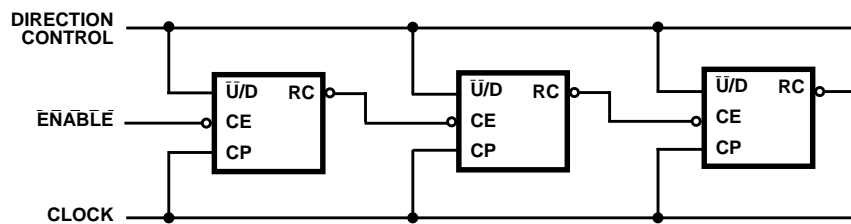


FIGURE 12. SYNCHRONOUS N-STAGE COUNTER USING RIPPLE TC/RC

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