

CD40192BC • CD40193BC Synchronous 4-Bit Up/Down Decade Counter • Synchronous 4-Bit Up/Down Binary Counter

General Description

The CD40192BC and CD40193BC up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The CD40192BC is a BCD counter, while the CD40193BC is a binary counter.

Counting up and counting down is performed by two count inputs, one being held HIGH while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

All inputs are protected against damage due to static discharge by clamps to V_{DD} and V_{SS} .

Features

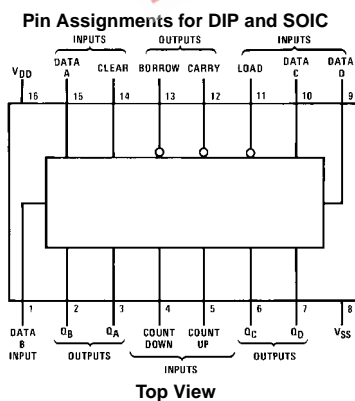
- Wide supply voltage range: 3V to 15V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility: Fan out of 2 driving 74L or 1 driving 74LS
- Carry and borrow outputs for easy expansion to N-bit by cascading
- Asynchronous clear
- Equivalent to: MM74C192 and MM74C193

Ordering Code:

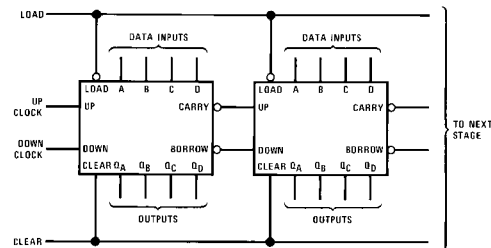
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| CD40192BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| CD40193BCN | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |
| CD40193BCM | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body |

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram

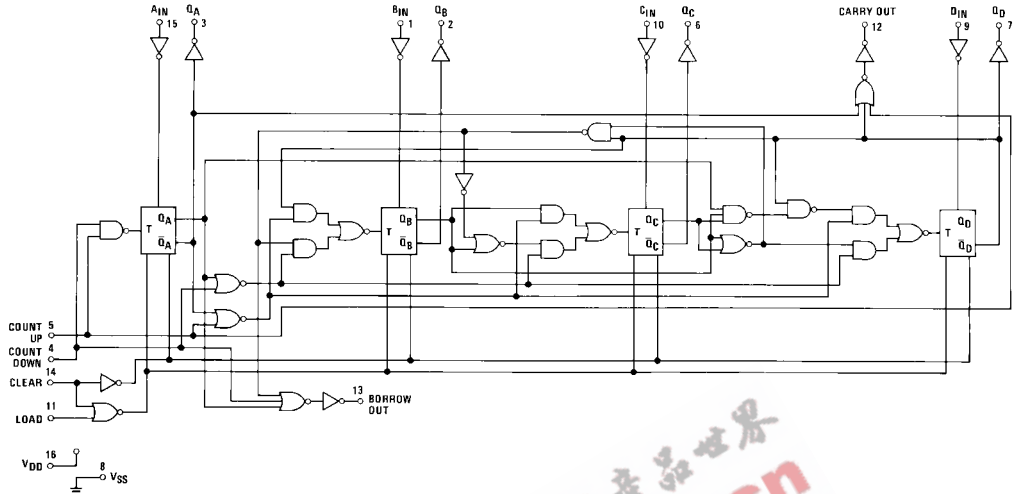


Cascading Packages

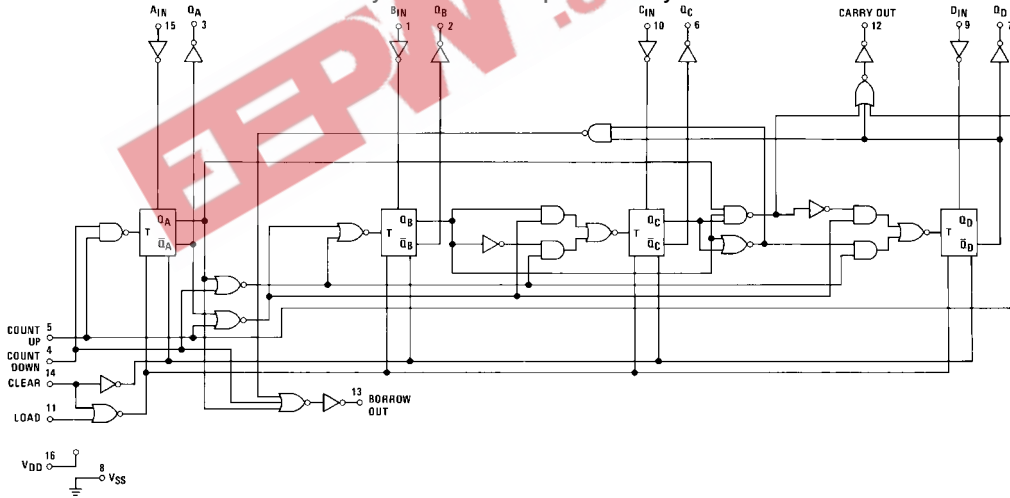


Block Diagrams

CD40192BC Synchronous 4-Bit Up/Down Decade Counter



CD40193BC Synchronous 4-Bit Up/Down Binary Counter



| | | | |
|--|-------------------------------|--|----------------------|
| Absolute Maximum Ratings (Note 1) | | Recommended Operating Conditions (Note 2) | |
| (Note 2) | | | |
| DC Supply Voltage (V_{DD}) | -0.5 to +18 V_{DC} | DC Supply Voltage (V_{DD}) | 3 to 15 V_{DC} |
| Input Voltage (V_{IN}) | -0.5 to $V_{DD} + 0.5 V_{DC}$ | Input Voltage (V_{IN}) | 0 to $V_{DD} V_{DC}$ |
| Storage Temperature Range (T_S) | -65°C to +150°C | Operating Temperature Range (T_A) | -40°C to +85°C |
| Power Dissipation (P_D) | | CD40192BC, CD40193BC | |
| Dual-In-Line | 700 mW | Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The "Recommended Operating Conditions" and Electrical Characteristics tables provide conditions for actual device operation. | |
| Small Outline | 500 mW | Note 2: $V_{SS} = 0V$ unless otherwise specified. | |
| Lead Temperature (T_L) | | | |
| (Soldering, 10 seconds) | 260°C | | |

DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | -40°C | | +25°C | | | +85°C | | Units |
|----------|------------------------------------|---|-------|------|-------|------------|------|-------|------|---------|
| | | | Min | Max | Min | Typ | Max | Min | Max | |
| I_{DD} | Quiescent Device Current | $V_{DD} = 5V, V_{IN} = V_{DD}$ or V_{SS} | | 20 | | | 20 | | 150 | μA |
| | | $V_{DD} = 10V, V_{IN} = V_{DD}$ or V_{SS} | | 40 | | | 40 | | 300 | μA |
| | | $V_{DD} = 15V, V_{IN} = V_{DD}$ or V_{SS} | | 80 | | | 80 | | 600 | μA |
| V_{OL} | LOW Level Output Voltage | $V_{DD} = 5V$ | | 0.05 | | | 0.05 | | 0.05 | V |
| | | $V_{DD} = 10V$ | | 0.05 | | | 0.05 | | 0.05 | V |
| | | $V_{DD} = 15V$ | | 0.05 | | | 0.05 | | 0.05 | V |
| V_{OH} | HIGH Level Output Voltage | $V_{DD} = 5V$ | 4.95 | | 4.95 | | | 4.95 | | V |
| | | $V_{DD} = 10V$ | 9.95 | | 9.95 | | | 9.95 | | V |
| | | $V_{DD} = 15V$ | 14.95 | | 14.95 | | | 14.95 | | V |
| V_{IL} | LOW Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | | 1.5 | | | 1.5 | | 1.5 | V |
| | | $V_{DD} = 10V, V_O = 1V$ or $9V$ | | 3.0 | | | 3.0 | | 3.0 | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | | 4.0 | | | 4.0 | | 4.0 | V |
| V_{IH} | HIGH Level Input Voltage | $V_{DD} = 5V, V_O = 0.5V$ or $4.5V$ | 3.5 | | 3.5 | | | 3.5 | | V |
| | | $V_{DD} = 10V, V_O = 1V$ or $9V$ | 7.0 | | 7.0 | | | 7.0 | | V |
| | | $V_{DD} = 15V, V_O = 1.5V$ or $13.5V$ | 11.0 | | 11.0 | | | 11.0 | | V |
| I_{OL} | LOW Level Output Current (Note 4) | $V_{DD} = 5V, V_O = 0.4V$ | 0.52 | | 0.44 | 0.88 | | 0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 0.5V$ | 1.3 | | 1.1 | 2.25 | | 0.9 | | mA |
| | | $V_{DD} = 15V, V_O = 1.5V$ | 3.6 | | 3.0 | 8.8 | | 2.4 | | mA |
| I_{OH} | HIGH Level Output Current (Note 4) | $V_{DD} = 5V, V_O = 4.6V$ | -0.52 | | -0.44 | -0.88 | | -0.36 | | mA |
| | | $V_{DD} = 10V, V_O = 9.5V$ | -1.3 | | -1.1 | -2.25 | | -0.9 | | mA |
| | | $V_{DD} = 15V, V_O = 13.5V$ | -3.6 | | -3.0 | -8.8 | | -2.4 | | mA |
| I_{IN} | Input Current | $V_{DD} = 15V, V_{IN} = 0V$ | | -0.3 | | -10^{-5} | -0.3 | | -1.0 | μA |
| | | $V_{DD} = 15V, V_{IN} = 15V$ | | 0.3 | | 10^{-5} | 0.3 | | 1.0 | μA |

Note 3: AC Parameters are guaranteed by DC correlated testing.

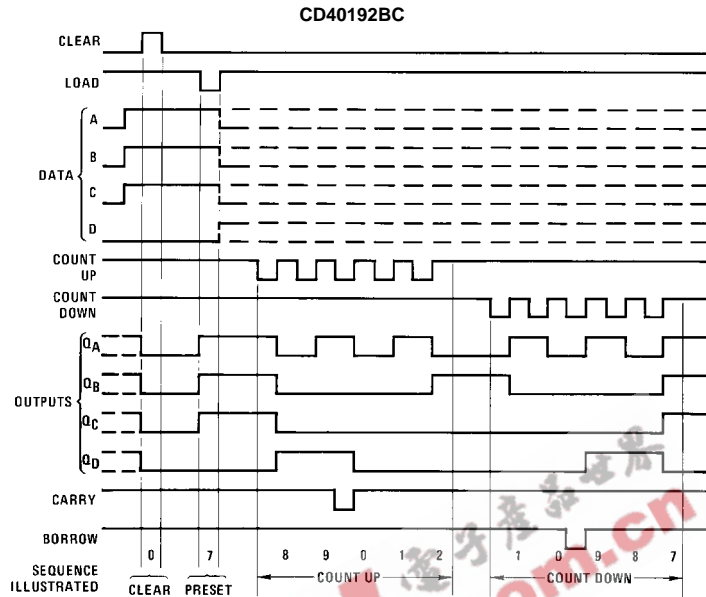
Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics (Note 3) $T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, input $t_r = t_f = 20\text{ ns}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------|---|-----------------------------------|-----|------|-----|---------------|
| t_{PHL} or t_{PLH} | Propagation Delay Time from Count Up or Count Down to Q | $V_{DD} = 5V$ | | 250 | 400 | ns |
| | | $V_{DD} = 10V$ | | 100 | 160 | ns |
| | | $V_{DD} = 15V$ | | 80 | 130 | ns |
| t_{PHL} or t_{PLH} | Propagation Delay Time from Count Up to Carry | $V_{DD} = 5V$ | | 120 | 200 | ns |
| | | $V_{DD} = 10V$ | | 50 | 80 | ns |
| | | $V_{DD} = 15V$ | | 40 | 65 | ns |
| t_{PHL} or t_{PLH} | Propagation Delay Time from Count Down to Borrow | $V_{DD} = 5V$ | | 120 | 200 | ns |
| | | $V_{DD} = 10V$ | | 50 | 80 | ns |
| | | $V_{DD} = 15V$ | | 40 | 65 | ns |
| t_{SU} | Time Prior to Load That Data Must Be Present | $V_{DD} = 5V$ | | 100 | 160 | ns |
| | | $V_{DD} = 10V$ | | 30 | 50 | ns |
| | | $V_{DD} = 15V$ | | 25 | 40 | ns |
| t_{PHL} | Propagation Delay Time from Clear to Q | $V_{DD} = 5V$ | | 130 | 220 | ns |
| | | $V_{DD} = 10V$ | | 60 | 100 | ns |
| | | $V_{DD} = 15V$ | | 50 | 80 | ns |
| t_{PLH} or t_{PHL} | Propagation Delay Time from Load to Q | $V_{DD} = 5V$ | | 300 | 480 | ns |
| | | $V_{DD} = 10V$ | | 120 | 190 | ns |
| | | $V_{DD} = 15V$ | | 95 | 150 | ns |
| t_{TLH} or t_{THL} | Output Transition Time | $V_{DD} = 5V$ | | 100 | 200 | ns |
| | | $V_{DD} = 10V$ | | 50 | 100 | ns |
| | | $V_{DD} = 15V$ | | 40 | 80 | ns |
| f_{CL} | Maximum Count Frequency | $V_{DD} = 5V$ | 2.5 | 4 | | MHz |
| | | $V_{DD} = 10V$ | 6 | 10 | | MHz |
| | | $V_{DD} = 15V$ | 7.5 | 12.5 | | MHz |
| t_{CL} or t_{ICL} | Maximum Count Rise or Fall Time | $V_{DD} = 5V$ | 15 | | | μs |
| | | $V_{DD} = 10V$ | 5 | | | μs |
| | | $V_{DD} = 15V$ | 1 | | | μs |
| t_{WH} , t_{WL} | Minimum Count Pulse Width | $V_{DD} = 5V$ | | 120 | 200 | ns |
| | | $V_{DD} = 10V$ | | 35 | 80 | ns |
| | | $V_{DD} = 15V$ | | 28 | 65 | ns |
| t_{WH} | Minimum Clear Pulse Width | $V_{DD} = 5V$ | | 300 | 480 | ns |
| | | $V_{DD} = 10V$ | | 120 | 190 | ns |
| | | $V_{DD} = 15V$ | | 95 | 150 | ns |
| t_{WL} | Minimum Load Pulse Width | $V_{DD} = 5V$ | | 100 | 160 | ns |
| | | $V_{DD} = 10V$ | | 40 | 65 | ns |
| | | $V_{DD} = 15V$ | | 32 | 55 | ns |
| C_{IN} | Average Input Capacitance | Load and Data Inputs (A,B,C,D) | | 5 | 7.5 | pF |
| | | Count Up, Count Down and Clear | | 10 | 15 | pF |
| C_{PD} | Power Dissipation Capacity | (Note 5) | | 100 | | pF |

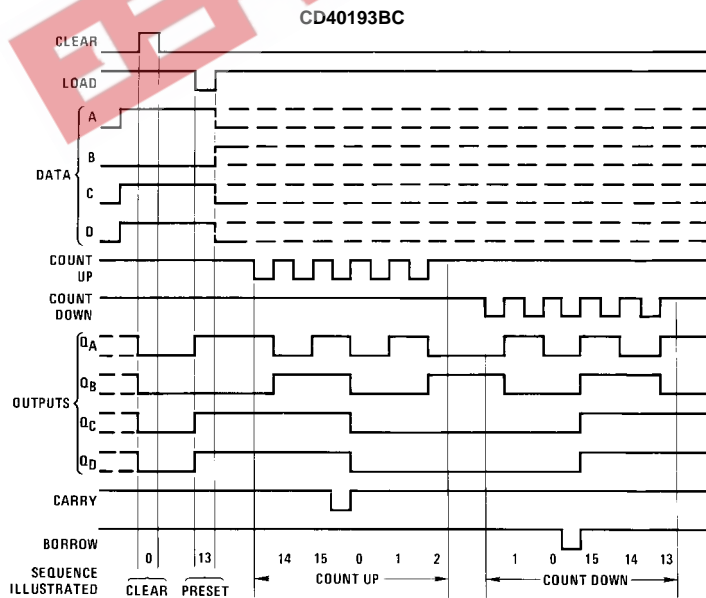
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see Family Characteristics application note, AN-90.

Timing Diagrams



Sequence:

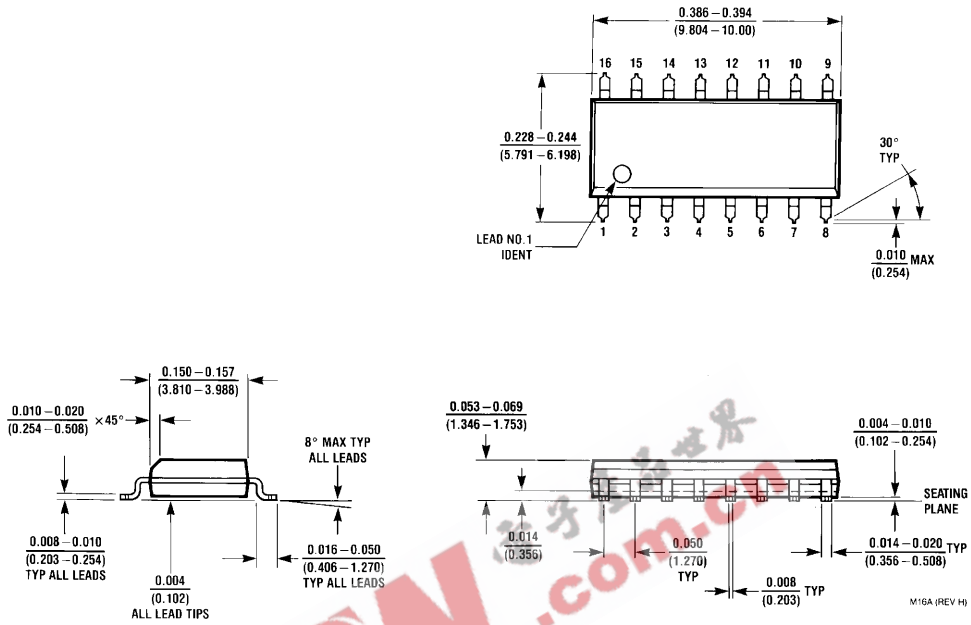
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.



Sequence:

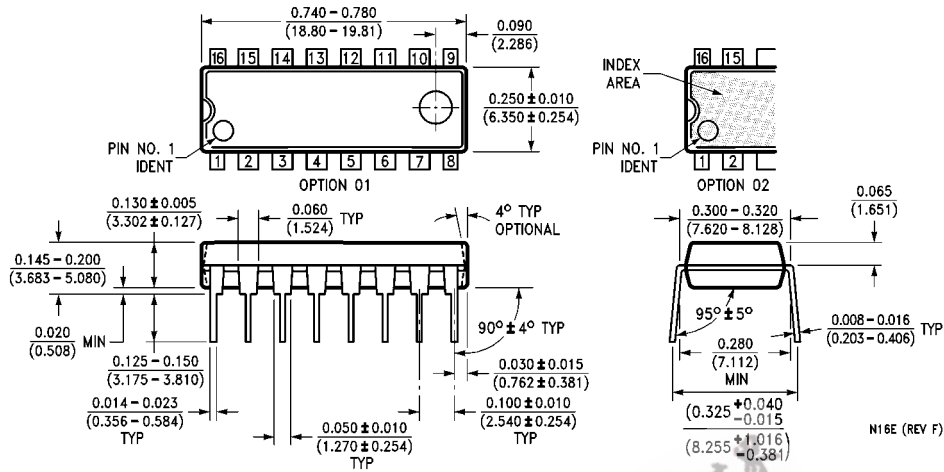
1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one and two.
4. Count down to one, zero, borrow, fifteen, fourteen and thirteen.

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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