

# CD54AC193/3A CD54ACT193/3A

## Pre-settable Synchronous 4-Bit Binary Up/Down Counter with Reset

**COMPLETE DATA SHEET  
COMING SOON!**

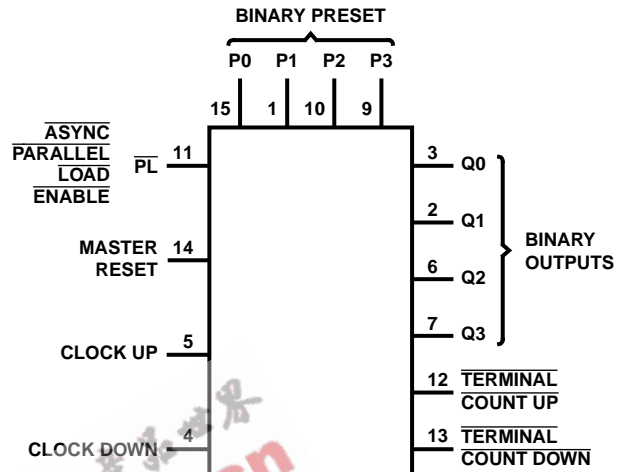
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### Description

The CD54AC193/3A and CD54ACT193/3A are up/down binary counters with separate up/down clocks. These devices utilize the Harris Advanced CMOS Logic technology. Presetting the counter to the number on preset data inputs (P0-P3) is accomplished by a LOW asynchronous parallel load input ( $\overline{PL}$ ). The counter is incremented on the LOW-to-HIGH transition of the Clock-Up input (and a HIGH level on the Clock-Down input) and decremented on the LOW-to-HIGH transition of the Clock-Down input (and a HIGH level on the Clock-Up input). A HIGH level on the Reset input overrides any other input to clear the counter to its zero state. The  $\overline{TCU}$  (carry) output goes LOW half a clock period before the zero count is reached and returns to a HIGH level at the zero count. The  $\overline{TCD}$  (borrow) output in the count down mode likewise goes LOW half a clock period before the maximum count (15 counts) and returns to HIGH at the maximum count. Cascading is effected by connecting the  $\overline{TCU}$  and  $\overline{TCD}$  outputs of a less significant counter to the Clock-Up and Clock-Down inputs, respectively, of the next most significant counter.

The CD54AC193/3A and CD54ACT193/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).s

### Functional Diagram



ACT INPUT LOAD TABLE

| INPUT                    | UNIT LOAD (NOTE 1) |
|--------------------------|--------------------|
| P0 - P3, $\overline{PL}$ | 0.75               |
| MR, CPU, CPD             | 0.85               |

NOTE:

- Unit load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications Table, e.g., 2.4mA Max at +25°C.

### Absolute Maximum Ratings

DC Supply Voltage,  $V_{CC}$  ..... -0.5V to +6V  
 DC Input Diode Current,  $I_{IK}$   
 For  $V_I < -0.5V$  or  $V_I > V_{CC} + 0.5V$  .....  $\pm 20mA$   
 DC Output Diode Current,  $I_{OK}$   
 For  $V_O < -0.5V$  or  $V_O > V_{CC} + 0.5V$  .....  $\pm 50mA$   
 DC Output Source or Sink Current, Per Output Pin,  $I_O$   
 For  $V_O > -0.5V$  or  $V_O < V_{CC} + 0.5V$  .....  $\pm 50mA$   
 DC  $V_{CC}$  or GND Current,  $I_{CC}$  or  $I_{GND}$   
 For Up to 4 Outputs Per Device, Add  $\pm 25mA$  For Each  
 Additional Output .....  $\pm 100mA$

Power Dissipation Per Package,  $P_D$   
 $T_A = -55^\circ C$  to  $+100^\circ C$  (Package F) ..... 500mW  
 $T_A = +100^\circ C$  to  $+125^\circ C$  (Package F) ..... Derate Linearly at  
 8mW/ $^\circ C$  to 300mW  
 Operating Temperature Range,  $T_A$   
 Package Type F .....  $-55^\circ C$  to  $+125^\circ C$   
 Storage Temperature,  $T_{STG}$  .....  $-65^\circ C$  to  $+150^\circ C$   
 Lead Temperature (During Soldering)  
 At Distance 1/16in.  $\pm$  1/32in. (1.59mm  $\pm$  0.79mm)  
 From Case For 10s Max .....  $+265^\circ C$   
 Unit Inserted Into a PC Board (Min Thickness 1/16in., 1.59mm)  
 With Solder Contacting Lead Tips Only .....  $+300^\circ C$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### Recommended Operating Conditions

Supply Voltage Range,  $V_{CC}$   
 Unless Otherwise Specified, All Voltages Referenced to GND  
 $T_A$  = Full Package Temperature Range  
 CD54AC Types ..... 1.5V to 5.5V  
 CD54ACT Types ..... 4.5V to 5.5V  
 DC Input or Output Voltage,  $V_I$ ,  $V_O$  ..... 0V to  $V_{CC}$

Operating Temperature,  $T_A$  .....  $-55^\circ C$  to  $+125^\circ C$   
 Input Rise and Fall Slew Rate,  $dt/dv$   
 at 1.5V to 3V (AC Types) ..... 0ns/V to 50ns/V  
 at 3.6V to 5.5V (AC Types) ..... 0ns/V to 20ns/V  
 at 4.5V to 5.5V (AC Types) ..... 0ns/V to 10ns/V