National Semiconductor

54LS95B/DM74LS95B
4-Bit Right/Left Shift Register

General Description

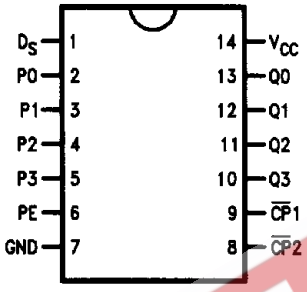
The 'LS95B is a 4-bit shift register with serial and parallel synchronous operating modes. The serial shift right and parallel load are activated by separate clock inputs which are selected by a mode control input. The data is transferred from the serial or parallel D inputs to the Q outputs synchronous with the HIGH-to-LOW transition of the appropriate clock input.

Features

- Synchronous, expandable shift right
- Synchronous shift left capability
- Synchronous parallel load
- Separate shift and load clock inputs

Connection Diagram

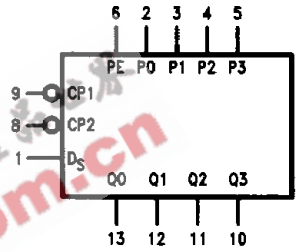
Dual-In-Line Package



TL/F/10175–1

Order Number 54LS95BDMQB, 54LS95BFMQB, DM74LS95BM or DM74LS95BN
See NS Package Number J14A, M14A, N14A or W14B

Logic Symbol



TL/F/10175–2

VCC = Pin 14
GND = Pin 7

Pin Names	Description
$\overline{CP}1$	Serial Clock Input (Active Falling Edge)
$\overline{CP}2$	Parallel Clock Input (Active Falling Edge)
D_S	Serial Data Input
P0–P3	Parallel Data Inputs
PE	Parallel Enable Input (Active HIGH)
Q0–Q3	Parallel Outputs

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions V_{CC} = +5.0V, T_A = +25°C

Symbol	Parameter	54LS95			DM74LS95			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C
t_s (H) t_s (L)	Setup Time HIGH or LOW D_S or Pn to $\overline{CP}$n	20 20			20 20			ns
t_h (H) t_h (L)	Hold Time HIGH or LOW D_S or Pn to $\overline{CP}$n	10 10			10 10			ns
t_w (H)	$\overline{CP}$n Pulse Width HIGH	20			20			ns
t_{en} (L)	Enable Time LOW, PE to $\overline{CP}$1	25			25			ns
t_{inh} (H)	Inhibit Time HIGH, PE to $\overline{CP}$1	20			20			ns
t_{en} (H)	Enable Time HIGH, PE to $\overline{CP}$2	25			25			ns
t_{inh} (L)	Inhibit Time LOW, PE to $\overline{CP}$2	20			20			ns

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 10V				0.1	mA
	PE Input	V_{CC} = Max, V_I = 10V				200	µA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
	PE Input	V_{CC} = Max, V_I = 2.7V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
	PE Input	V_{CC} = Max, V_I = 0.4V				−0.8	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max				21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics

V_{CC} = +5.0V, T_A = +25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		27	ns
f_{max}	Maximum Shift Frequency	30		MHz

Functional Description

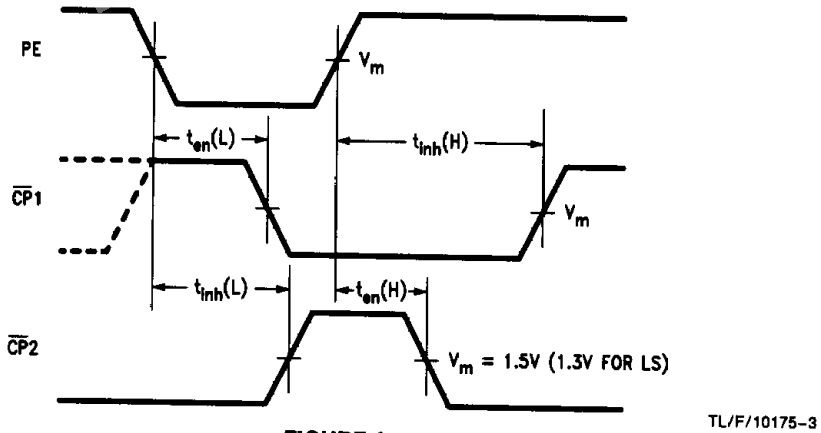
The '95 is a 4-bit shift register with serial and parallel synchronous operating modes. It has a Serial (D_S) and four Parallel (P0–P3) Data inputs and four Parallel Data outputs (Q0–Q3). The serial or parallel mode of operation is controlled by a Parallel Enable input (PE) and two Clock inputs, $\overline{CP}1$ and $\overline{CP}2$. The serial (right-shift) or parallel data transfers occur synchronous with the HIGH-to-LOW transition of the selected clock input.

When PE is HIGH, $\overline{CP}2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}2$ transfers parallel data from the P0–P3 inputs to the Q0–Q3 outputs. When PE is LOW, $\overline{CP}1$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}1$ transfers the data from Serial input (D_S) to Q0 and shifts the data in Q0 to Q1, Q1 to Q2, and Q2 to Q3 respectively (right-shift). A left-shift is accomplished by externally connecting Q3 to P2, Q2 to P1, and Q1 to P0, and operating the '95 in the parallel mode (PE = HIGH). For normal operation, PE should only change states when both Clock inputs are LOW. However, changing PE from LOW to HIGH while $\overline{CP}2$ is HIGH, or changing PE from HIGH to LOW while $\overline{CP}1$ is HIGH and $\overline{CP}2$ is LOW will not cause any changes on the register outputs.

Mode Select Table

Operating Mode	Inputs					Outputs			
	PE	$\overline{CP}1$	$\overline{CP}2$	D_S	Pn	Q0	Q1	Q2	Q3
Shift	L	↘	X	l	X	L	q0	q1	q2
	L	↘	X	h	X	H	q0	q1	q2
Parallel Load	H	X	↘	X	pn	p0	p1	p2	p3
Mode Change	↘	L	L	X	X	No Change			
	↗	L	L	X	X	No Change			
	↘	H	L	X	X	No Change			
	↗	H		X	X	Undetermined			
	↘	L	H	X	X	Undetermined			
	↗	L	H	X	X	No Change			
	↘	H	H	X	X	Undetermined			
	↗	H	H	X	X	No Change			

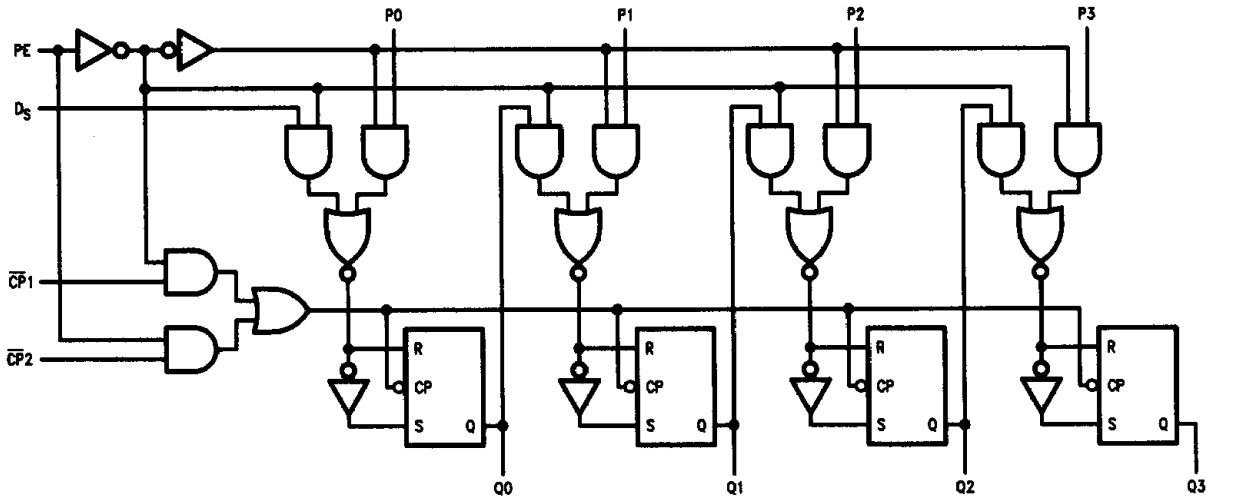
l = LOW Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
h = HIGH Voltage Level one set-up time prior to the HIGH-to-LOW clock transition.
pn = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH-to-LOW clock transition.
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



TL/F/10175–3

FIGURE A

Logic Diagram



TL/F/10175–4