Data Sheet | July 1999 | File Number 4621.1

CMOS Dual 4-Stage Static Shift Register With Serial Input/Parallel Output

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

CD4015BT consists of two identical, independent, 4-stage serial-input/parallel output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015BT, or to more than 8 stages using additional CD4015BT's is possible.

Specifications

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the CD4015BT are contained in SMD 5962-96624. A "hot-link" is provided from our website for downloading**.**
www.intersil.com/spacedefense/newsafclasst.asp

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.
www.intersil.com/quality/manuals.asp

Ordering Information

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (^oC)
5962R9662401TEC	CD4015BDTR	-55 to 125
5962R9662401TXC	CD4015BKTR	-55 to 125

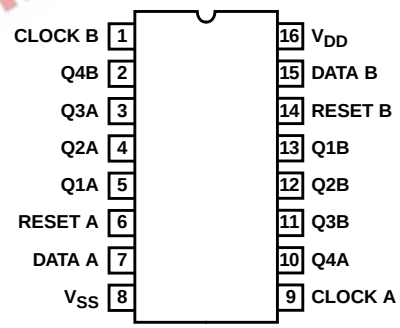
NOTE: ***Minimum order quantity for -T is 150 units through distribution, or 450 units direct.***

Features

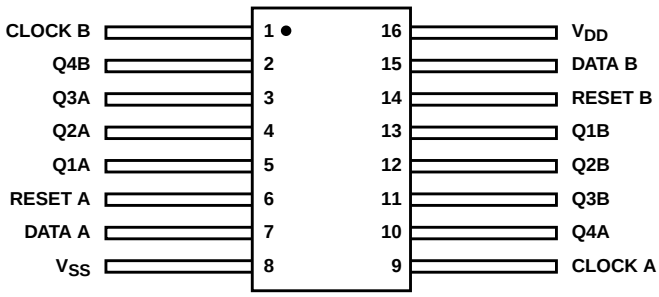
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose (γ) 1 x 10^5 RAD(Si)
  - SEP Effective LET > 75 MEV/gm/cm^2
- Medium Speed Operation 12MHz (typ.) Clock Rate at V_{DD} - V_{SS} = 10V
- Fully Static Operation
- 8 Master-Slave Flip-Flops Plus Input and Output Buffering
- 100% Tested For Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics

Pinouts

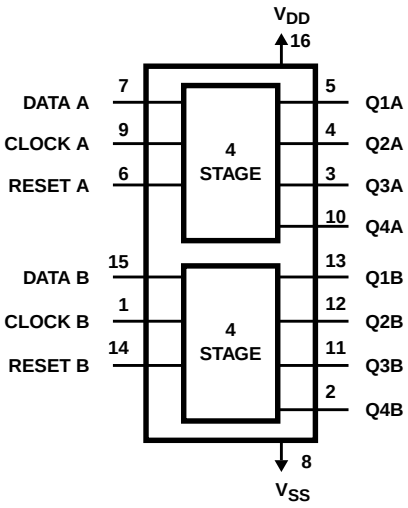
CD4015BT (SBDIP), CDIP2-T16
TOP VIEW



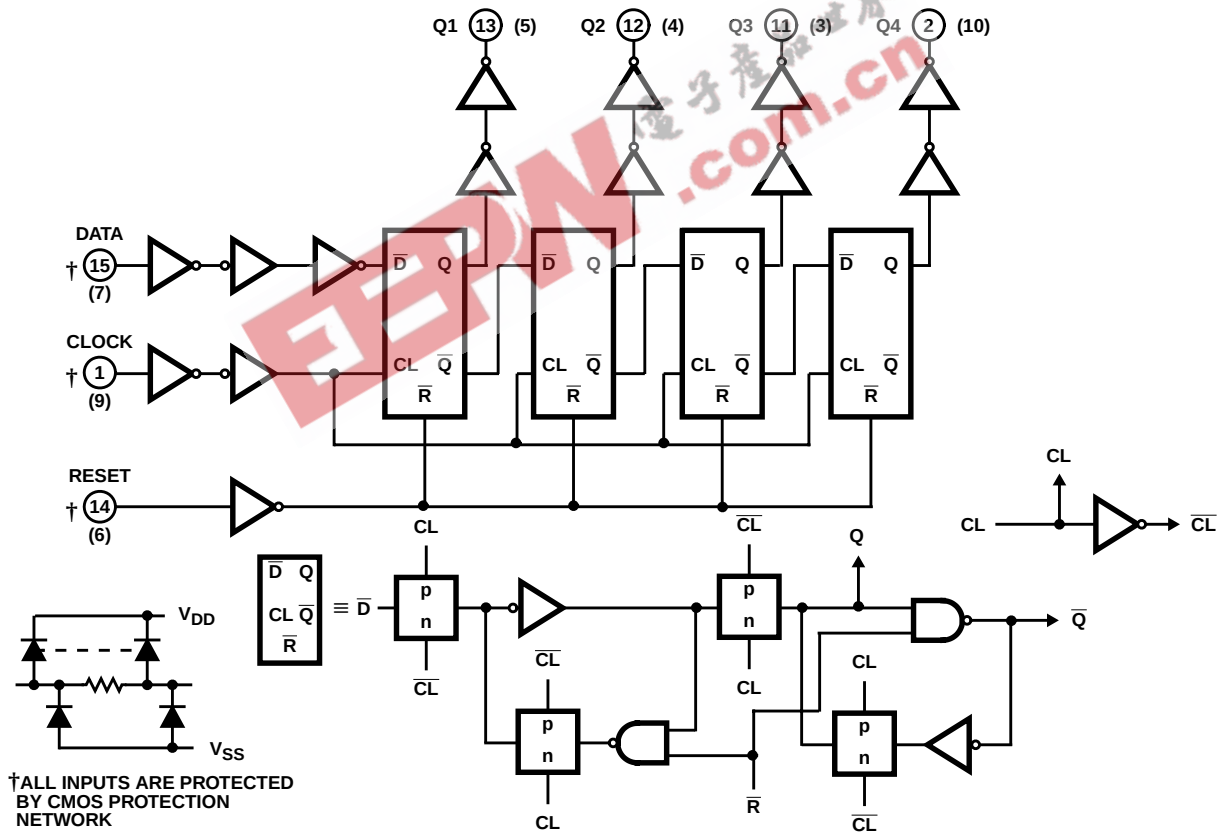
CD4015BT (FLATPACK), CDFP4-F16
TOP VIEW



Functional Diagram



Logic Diagram



TRUTH TABLE

CL	D	R	Q1	Qn	
↑	0	0	0	Qn-1	
↑	1	0	1	Qn-1	
↓	X	0	Q1	Qn	(No Change)
X	X	1	0	0	

X = Don't care Case

Die Characteristics

DIE DIMENSIONS:

(2032µm x 2489µm x 533µm ±25.4µm)

80 x 98 x 21mils ±1mil

METALLIZATION:

Type: Al

Thickness: 12.5kÅ ±1.5kÅ

SUBSTRATE POTENTIAL:

Leave Floating or Tie to $V_{DD;}$ Bond Pad #16 (V_{DD}) First

BACKSIDE FINISH:

Silicon

PASSIVATION:

Type: Phosphorus Doped Silox (S_iO_2)

Thickness: 13kÅ ±2.6kÅ

WORST CASE CURRENT DENSITY:

< 2.0e5 A/cm^2

TRANSISTOR COUNT:

60

PROCESS:

Bulk CMOS

Metallization Mask Layout

CD4015BT