

**CMOS Dual 4-Stage Static Shift Register With Serial Input/Parallel Output**

Intersil's Satellite Applications Flow™ (SAF) devices are fully tested and guaranteed to 100kRAD total dose. These QML Class T devices are processed to a standard flow intended to meet the cost and shorter lead-time needs of large volume satellite manufacturers, while maintaining a high level of reliability.

CD4015BT consists of two identical, independent, 4-stage serial-input/parallel output registers. Each register has independent CLOCK and RESET inputs as well as a single serial DATA input. "Q" outputs are available from each of the four stages on both registers. All register stages are D type, master-slave flip-flops. The logic level present at the DATA input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015BT, or to more than 8 stages using additional CD4015BT's is possible.

**Specifications**

Specifications for Rad Hard QML devices are controlled by the Defense Supply Center in Columbus (DSCC). The SMD numbers listed below must be used when ordering.

**Detailed Electrical Specifications for the CD4015BT are contained in SMD 5962-96624.** A "hot-link" is provided from our website for downloading.

[www.intersil.com/spacedefense/newsafclasst.asp](http://www.intersil.com/spacedefense/newsafclasst.asp)

Intersil's Quality Management Plan (QM Plan), listing all Class T screening operations, is also available on our website.

[www.intersil.com/quality/manuals.asp](http://www.intersil.com/quality/manuals.asp)

**Ordering Information**

ORDERING NUMBER	PART NUMBER	TEMP. RANGE (°C)
5962R9662401TEC	CD4015BDTR	-55 to 125
5962R9662401TXC	CD4015BKTR	-55 to 125

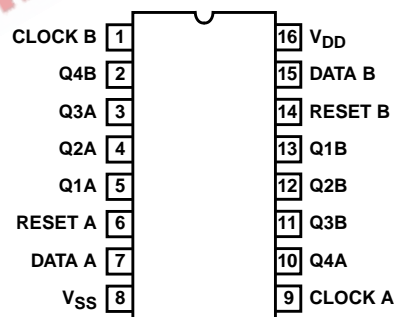
NOTE: **Minimum order quantity for -T is 150 units through distribution, or 450 units direct.**

**Features**

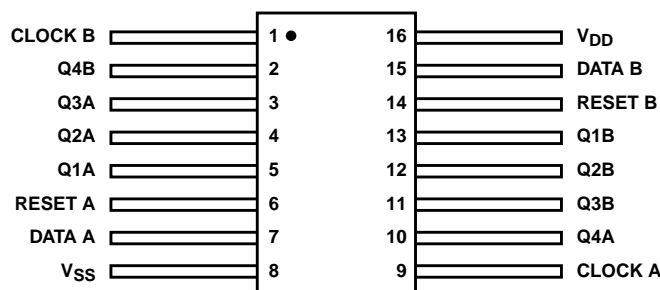
- QML Class T, Per MIL-PRF-38535
- Radiation Performance
  - Gamma Dose ( $\gamma$ )  $1 \times 10^5$  RAD(Si)
  - SEP Effective LET  $> 75$  MEV/gm/cm<sup>2</sup>
- Medium Speed Operation 12MHz (typ.) Clock Rate at V<sub>DD</sub> - V<sub>SS</sub> = 10V
- Fully Static Operation
- 8 Master-Slave Flip-Flops Plus Input and Output Buffering
- 100% Tested For Quiescent Current at 20V
- 5V, 10V and 15V Parametric Ratings
- Standardized Symmetrical Output Characteristics

**Pinouts**

CD4015BT (SBDIP), CDIP2-T16  
TOP VIEW

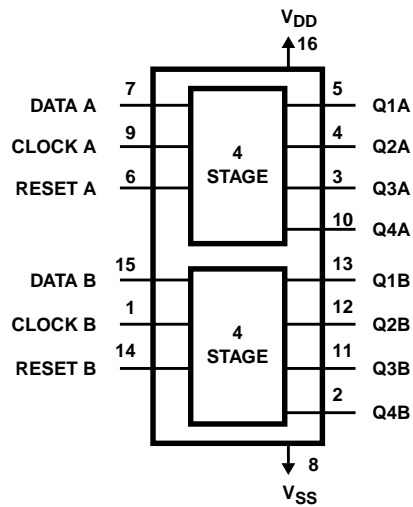


CD4015BT (FLATPACK), CDFP4-F16  
TOP VIEW

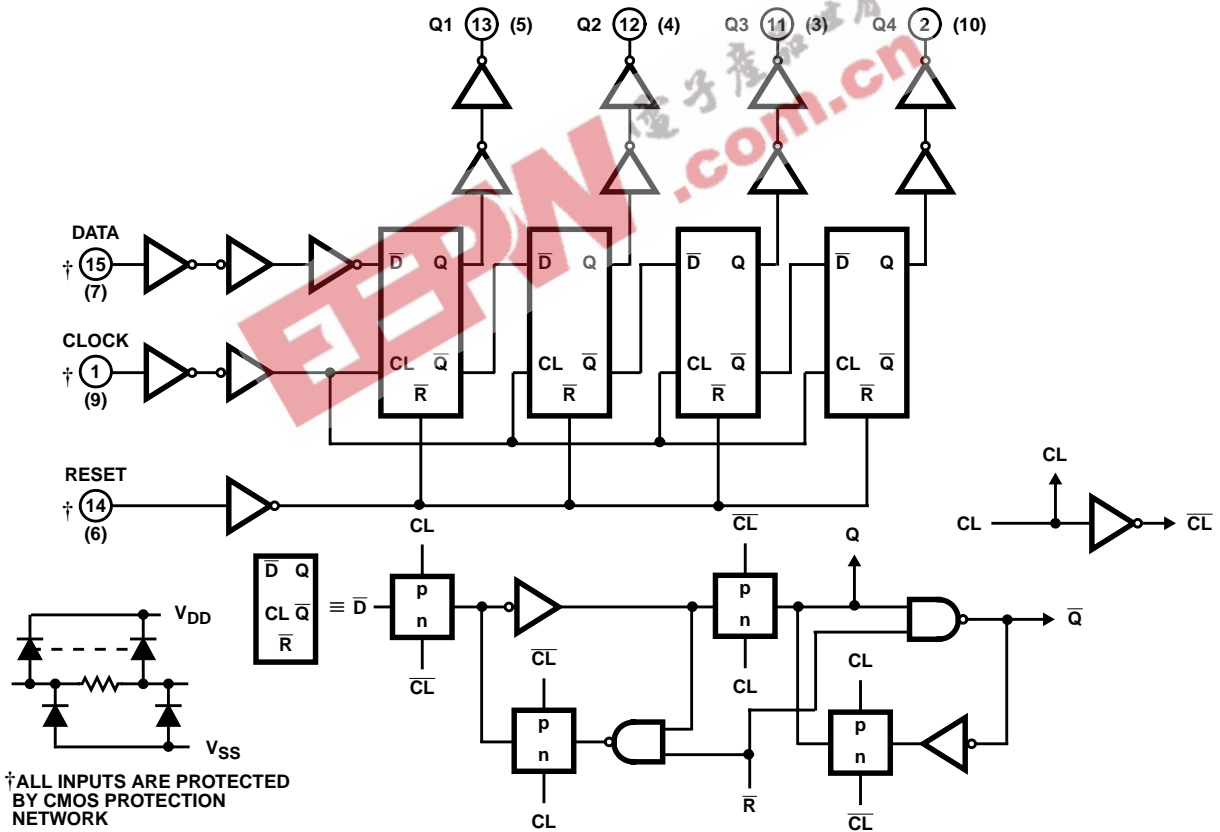


# CD4015BT

## Functional Diagram



## Logic Diagram



TRUTH TABLE

CL	D	R	Q1	Qn
	0	0	0	Qn-1
	1	0	1	Qn-1
	X	0	Q1	Qn
X	X	1	0	0

(No Change)

X = Don't care Case

## CD4015BT

### Die Characteristics

#### DIE DIMENSIONS:

(2032 $\mu\text{m}$  x 2489 $\mu\text{m}$  x 533 $\mu\text{m}$   $\pm$ 25.4 $\mu\text{m}$ )

80 x 98 x 21mils  $\pm$ 1mil

#### METALLIZATION:

Type: Al

Thickness: 12.5k $\text{\AA}$   $\pm$ 1.5k $\text{\AA}$

#### SUBSTRATE POTENTIAL:

Leave Floating or Tie to  $V_{DD}$ ; Bond Pad #16 ( $V_{DD}$ ) First

#### BACKSIDE FINISH:

Silicon

#### PASSIVATION:

Type: Phosphorus Doped Silox ( $\text{SiO}_2$ )

Thickness: 13k $\text{\AA}$   $\pm$ 2.6k $\text{\AA}$

#### WORST CASE CURRENT DENSITY:

$< 2.0\text{e}5 \text{ A/cm}^2$

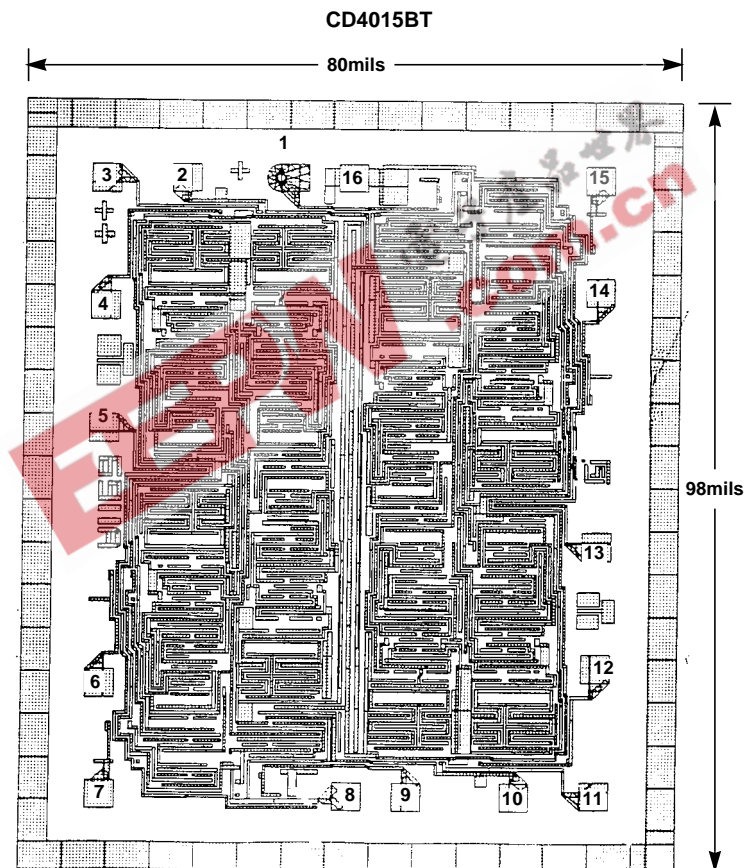
#### TRANSISTOR COUNT:

60

#### PROCESS:

Bulk CMOS

### Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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