

FSTD3125 4-Bit Bus Switch with Level Shifting

General Description

The Fairchild Switch FSTD3125 provides four high-speed CMOS TTL-compatible bus switches. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. A diode to V_{CC} has been integrated into the circuit to allow for level shifting between 5V inputs and 3.3V outputs.

The device is organized as four 1-bit switches with separate \overline{OE} inputs. When \overline{OE} is LOW, the switch is ON and Port A is connected to Port B. When \overline{OE} is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

- 4Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- TruTranslation™ voltage translation from 5.0V inputs to 3.3V outputs

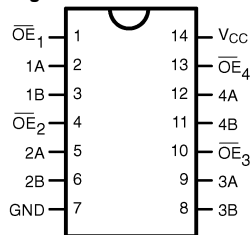
Ordering Code:

| Order Number | Package Number | Package Description |
|----------------|----------------|---|
| FSTD3125M | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| FSTD3125QSC | MQA16 | 16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide |
| FSTD3125MTC | MTC14 | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| FSTD3125MTC_NL | MTC14 | Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |

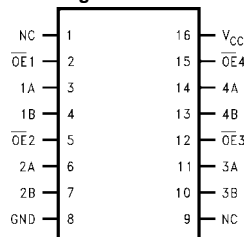
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagrams

Pin Assignment for SOIC and TSSOP



Pin Assignment for QSOP



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Pin Descriptions

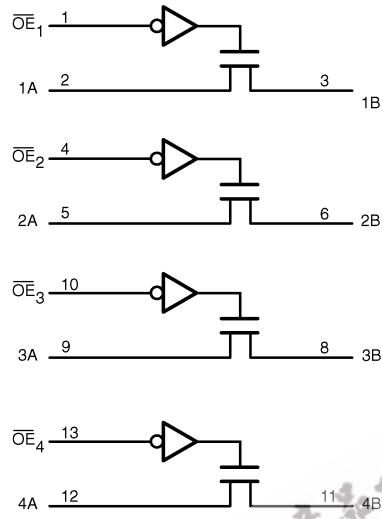
| Pin Name | Description |
|--|--------------------|
| $\overline{OE}_1, \overline{OE}_2, \overline{OE}_3, \overline{OE}_4$ | Bus Switch Enables |
| 1A, 2A, 3A, 4A | Bus A |
| 1B, 2B, 3B, 4B | Bus B |
| NC | Not Connected |

Truth Table

| Inputs | Inputs/Outputs |
|-----------------|----------------|
| \overline{OE} | A, B |
| L | A = B |
| H | Z |

FSTD3125

Logic Diagram



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Absolute Maximum Ratings (Note 1)

| | |
|---|------------------|
| Supply Voltage (V_{CC}) | -0.5V to +7.0V |
| DC Switch Voltage (V_S) | -0.5V to +7.0V |
| DC Input Voltage (V_{IN}) (Note 2) | -0.5V to +7.0V |
| DC Input Diode Current (I_{IK}) $V_{IN} < 0V$ | -50 mA |
| DC Output (I_{OUT}) Sink Current | 128 mA |
| DC V_{CC}/GND Current (I_{CC}/I_{GND}) | +/- 100 mA |
| Storage Temperature Range (T_{STG}) | -65°C to +150 °C |

Recommended Operating Conditions (Note 3)

| | |
|--|------------------|
| Power Supply Operating (V_{CC}) | 4.5V to 5.5V |
| Input Voltage (V_{IN}) | 0V to 5.5V |
| Output Voltage (V_{OUT}) | 0V to 5.5V |
| Input Rise and Fall Time (t_r, t_f) | |
| Switch Control Input | 0 ns/V to 5 ns/V |
| Switch I/O | 0 ns/V to DC |
| Free Air Operating Temperature (T_A) | -40 °C to +85 °C |

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}$ | | | Units | Conditions |
|-----------------|----------------------------------|-----------------|---|-----------------|-----------|---------------|---|
| | | | Min | Typ (Note 4) | Max | | |
| V_{IK} | Clamp Diode Voltage | 4.5 | | | -1.2 | V | $I_{IN} = -18\text{ mA}$ |
| V_{IH} | HIGH Level Input Voltage | 4.5-5.5 | 2.0 | | | V | |
| V_{OH} | HIGH Level | 4.0-5.5 | Figure 3 | | | V | |
| V_{IL} | LOW Level Input Voltage | 4.5-5.5 | | | 0.8 | V | |
| I_I | Input Leakage Current | 5.5 | | | ± 1.0 | μA | $0 \leq V_{IN} \leq 5.5V$ |
| | | 0 | | | 10 | μA | $V_{IN} = 5.5V$ |
| I_{OZ} | OFF-STATE Leakage Current | 5.5 | | | ± 1.0 | μA | $0 \leq A, B \leq V_{CC}$ |
| R_{ON} | Switch On Resistance (Note 5) | 4.5 | | 4 | 7 | Ω | $V_{IN} = 0V, I_{IN} = 64\text{ mA}$ |
| | | 4.5 | | 4 | 7 | Ω | $V_{IN} = 0V, I_{IN} = 30\text{ mA}$ |
| | | 4.5 | | 35 | 50 | Ω | $V_{IN} = 2.4V, I_{IN} = 1.5\text{ mA}$ |
| I_{CC} | Quiescent Supply Current | 5.5 | | | 1.5 | mA | $OE_1 = OE_2 = GND$ $V_{IN} = V_{CC}$ or $GND, I_{OUT} = 0$ |
| | | | | | 10 | μA | $OE_1 = OE_2 = V_{CC}$ $V_{IN} = V_{CC}$ or $GND, I_{OUT} = 0$ |
| ΔI_{CC} | Increase in I_{CC} per Input | 5.5 | | | 2.5 | mA | One Input at 3.4V. Other Inputs at V_{CC} or GND |

Note 4: Typical values are at $V_{CC} = 5.0V$ and $T_A = +25^\circ\text{C}$

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

| Symbol | Parameter | T _A = -40 °C to +85 °C, C _L = 50pF, R _U = R _D = 500Ω | | Units | Conditions | Figure Number |
|-------------------------------------|--|---|------|-------|--|---------------|
| | | V _{CC} = 4.5 - 5.5V | | | | |
| | | Min | Max | | | |
| t _{PHL} , t _{PLH} | Propagation Delay Bus to Bus (Note 6) | | 0.25 | ns | V _I = OPEN | Figures 1, 2 |
| t _{PZH} , t _{PZL} | Output Enable Time | 1.0 | 6.1 | ns | V _I = 7V for t _{PZL} V _I = OPEN for t _{PZH} | Figures 1, 2 |
| t _{PHZ} , t _{PLZ} | Output Disable Time | 1.5 | 6.4 | ns | V _I = 7V for t _{PLZ} V _I = OPEN for t _{PHZ} | Figures 1, 2 |

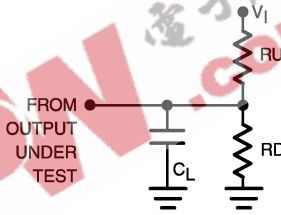
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

| Symbol | Parameter | Typ | Max | Units | Conditions |
|------------------|-------------------------------|-----|-----|-------|--|
| C _{IN} | Control Pin Input Capacitance | 3 | | pF | V _{CC} = 5.0V |
| C _{I/O} | Input/Output Capacitance | 6 | | pF | V _{CC} , \overline{OE} = 5.0V |

Note 7: T_A = +25°C, f = 1 MHz. Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500ns

FIGURE 1. AC Test Circuit

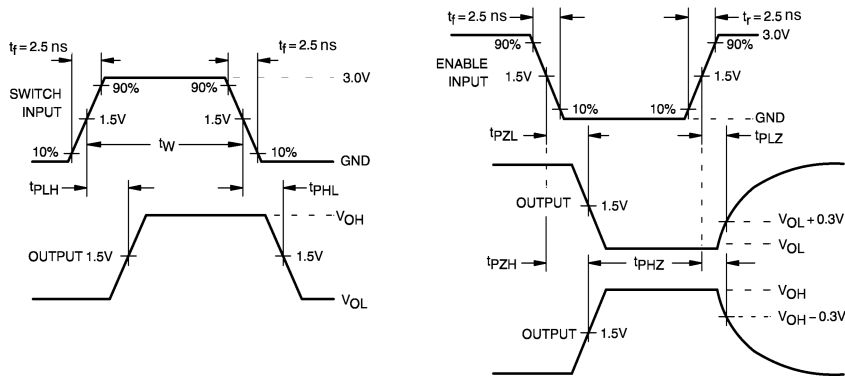
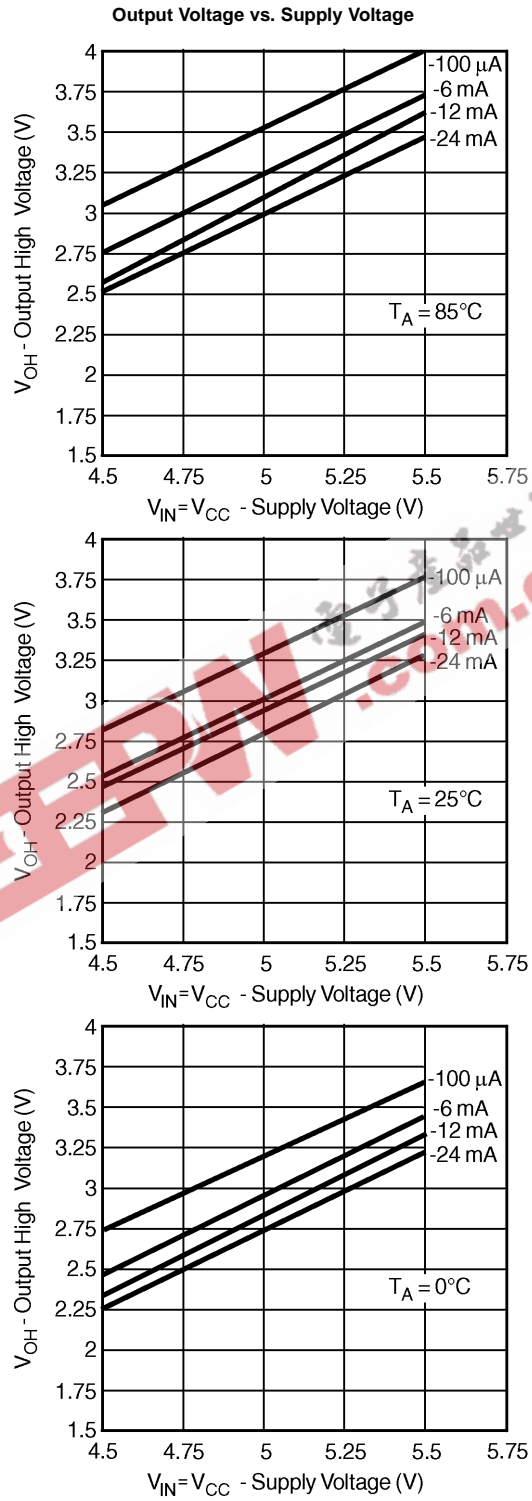
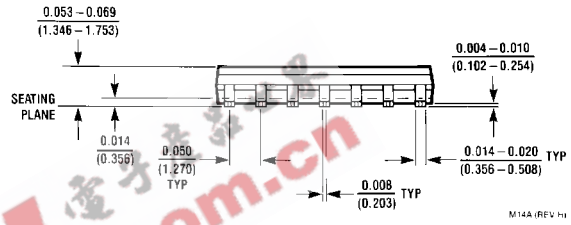
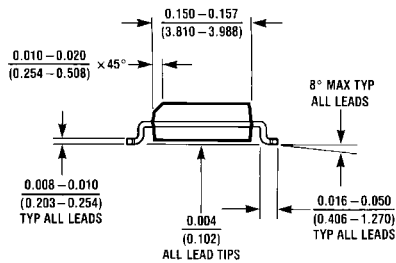
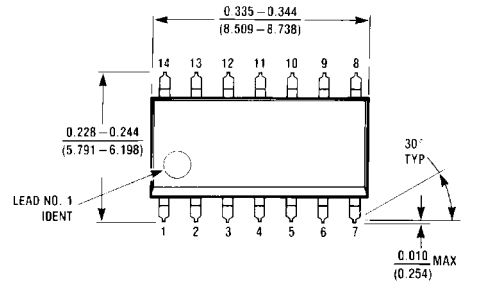


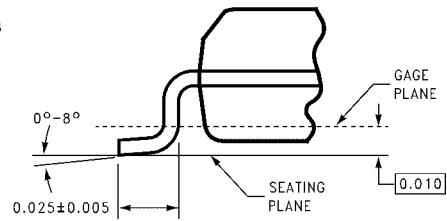
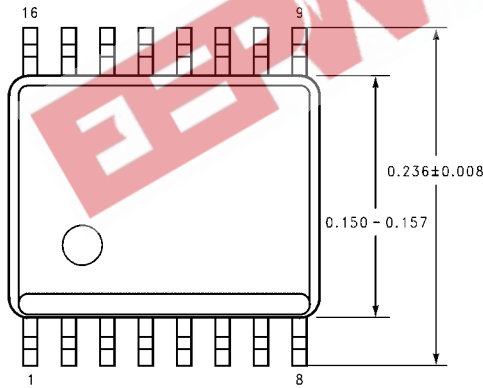
FIGURE 2. AC Waveforms



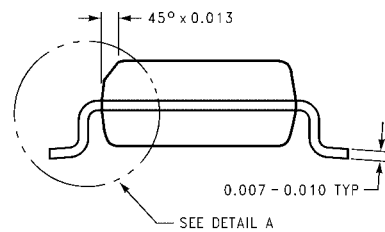
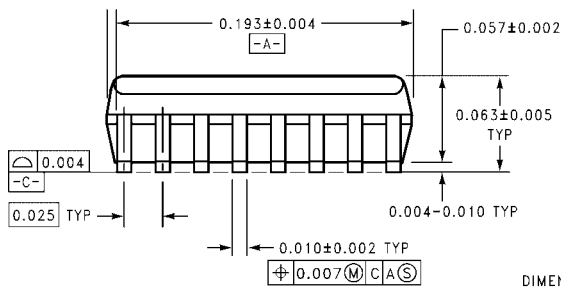
Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M14A



DETAIL A
TYPICAL, SCALE: 40%

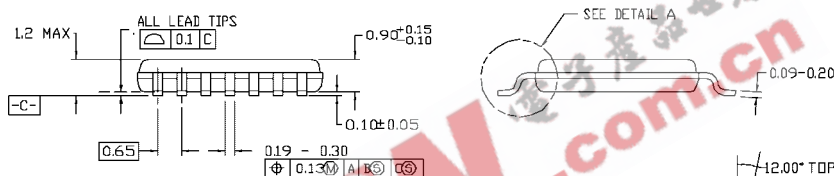
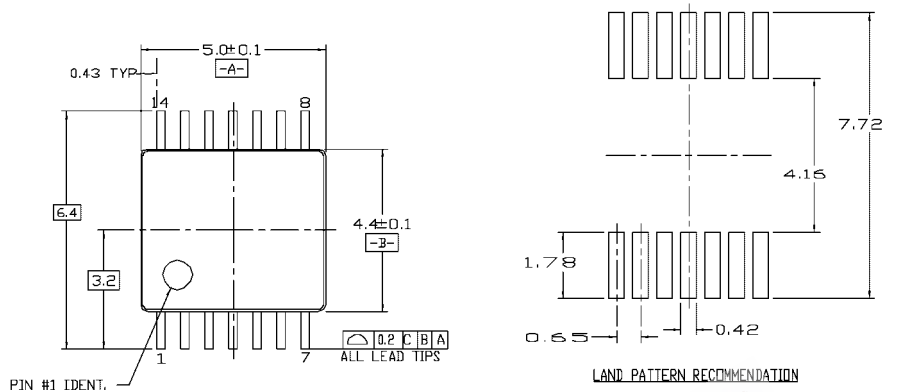


DIMENSIONS ARE IN INCHES

MQA16 (REV. A)

16-Lead Quarter Size Outline Package (QSOP), JEDEC MO-137, 0.150" Wide Package Number MQA16

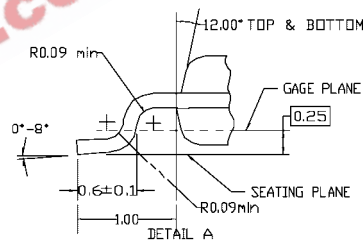
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153 VARIATION AB, REF NOTE 6, DATED 7/93
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD



14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.

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