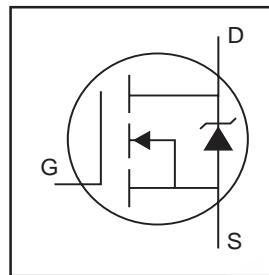


IRL1404PbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

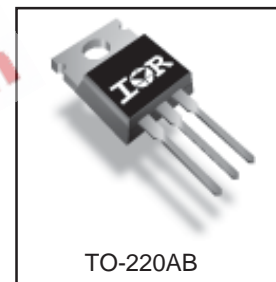


$V_{DSS} = 40V$
$R_{DS(on)} = 4.0m\Omega$
$I_D = 160A\text{⑥}$

Description

Seventh Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	160⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	110⑥	
I_{DM}	Pulsed Drain Current ①	640	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	620	mJ
I_{AR}	Avalanche Current③	95	A
E_{AR}	Repetitive Avalanche Energy④	20	mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

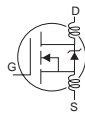
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted)⑥	—	62	

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.038	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	4.0	mΩ	V _{GS} = 10V, I _D = 95A ①
		—	—	5.9		V _{GS} = 4.3V, I _D = 40A ②
V _{GS(th)}	Gate Threshold Voltage	1.0	—	3.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	93	—	—	S	V _{DS} = 25V, I _D = 95A
I _{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	V _{DS} = 40V, V _{GS} = 0V
		—	—	250		V _{DS} = 32V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage Gate-to-Source Reverse Leakage	—	—	200 -200	nA	V _{GS} = 20V
		—	—	—		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	140	nC	I _D = 95A
Q _{gs}	Gate-to-Source Charge	—	—	48		V _{DS} = 32V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	60		V _{GS} = 5.0V, See Fig. 6 ④
t _{d(on)}	Turn-On Delay Time	—	18	—	ns	V _{DD} = 20V
t _r	Rise Time	—	270	—		I _D = 95A
t _{d(off)}	Turn-Off Delay Time	—	38	—		R _G = 2.5Ω V _{GS} = 4.5V
t _f	Fall Time	—	37	—		R _D = 0.25Ω ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	6590	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	1710	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	350	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	6650	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	1510	—		V _{GS} = 0V, V _{DS} = 32V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance ⑤	—	1480	—		V _{GS} = 0V, V _{DS} = 0V to 32V

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	160⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	640		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 95A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	63	94	ns	T _J = 25°C, I _F = 95A
Q _{rr}	Reverse Recovery Charge	—	170	250	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting T_J = 25°C, L = 0.35mH
R_G = 25Ω, I_{AS} = 95A. (See Figure 12).
- ③ I_{SD} ≤ 95A, di/dt ≤ 160A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

- ⑤ C_{oss eff.} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DS}.
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4.
- ⑦ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

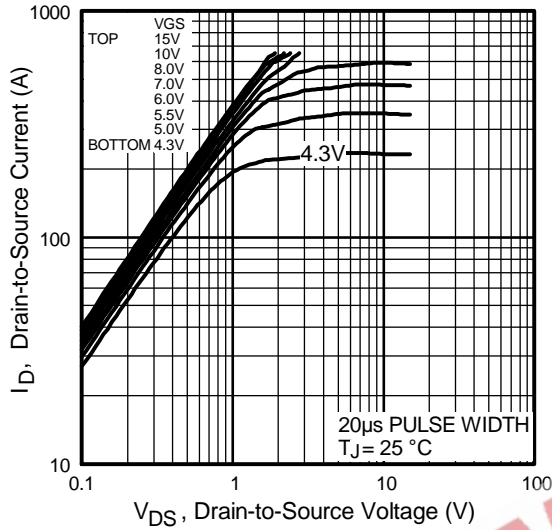


Fig 1. Typical Output Characteristics

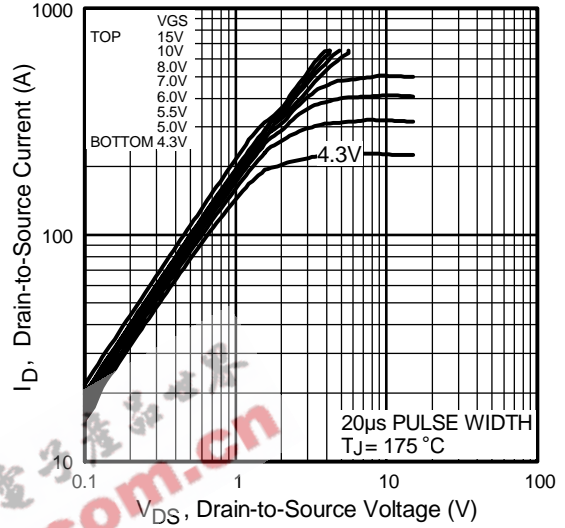


Fig 2. Typical Output Characteristics

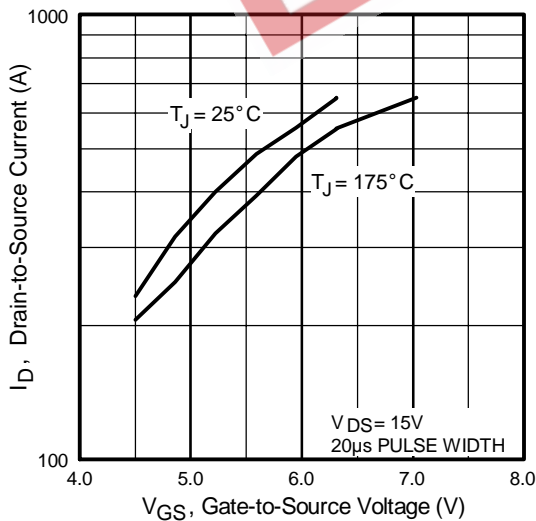


Fig 3. Typical Transfer Characteristics

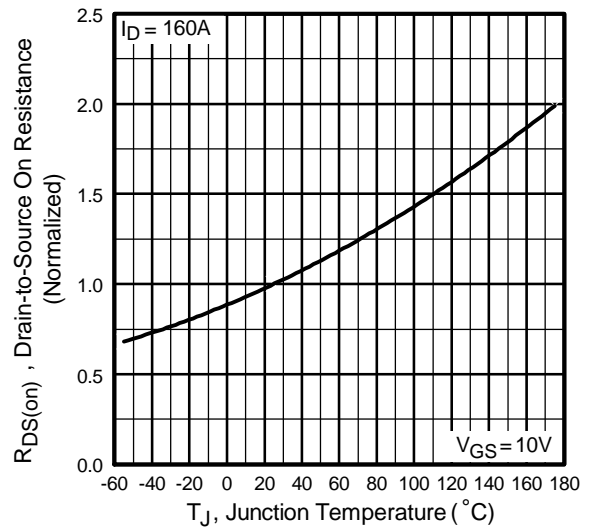


Fig 4. Normalized On-Resistance Vs. Temperature

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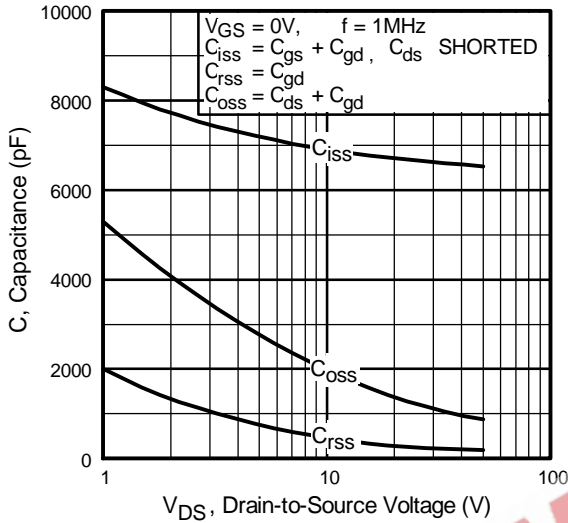


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

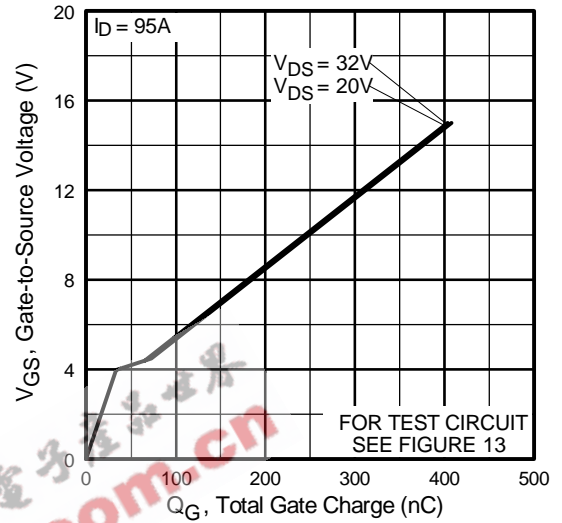


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

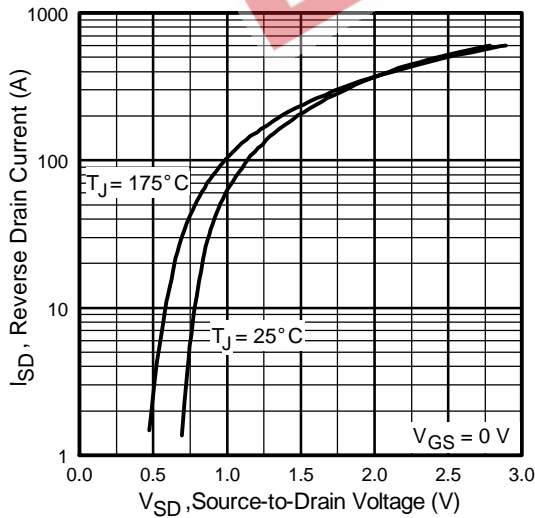


Fig 7. Typical Source-Drain Diode Forward Voltage

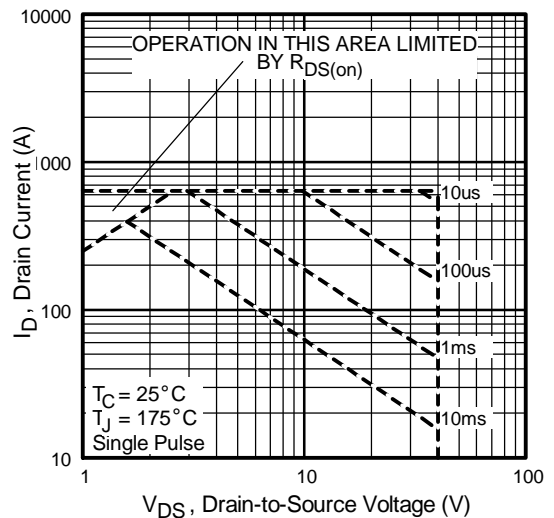


Fig 8. Maximum Safe Operating Area

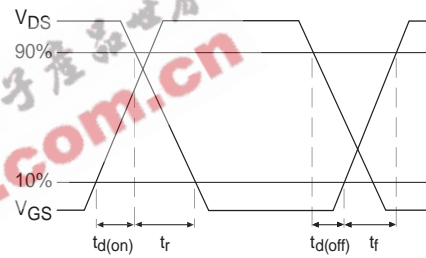
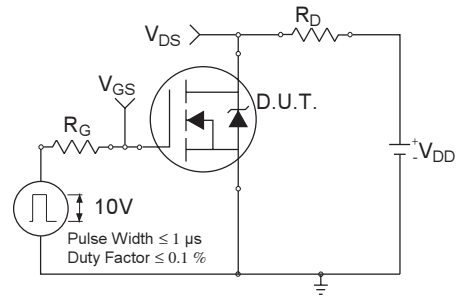
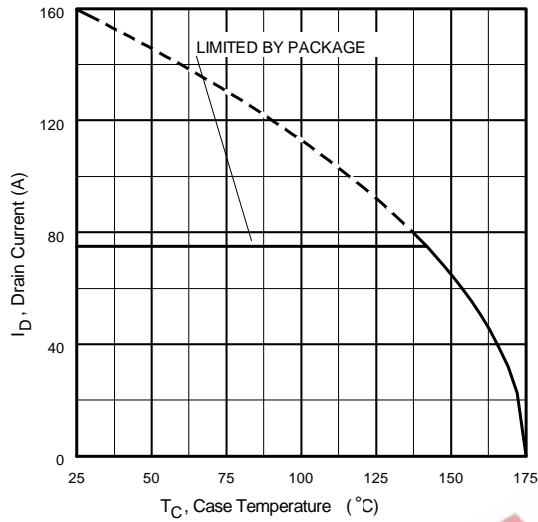


Fig 9. Maximum Drain Current Vs. Case Temperature

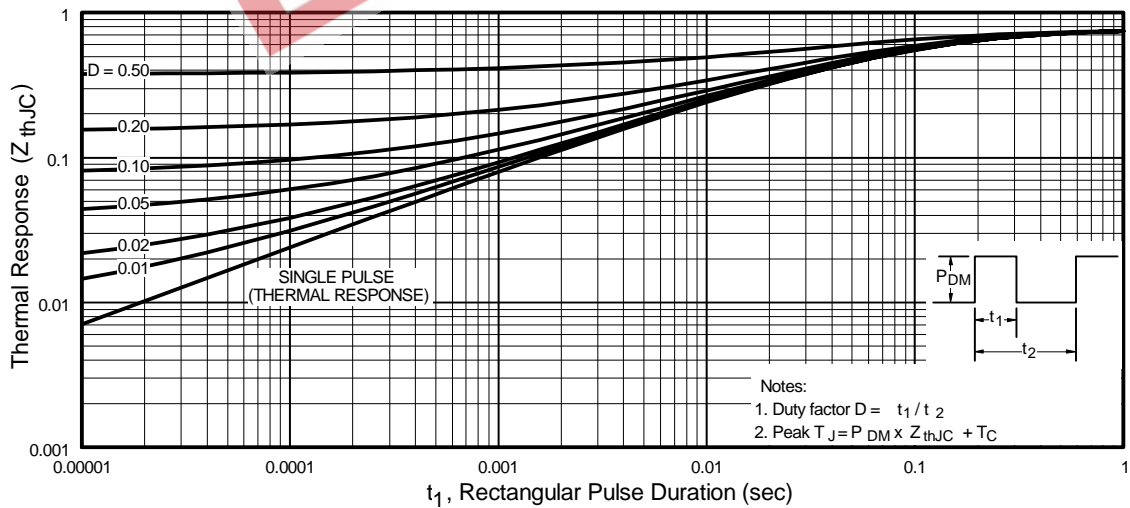


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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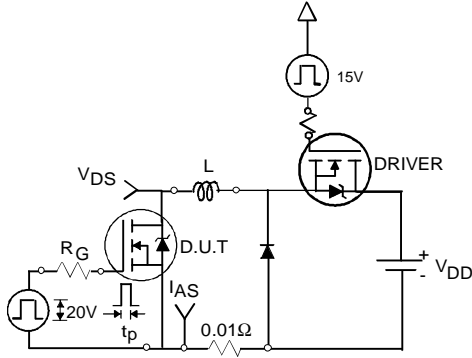


Fig 12a. Unclamped Inductive Test Circuit

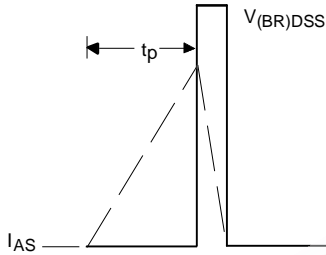


Fig 12b. Unclamped Inductive Waveforms

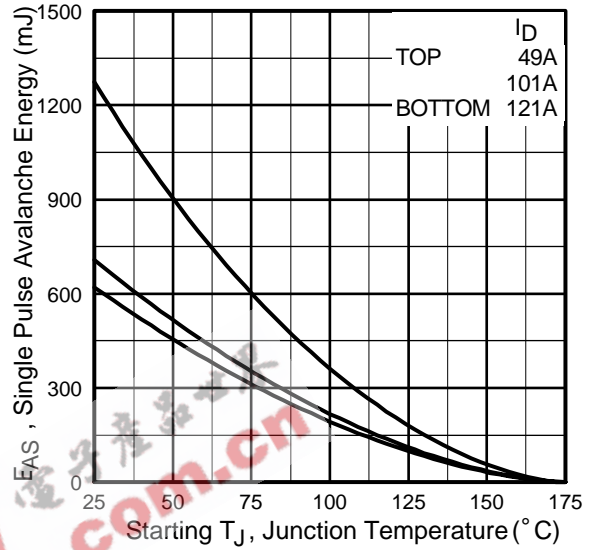


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

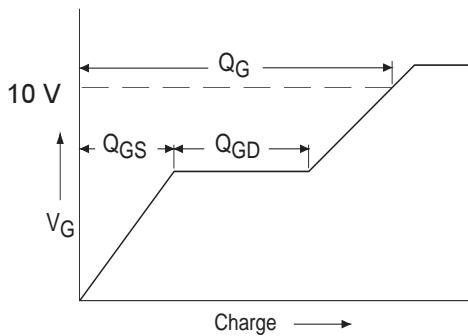


Fig 13a. Basic Gate Charge Waveform

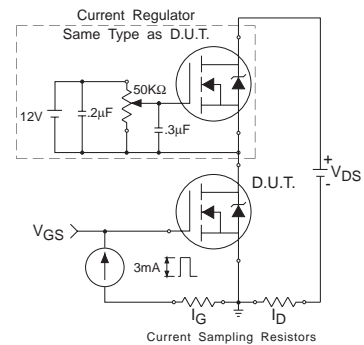
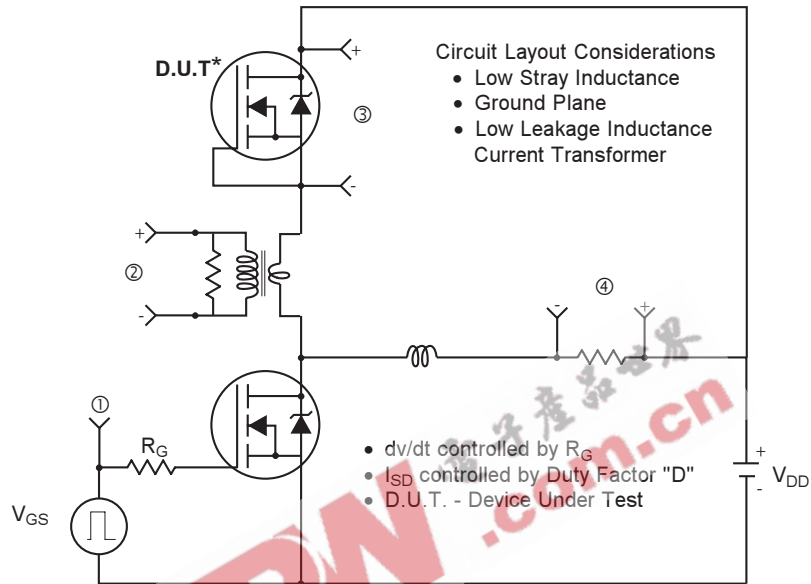
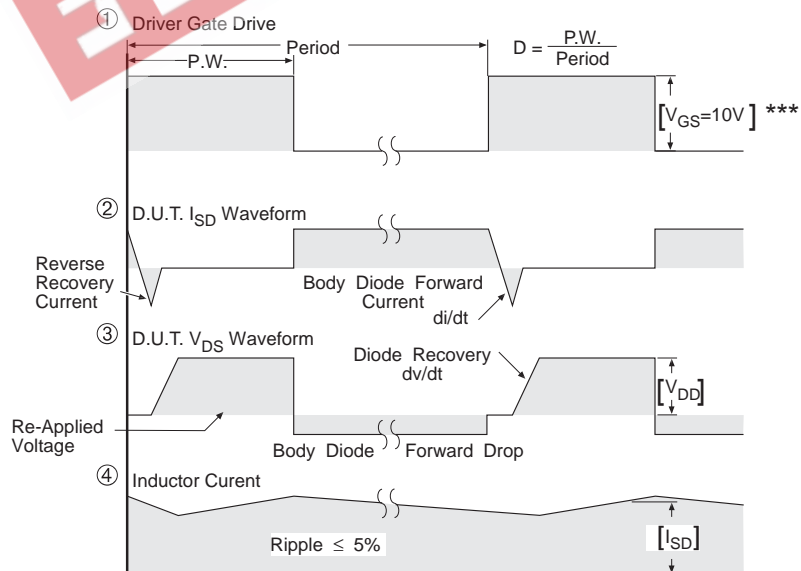


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

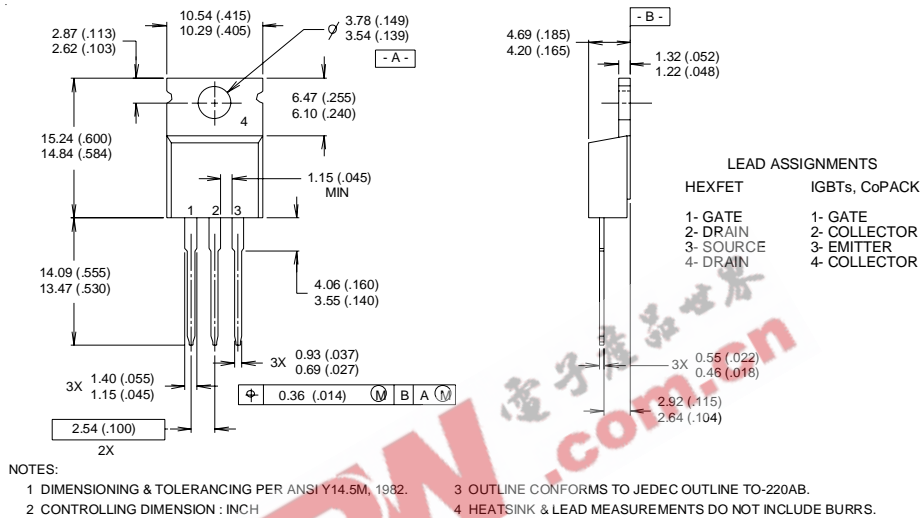
Fig 14. For N-channel HEXFET® power MOSFETs

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TO-220AB Package Outline

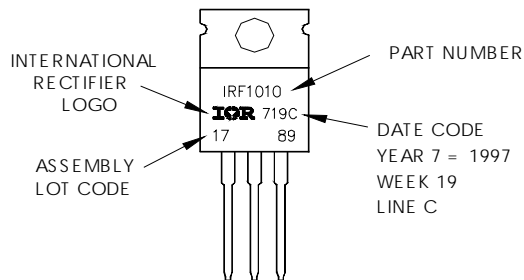
Dimensions are shown in millimeters (inches)



TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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