# P4C168, P4C169, P4C170 ULTRA HIGH SPEED 4K x 4 STATIC CMOS RAMS

## FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 12/15/20/25ns (Commercial)**
  - **– 20/25/35ns (P4C168 Military)**
- **Low Power Operation (Commercial)**
  - **– 715 mW Active**
  - **– 193 mW Standby (TTL Input) P4C168**
  - **– 83 mW Standby (CMOS Input) P4C168**
- **Single 5V±10% Power Supply**
- **Fully TTL Compatible, Common I/O Ports**
- **Three Options**
  - **– P4C168 Low Power Standby Mode**
  - **– P4C169 Fast Chip Select Control**
  - **– P4C170 Fast Chip Select, Output Enable Controls**
- **Standard Pinout (JEDEC Approved)**
  - **– P4C168: 20-pin DIP, SOJ and SOIC**
  - **– P4C169: 20-pin DIP and SOIC**
  - **– P4C170: 22-pin DIP**

## DESCRIPTION

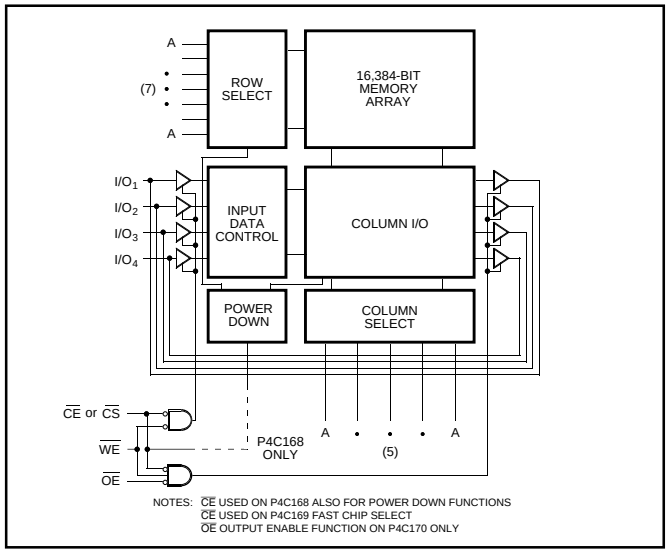
The P4C168, P4C169 and P4C170 are a family of 16,384-bit ultra high-speed static RAMs organized as 4K x 4. All three devices have common input/output ports.The P4C168 enters the standby mode when the chip enable ($\overline{CE}$) control goes high; with CMOS input levels, power consumption is only 83mW in this mode. Both the P4C169 and the P4C170 offer a fast chip select access time that is only 67% of the address access time. In addition, the P4C170 includes an output enable ($\overline{OE}$) control to eliminate data bus contention. The RAMs operate from a single 5V ± 10% tolerance power supply.

Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption to a low 715 mW active, 193 mW standby.

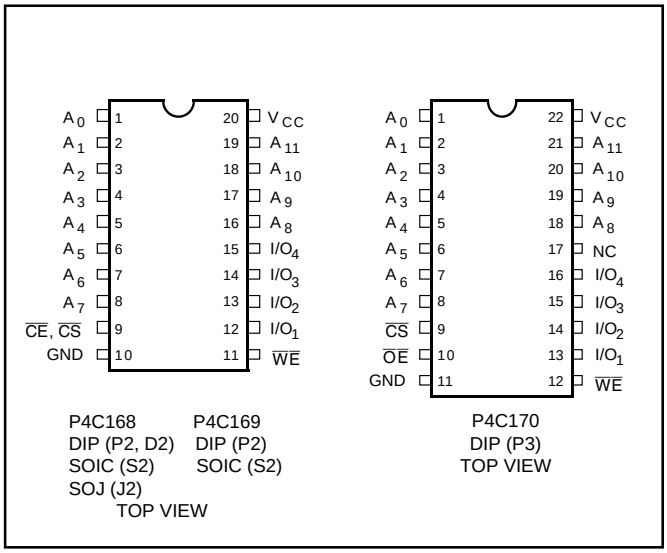
The P4C168 and P4C169 are available in 20-pin (P4C170 in 22-pin) 300 mil DIP packages providing excellent board level densities. The P4C168 is also available in 20-pin 300 mil SOIC and SOJ packages.

The P4C169 is also available in a 20-pin 300 mil SOIC package. The P4C170 is also available in a 22-pin 300 mil SOJ package.

## FUNCTIONAL BLOCK DIAGRAM




## PIN CONFIGURATIONS




P4C168 DIP (P2, D2) SOIC (S2) SOJ (J2) TOP VIEW

P4C169 DIP (P2) SOIC (S2) TOP VIEW

P4C170 DIP (P3) TOP VIEW

## MAXIMUM RATINGS[1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Pin with Respect to GND | –0.5 to +7 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND (up to 7.0V) | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | –55 to +125 | °C |

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.0 | W |
| $I_{OUT}$ | DC Output Current | 50 | mA |

## RECOMMENDED OPERATING CONDITIONS

| Grade[2] | Ambient Temp | Gnd | $V_{CC}$ |
|---|---|---|---|
| Commercial | 0°C to 70°C | 0V | 5.0V ± 10% |
| Military | –55°C to +125°C | 0V | 5.0V ± 10% |

## CAPACITANCES[4]

($V_{CC}$ = 5.0V, $T_A$ = 25°C, f = 1.0MHz)

| Symbol | Parameter | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$= 0V | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | | P4C168/169/170 Min | P4C168/169/170 Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2.2 | $V_{CC}$ +0.5 | V |
| $V_{IL}$ | Input Low Voltage | | | –0.5(3) | 0.8 | V |
| $V_{HC}$ | CMOS Input High Voltage | | | $V_{CC}$ –0.2 | $V_{CC}$ +0.5 | V |
| $V_{LC}$ | CMOS Input Low Voltage | | | –0.5(3) | 0.2 | V |
| $V_{CD}$ | Input Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18 mA | | | –1.2 | V |
| $V_{OL}$ | Output Low Voltage (TTL Load) | $I_{OL}$ = +8 mA, $V_{CC}$ = Min. | | | 0.4 | V |
| $V_{OLC}$ | Output Low Voltage (CMOS Load) | $I_{OLC}$ = +100 µA, $V_{CC}$ = Min. | | | 0.2 | V |
| $V_{OH}$ | Output High Voltage (TTL Load) | $I_{OH}$ = –4 mA, $V_{CC}$ = Min. | | 2.4 | | V |
| $V_{OHC}$ | Output High Voltage (CMOS Load) | $I_{OHC}$ = –100 µA, $V_{CC}$ = Min. | | $V_{CC}$ –0.2 | | V |
| $I_{LI}$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = GND to $V_{CC}$ | Mil.<br>Comm'l | –10<br>–5 | +10<br>+5 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max., $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to $V_{CC}$ | Mil.<br>Comm'l | –10<br>–5 | +10<br>+5 | µA |
| $I_{CC}$ | Dynamic Operating Current | $V_{CC}$ = Max., f = Max., Outputs Open | | — | 130 | mA |
| $I_{SB}$ | Standby Power Supply Current (TTL Input Levels) P4C168 only | $\overline{CE} \geq V_{IH}$, $V_{CC}$ = Max., f = Max., Outputs Open | | — | 35 | mA |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) P4C168 only | $\overline{CE} \geq V_{HC}$, $V_{CC}$ = Max., f = 0, Outputs Open $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$ | | — | 15 | mA |

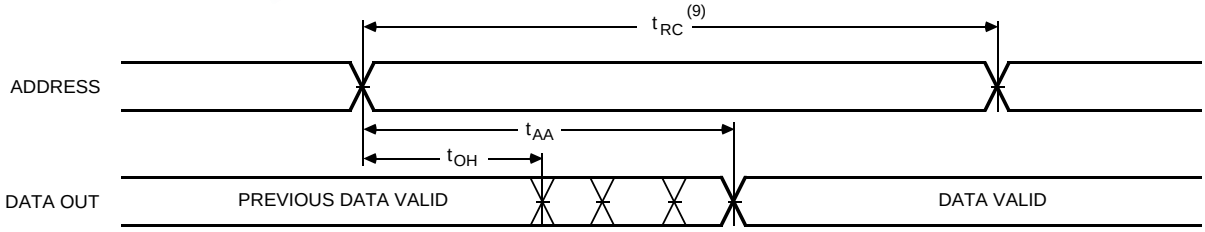
## AC CHARACTERISTICS—READ CYCLE

($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | –12 | | –15 | | –20 | | –25 | | –35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 12 | | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{AA}$ | Address Access Time | | 12 | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{AC}$ § | Chip Enable Access Time | | 12 | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{AC}$ ‡ | Chip Select Access Time | | 8 | | 9 | | 12 | | 15 | | 20 | ns |
| $t_{OH}$ | Output Hold from Address Change | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{LZ}$ ‡ | Chip Enable to Output in Low Z | 2 | | 2 | | 2 | | 2 | | 2 | | ns |
| $t_{HZ}$ † | Chip Disable to Output in High Z | | 6 | | 7 | | 9 | | 10 | | 15 | ns |
| $t_{OE}$ † | Output Enable to Data Valid | | 8 | | 10 | | 12 | | 15 | | 15 | ns |
| $t_{OLZ}$ † | Output Enable to Output in Low Z | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{OHZ}$ † | Output Disable to Output in High Z | | 6 | | 7 | | 9 | | 11 | | 15 | ns |
| $t_{RCS}$ | Read Command Setup Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{RCH}$ | Read Command Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PU}$ § | Chip Enable to Power Up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ § | Chip Disable to Power Down Time | | 12 | | 15 | | 20 | | 25 | | 35 | ns |

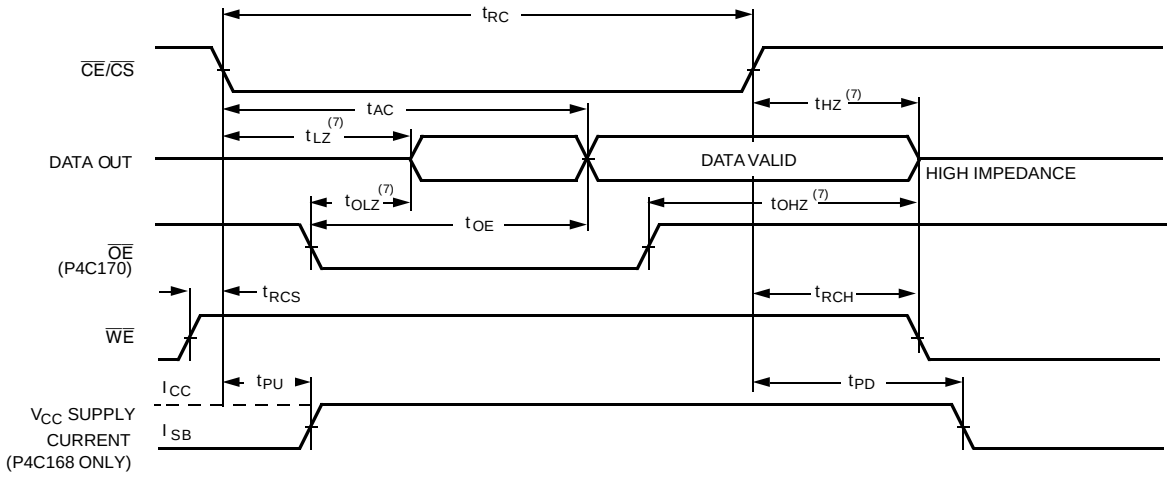
§ P4C168 only
† P4C170 only
‡ Chip Select/Deselect for P4C169 and P4C170

## TIMING WAVEFORM OF READ CYCLE NO. 1 (ADDRESS CONTROLLED)[5,6]

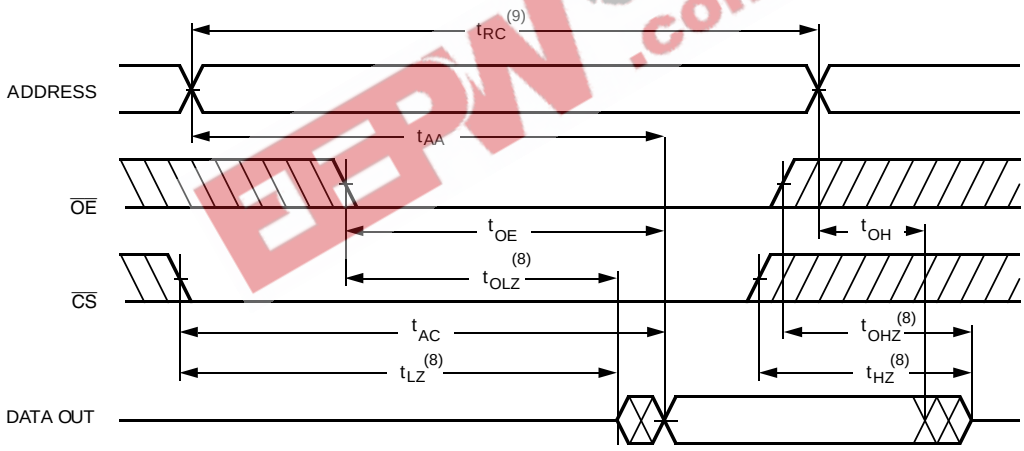



**Notes:**
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$/$\overline{CS}$ and $\overline{OE}$ are LOW for READ cycle.

## TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{CE}/\overline{CS}$ CONTROLLED)[5,7]




## TIMING WAVEFORM OF READ CYCLE NO. 3—P4C170 ONLY ($\overline{OE}$ CONTROLLED)[5]




**Notes:**

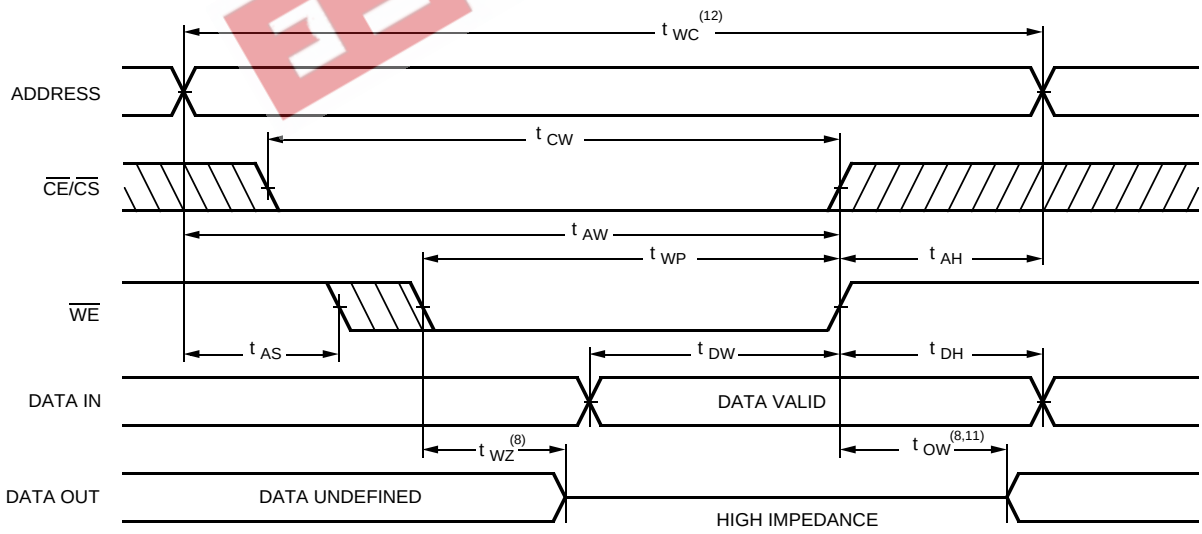
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}/\overline{CS}$ transition low. For Fast $\overline{CS}$, $t_{AA}$ must still be met.
8. Transition is measured ±200mV from steady state voltage prior to change, with loading as specified in Figure 1.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

## AC ELECTRICAL CHARACTERISTICS - WRITE CYCLE

($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym. | Parameter | –12 | | –15 | | –20 | | –25 | | –35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{WC}$ | Write Cycle Time | 12 | | 15 | | 18 | | 20 | | 35 | | ns |
| $t_{CW}$ | Chip Enable Time to End of Write | 12 | | 15 | | 18 | | 20 | | 30 | | ns |
| $t_{AW}$ | Address Valid to End of Write | 12 | | 15 | | 18 | | 20 | | 30 | | ns |
| $t_{AS}$ | Address Set-up Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 12 | | 15 | | 18 | | 20 | | 30 | | ns |
| $t_{AH}$ | Address Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{DW}$ | Data Valid to End of Write | 7 | | 8 | | 10 | | 10 | | 15 | | ns |
| $t_{DH}$ | Data Hold Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{WZ}$ | Write Enable to Output in High Z | | 4 | | 5 | | 7 | | 7 | | 13 | ns |
| $t_{OW}$ | Output Active from End of Write | 0 | | 0 | | 0 | | 0 | | 0 | | ns |

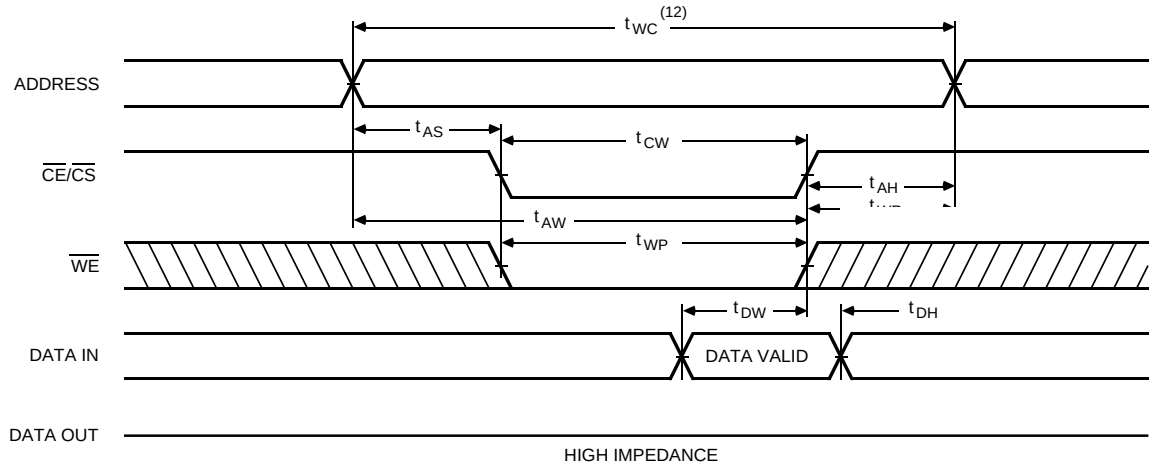
## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[10]




**Notes:**

10. $\overline{CE}/\overline{CS}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. If $\overline{CE}/\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
12. Write Cycle Time is measured from the last valid address to the first transitioning address.

## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$/$\overline{CS}$ CONTROLLED)[10]




## TRUTH TABLES

P4C168 (P4C169)

| Mode | $\overline{CE}$ ($\overline{CS}$) | $\overline{WE}$ | Output |
|---|---|---|---|
| Standby (Deselect) | H | X | High Z |
| Read | L | H | $D_{OUT}$ |
| Write | L | L | High Z |

P4C170

| Mode | $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | Output |
|---|---|---|---|---|
| Deselect | H | X | X | High Z |
| Read | L | H | L | $D_{OUT}$ |
| Output Inhibit | L | H | H | High Z |
| Write | L | L | X | High Z |

## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

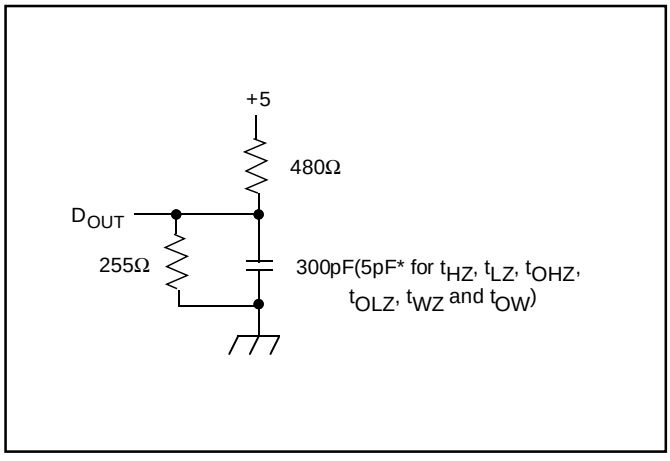



**Figure 1. Output Load**

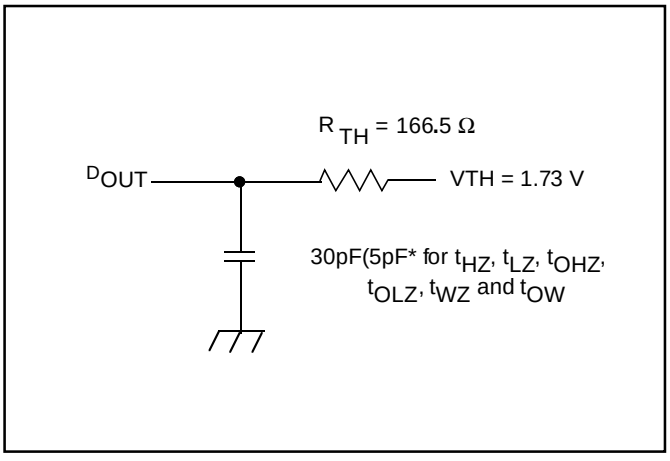



**Figure 2. Thevenin Equivalent**

* including scope and test fixture.

**Note:**
Because of the ultra-high speed of the P4C168, P4C169 AND P4C170 care must be taken when testing these devices; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the $V_{CC}$ and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between $V_{CC}$ and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with $D_{OUT}$ to match 166Ω (Thevenin Resistance).

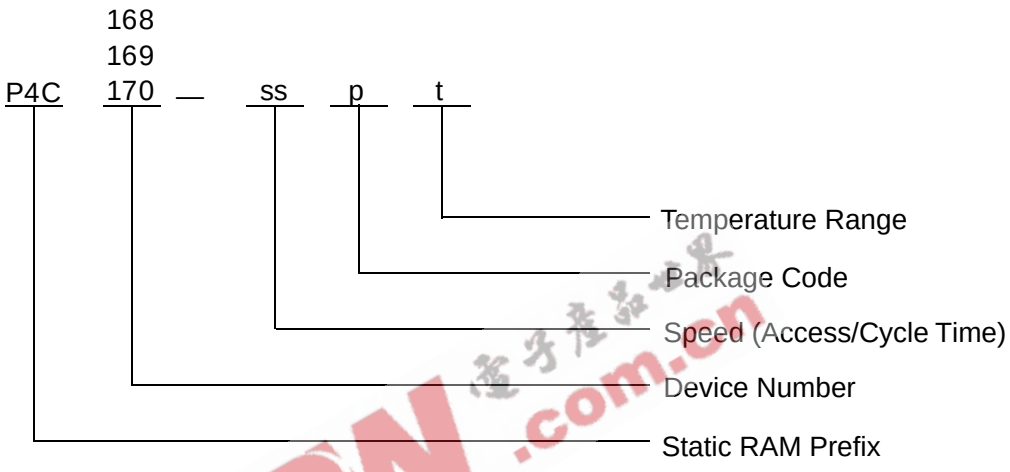
## PACKAGE SUFFIX

| Package Suffix | Description |
|---|---|
| P | Plastic DIP, 300 mil wide standard |
| S | Plastic SOIC, 300 mil wide standard |
| J | Plastic SOJ, 300 mil wide standard |
| D | CERDIP, 300 mil wide standard |

## TEMPERATURE RANGE SUFFIX

| Temperature Range Suffix | Description |
|---|---|
| C | Commercial Temperature Range, 0°C – +70°C. |
| M | Military Temperature Range, –55°C – +125°C. |
| MB | Mil. Temp. with MIL-STD-883D Class B compliance |

## ORDERING INFORMATION




ss = Speed (access/cycle time in ns), e.g., 15, 20

p = Package code, i.e., P, S,D, J.

t = Temperature range, i.e., C, M, MB.

The P4C168 is also available per SMD #5962-86705

## SELECTION GUIDE

The P4C168, P4C169 and P4C170 are available in the following temperature, speed and package options.

| Temperature Range | Speed (ns) / Package | 12 | 15 | 20 | 25 | 35 |
|---|---|---|---|---|---|---|
| Commercial | Plastic DIP<br>Plastic SOIC†<br>Plastic SOJ†† | -12PC<br>-12SC<br>-12JC | -15PC<br>-15SC<br>-15JC | -20PC<br>-20SC<br>-20JC | -25PC<br>-25SC<br>-25JC | N/A<br>N/A<br>N/A |
| Military Temp. (P4C168 only) | CERDIP | N/A | N/A | -20DM | -25DM | -35DM |
| Military Processed* (P4C168 only) | CERDIP | N/A | N/A | -20DMB | -25DMB | -35DMB |

† P4C168 and P4C169 only.
†† P4C168
* Military temperature range with MIL-STD-883, Class B processing.
N/A = Not available