

# P4C168, P4C169, P4C170 ULTRA HIGH SPEED 4K x 4 STATIC CMOS RAMS

## FEATURES

- Full CMOS, 6T Cell
- High Speed (Equal Access and Cycle Times)
  - 12/15/20/25/35ns (Commercial)
  - 20/25/35/45/55/70ns (P4C168 Military)
- Low Power Operation (Commercial)
  - 715 mW Active
  - 193 mW Standby (TTL Input) P4C168
  - 83 mW Standby (CMOS Input) P4C168
- Single 5V±10% Power Supply
- Fully TTL Compatible, Common I/O Ports
- Three Options
  - P4C168 Low Power Standby Mode
  - P4C169 Fast Chip Select Control
  - P4C170 Fast Chip Select, Output Enable Controls
- Standard Pinout (JEDEC Approved)
  - P4C168: 20-pin DIP, SOJ, LCC, SOIC, CERPACK, and Flat Pack
  - P4C169: 20-pin DIP and SOIC
  - P4C170: 22-pin DIP

## DESCRIPTION

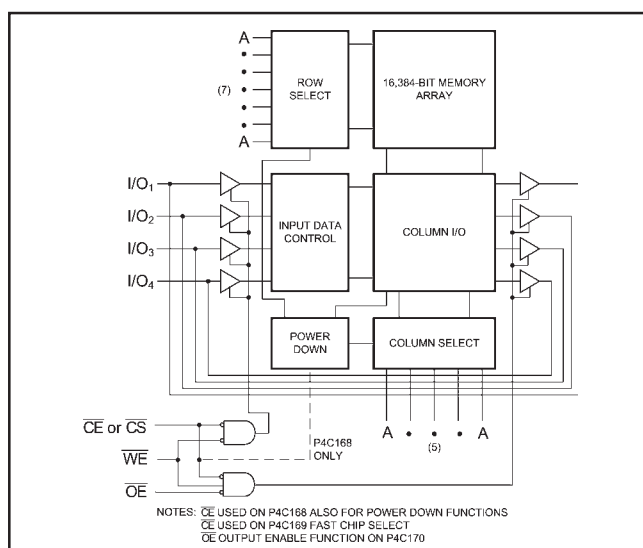
The P4C168, P4C169 and P4C170 are a family of 16,384-bit ultra high-speed static RAMs organized as 4K x 4. All three devices have common input/output ports. The P4C168 enters the standby mode when the chip enable ( $\overline{CE}$ ) control goes HIGH; with CMOS input levels, power consumption is only 83mW in this mode. Both the P4C169 and the P4C170 offer a fast chip select access time that is only 67% of the address access time. In addition, the P4C170 includes an output enable ( $\overline{OE}$ ) control to eliminate data bus contention. The RAMs operate from a single 5V ± 10% tolerance power supply.

Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption to a low 715 mW active, 193 mW standby.

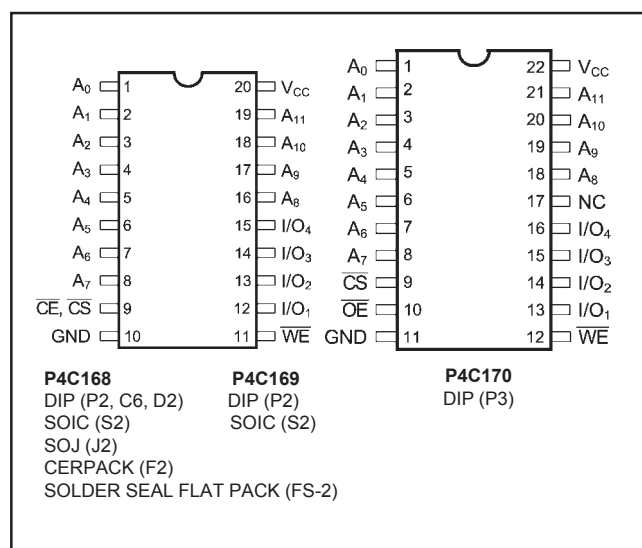
The P4C168 and P4C169 are available in 20-pin (P4C170 in 22-pin) 300 mil DIP packages providing excellent board level densities. The P4C168 is also available in 20-pin 300 mil SOIC, SOJ, CERPACK, and Flat Pack packages.

The P4C169 is also available in a 20-pin 300 mil SOIC package.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATIONS



**MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply Pin with Respect to GND	-0.5 to +7	V
$V_{TERM}$	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to $V_{CC} + 0.5$	V
$T_A$	Operating Temperature	-55 to +125	°C

Symbol	Parameter	Value	Unit
$T_{BIAS}$	Temperature Under Bias	-55 to +125	°C
$T_{STG}$	Storage Temperature	-65 to +150	°C
$P_T$	Power Dissipation	1.0	W
$I_{OUT}$	DC Output Current	50	mA

**RECOMMENDED OPERATING CONDITIONS**

Grade <sup>(2)</sup>	Ambient Temp	Gnd	$V_{CC}$
Commercial	0°C to 70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

**CAPACITANCES<sup>(4)</sup>**(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
$C_{IN}$	Input Capacitance	V <sub>IN</sub> = 0V	5	pF
$C_{OUT}$	Output Capacitance	V <sub>OUT</sub> = 0V	7	pF

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Parameter	Test Conditions	P4C168/169/170		Unit
			Min	Max	
$V_{IH}$	Input High Voltage		2.2	$V_{CC} + 0.5$	V
$V_{IL}$	Input Low Voltage		-0.5(3)	0.8	V
$V_{HC}$	CMOS Input High Voltage		$V_{CC} - 0.2$	$V_{CC} + 0.5$	V
$V_{LC}$	CMOS Input Low Voltage		-0.5(3)	0.2	V
$V_{CD}$	Input Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$		-1.2	V
$V_{OL}$	Output Low Voltage (TTL Load)	$I_{OL} = +8 \text{ mA}, V_{CC} = \text{Min.}$		0.4	V
$V_{OLC}$	Output Low Voltage (CMOS Load)	$I_{OLC} = +100 \mu\text{A}, V_{CC} = \text{Min.}$		0.2	V
$V_{OH}$	Output High Voltage (TTL Load)	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min.}$	2.4		V
$V_{OHC}$	Output High Voltage (CMOS Load)	$I_{OHC} = -100 \mu\text{A}, V_{CC} = \text{Min.}$	$V_{CC} - 0.2$		V
$I_{LI}$	Input Leakage Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$	Mil. -10 Comm'l -5	+10 +5	μA
$I_{LO}$	Output Leakage Current	$V_{CC} = \text{Max.}, \overline{CS} = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	Mil. -10 Comm'l -5	+10 +5	μA
$I_{CC}$	Dynamic Operating Current	$V_{CC} = \text{Max.}, f = \text{Max.}, \text{Outputs Open}$	—	130	mA
$I_{SB}$	Standby Power Supply Current (TTL Input Levels) P4C168 only	$\overline{CE} \geq V_{IH}, V_{CC} = \text{Max.}, f = \text{Max.}, \text{Outputs Open}$	—	35	mA
$I_{SB1}$	Standby Power Supply Current (CMOS Input Levels) P4C168 only	$\overline{CE} \geq V_{HC}, V_{CC} = \text{Max.}, f = 0, V_{IN} \leq V_{LC} \text{ or } V_{IN} \geq V_{HC}$	—	15	mA

**AC CHARACTERISTICS—READ CYCLE** $(V_{CC} = 5V \pm 10\%, \text{ All Temperature Ranges})^{(2)}$ 

Sym	Parameter	-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{RC}$	Read Cycle Time	12		15		20		25		35		ns
$t_{AA}$	Address Access Time		12		15		20		25		35	ns
$t_{AC}^{\S}$	Chip Enable Access Time		12		15		20		25		35	ns
$t_{AC}^{\ddagger}$	Chip Select Access Time		8		9		12		15		20	ns
$t_{OH}$	Output Hold from Address Change	2		2		2		2		2		ns
$t_{LZ}^{\ddagger}$	Chip Enable to Output in Low Z	2		2		2		2		2		ns
$t_{HZ}^{\dagger}$	Chip Disable to Output in High Z		7		8		9		10		15	ns
$t_{OE}^{\dagger}$	Output Enable to Data Valid		8		10		12		15		15	ns
$t_{OLZ}^{\dagger}$	Output Enable to Output in Low Z	0		0		0		0		0		ns
$t_{OHZ}^{\dagger}$	Output Disable to Output in High Z		6		7		9		11		15	ns
$t_{RCS}$	Read Command Setup Time	0		0		0		0		0		ns
$t_{RCH}$	Read Command Hold Time	0		0		0		0		0		ns
$t_{PU}^{\S}$	Chip Enable to Power Up Time	0		0		0		0		0		ns
$t_{PD}^{\S}$	Chip Disable to Power Down Time		12		15		20		25		35	ns

**AC CHARACTERISTICS—READ CYCLE (CONTINUED)** $(V_{CC} = 5V \pm 10\%, \text{ All Temperature Ranges})^{(2)}$ 

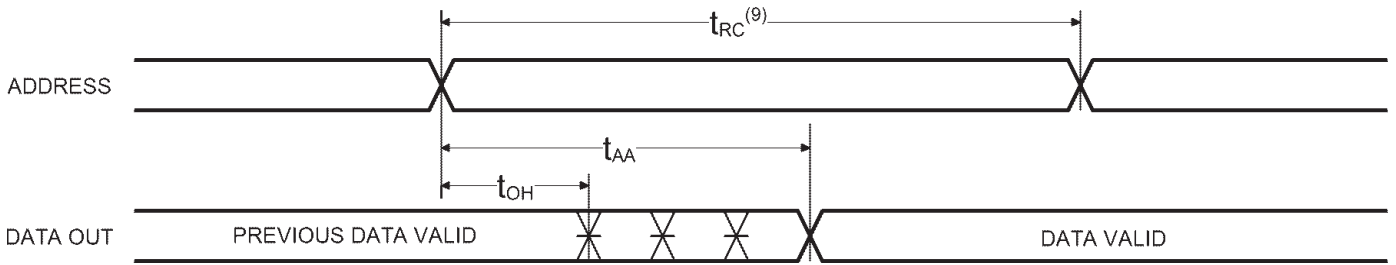
Sym	Parameter	-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	
$t_{RC}$	Read Cycle Time	45		55		70		ns
$t_{AA}$	Address Access Time		45		55		70	ns
$t_{AC}^{\S}$	Chip Enable Access Time		45		55		70	ns
$t_{OH}$	Output Hold from Address Change	2		2		2		ns
$t_{LZ}^{\ddagger}$	Chip Enable to Output in Low Z	2		2		2		ns
$t_{HZ}^{\dagger}$	Chip Disable to Output in High Z		25		25		30	ns
$t_{RCS}$	Read Command Setup Time	0		0		0		ns
$t_{RCH}$	Read Command Hold Time	0		0		0		ns
$t_{PU}^{\S}$	Chip Enable to Power Up Time	0		0		0		ns
$t_{PD}^{\S}$	Chip Disable to Power Down Time		45		55		70	ns

§ P4C168 only

† P4C170 only

‡ Chip Select/Deselect for P4C169 and P4C170

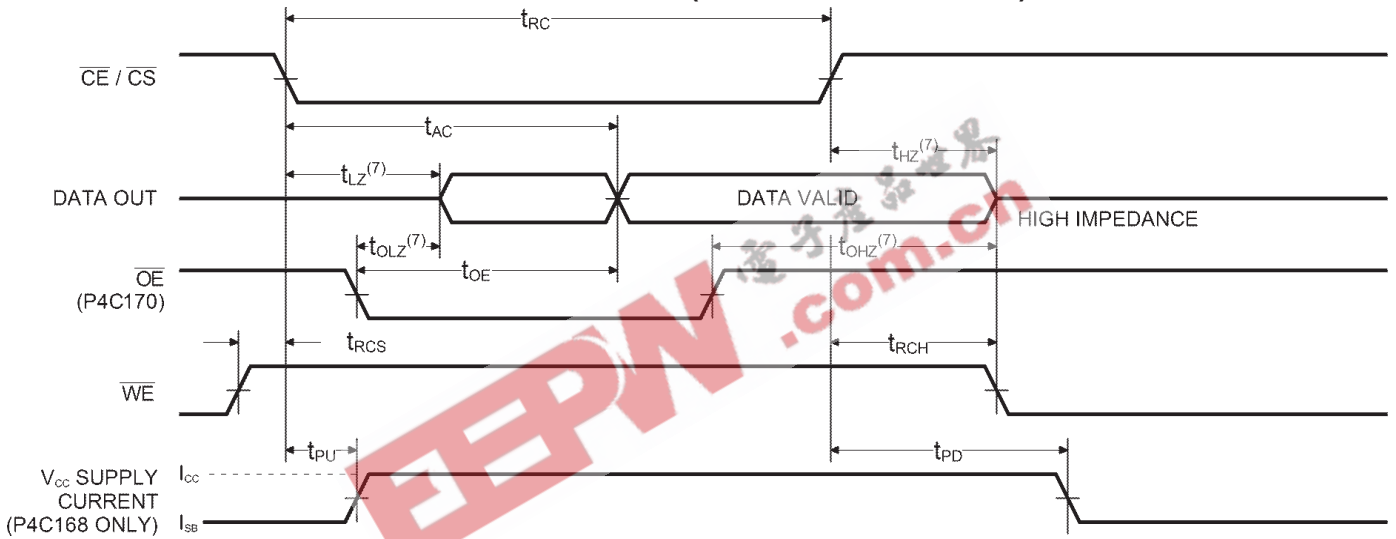
**TIMING WAVEFORM OF READ CYCLE NO. 1 (ADDRESS CONTROLLED)<sup>(5,6)</sup>**



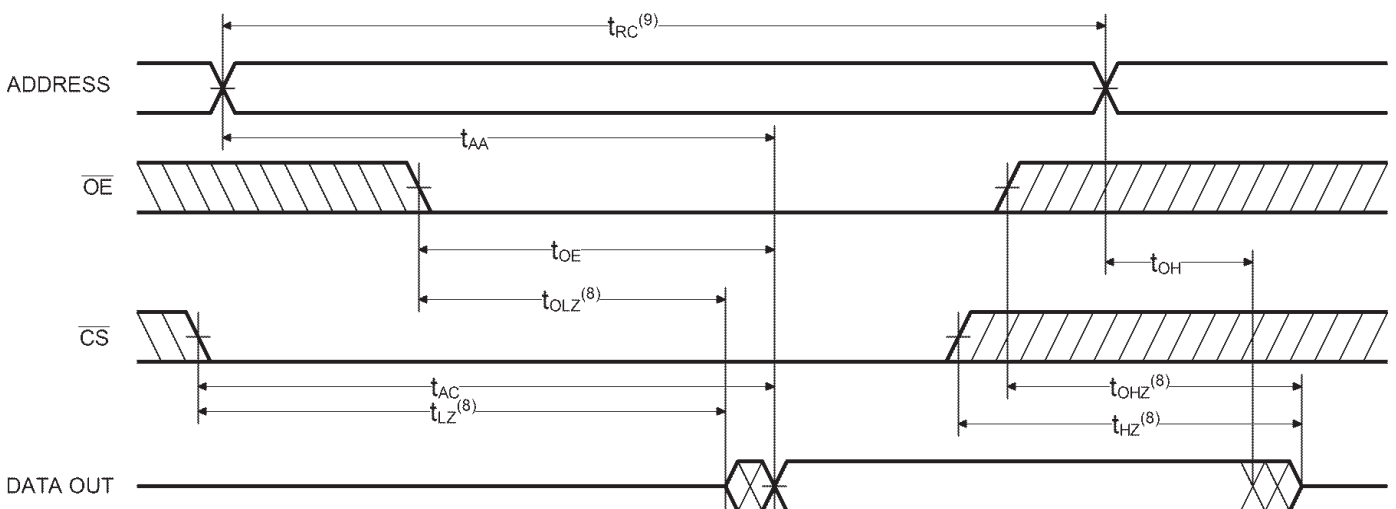
**Notes:**

- 5.  $\overline{WE}$  is HIGH for READ cycle.
- 6.  $\overline{CE}/\overline{CS}$  and  $\overline{OE}$  are LOW for READ cycle.

**TIMING WAVEFORM OF READ CYCLE NO. 2 ( $\overline{CE}/\overline{CS}$  CONTROLLED)<sup>(5,7)</sup>**



**TIMING WAVEFORM OF READ CYCLE NO. 3—P4C170 ONLY ( $\overline{OE}$  CONTROLLED)<sup>(5)</sup>**



**Notes:**

- 7. ADDRESS must be valid prior to, or coincident with  $\overline{CE}/\overline{CS}$  transition low. For Fast  $\overline{CS}$ ,  $t_{AA}$  must still be met.
- 8. Transition is measured  $\pm 200\text{mV}$  from steady state voltage prior to change, with loading as specified in Figure 1.
- 9. Read Cycle Time is measured from the last valid address to the first transitioning address.

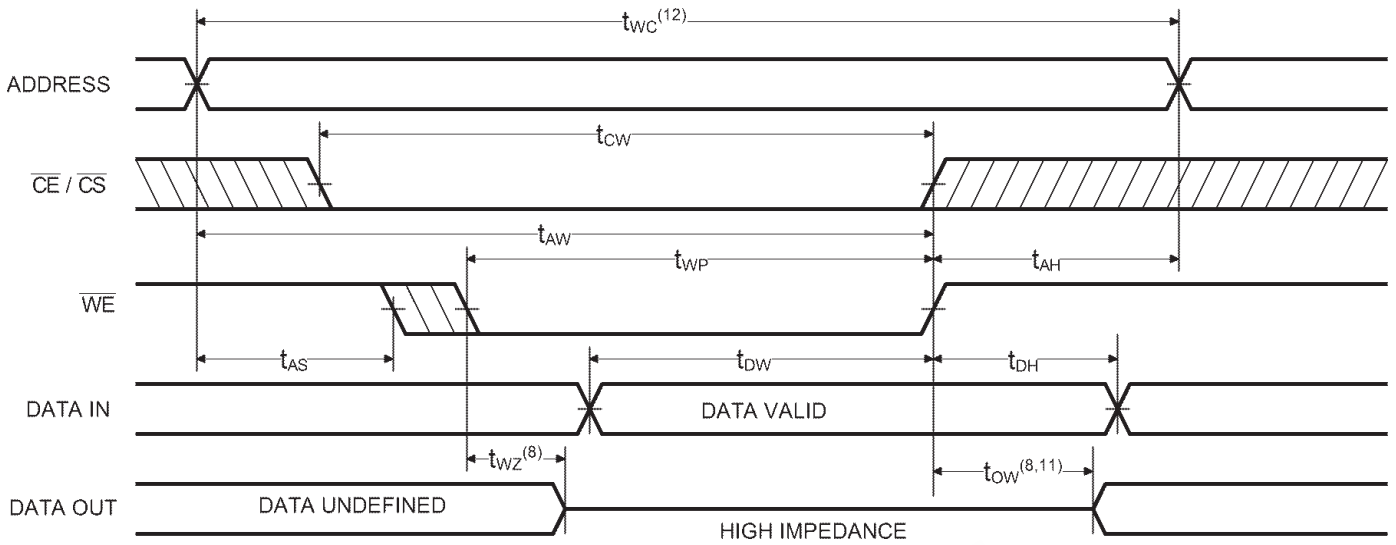
**AC ELECTRICAL CHARACTERISTICS - WRITE CYCLE** $(V_{CC} = 5V \pm 10\%, \text{ All Temperature Ranges})^{(2)}$ 

Sym	Parameter	-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>WC</sub>	Write Cycle Time	12		15		18		20		30		ns
t <sub>cw</sub>	Chip Enable Time to End of Write	12		15		18		20		30		ns
t <sub>AW</sub>	Address Valid to End of Write	12		15		18		20		30		ns
t <sub>AS</sub>	Address Set-up Time	0		0		0		0		0		ns
t <sub>WP</sub>	Write Pulse Width	12		15		18		20		30		ns
t <sub>AH</sub>	Address Hold Time	0		0		0		0		0		ns
t <sub>DW</sub>	Data Valid to End of Write	7		8		10		10		15		ns
t <sub>DH</sub>	Data Hold Time	0		0		0		0		0		ns
t <sub>WZ</sub>	Write Enable to Output in High Z		4		5		6		7		13	ns
t <sub>OW</sub>	Output Active from End of Write	0		0		0		0		0		ns

**AC ELECTRICAL CHARACTERISTICS - WRITE CYCLE (CONTINUED)** $(V_{CC} = 5V \pm 10\%, \text{ All Temperature Ranges})^{(2)}$ 

Sym	Parameter	-45		-55		-70		Unit
		Min	Max	Min	Max	Min	Max	
t <sub>WC</sub>	Write Cycle Time	45		55		70		ns
t <sub>cw</sub>	Chip Enable Time to End of Write	40		50		60		ns
t <sub>AW</sub>	Address Valid to End of Write	40		50		60		ns
t <sub>AS</sub>	Address Set-up Time	0		0		0		ns
t <sub>WP</sub>	Write Pulse Width	40		50		60		ns
t <sub>AH</sub>	Address Hold Time	0		0		0		ns
t <sub>DW</sub>	Data Valid to End of Write	20		20		25		ns
t <sub>DH</sub>	Data Hold Time	3		3		3		ns
t <sub>WZ</sub>	Write Enable to Output in High Z		20		25		30	ns
t <sub>OW</sub>	Output Active from End of Write	0		0		0		ns

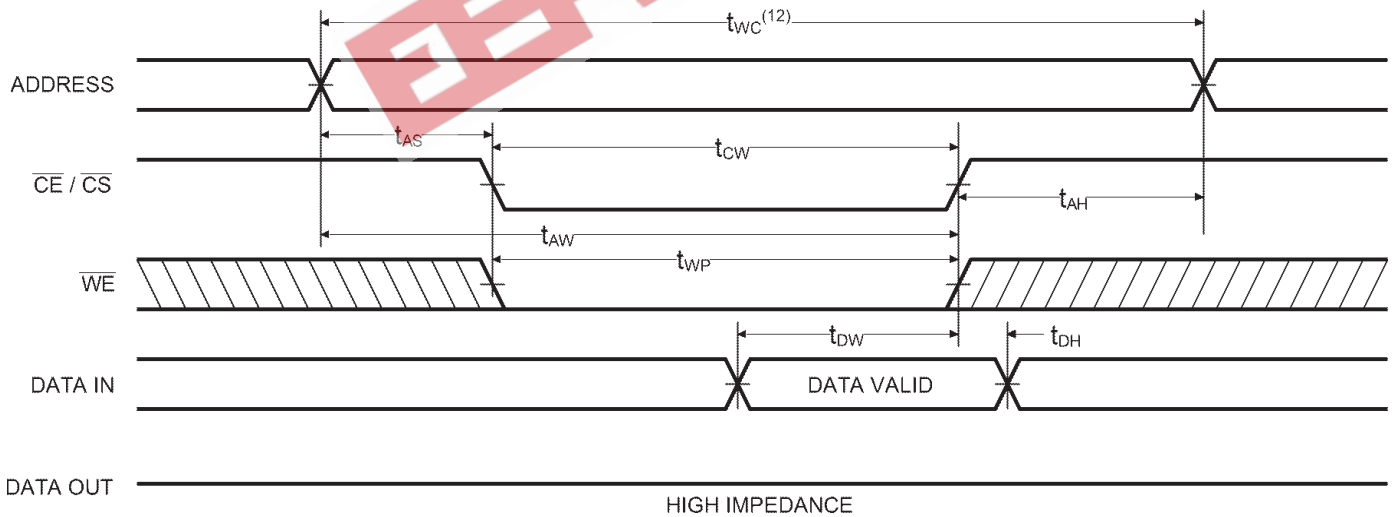
**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED)<sup>(10)</sup>**



**Notes:**

- 10.  $\overline{CE}/\overline{CS}$  and  $\overline{WE}$  must be LOW for WRITE cycle.
- 11. If  $\overline{CE}/\overline{CS}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high impedance state.
- 12. Write Cycle Time is measured from the last valid address to the first transitioning address.

**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CE}/\overline{CS}$  CONTROLLED)<sup>(10)</sup>**



**TRUTH TABLES**

P4C168 (P4C169)

Mode	$\overline{CE}$ ( $\overline{CS}$ )	$\overline{WE}$	Output
Standby (Deselect)	H	X	High Z
Read	L	H	$D_{OUT}$
Write	L	L	High Z

P4C170

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Output
Deselect	H	X	X	High Z
Read	L	H	L	$D_{OUT}$
Output Inhibit	L	H	H	High Z
Write	L	L	X	High Z

### AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

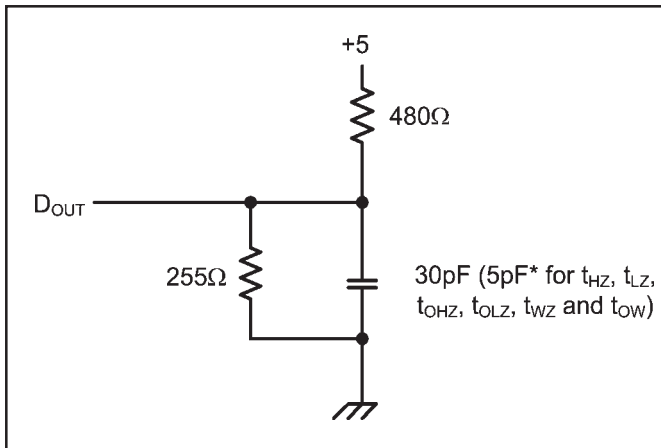


Figure 1. Output Load

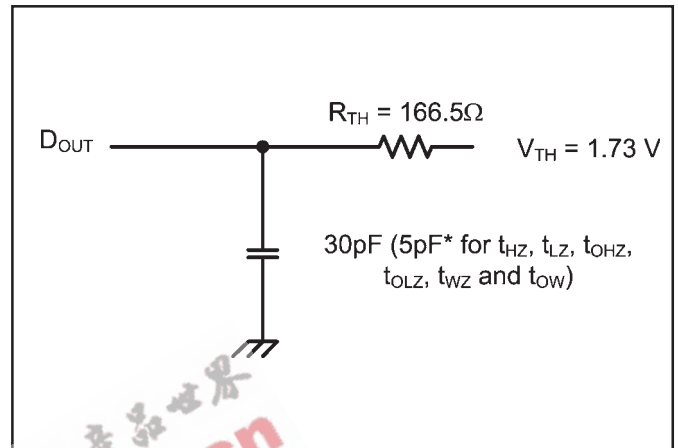


Figure 2. Thevenin Equivalent

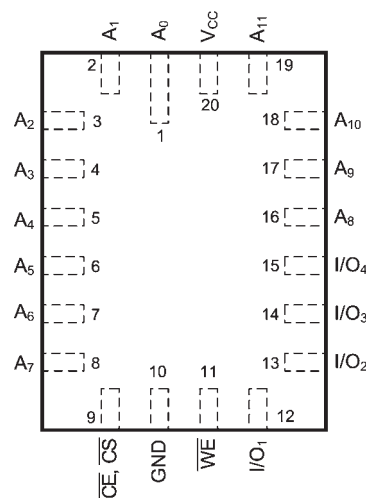
\* including scope and test fixture.

**Note:**

Because of the ultra-high speed of the P4C168, P4C169 AND P4C170 care must be taken when testing these devices; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V<sub>CC</sub> and ground planes directly up to the contactor fingers. A high frequency capacitor of 0.01 μF is also required between V<sub>CC</sub> and ground.

To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D<sub>OUT</sub> to match 166Ω (Thevenin Resistance).

### LCC PIN CONFIGURATION



LCC (L9)

**ORDERING INFORMATION**

P4C168  
P4C169  
P4C170

Device Type	Speed	Package	Processing	
				C 0°C to +70°C
				M -55°C to +125°C
				MB Mil Temp. with MIL-STD-883 Class B Compliance
				C Ceramic Side Brazed DIP, 300 mil
				D Ceramic DIP (CERDIP), 300 mil
				F CERPACK
				FS Solder Seal Flat Pack
				J Plastic SOJ, 300 mil
				L Ceramic LCC (290 x 430 mil)
				P Plastic DIP, 300 mil
				S Plastic SOIC, 300 mil
				12, 15, 20, 25, 35, 45, 55, 70
				4K x 4 SRAM

**SELECTION GUIDE**

The P4C168, P4C169 and P4C170 are available in the following temperature, speed and package options.

Temperature Range	Package	Speed				
		12	15	20	25	35
Commercial Temperature	Plastic DIP	-12PC	-15PC	-20PC	-25PC	N/A
	Plastic SOIC†	-12SC	-15SC	-20SC	-25SC	N/A
	Plastic SOJ††	-12JC	-15JC	-20JC	-25JC	N/A
Military Temperature (P4C168 only)	LCC	N/A	-15LM	-20LM	-25LM	-35LM
	CERDIP	N/A	-15DM	-20DM	-25DM	-35DM
	Side Brazed DIP	N/A	-15CM	-20CM	-25CM	-35CM
	CERPACK	N/A	-15FM	-20FM	-25FM	-35FM
	Solder Seal Flat Pack	N/A	-15FSM	-20FSM	-25FSM	-35FSM
Military Processed* (P4C168 only)	LCC	N/A	-15LMB	-20LMB	-25LMB	-35LMB
	CERDIP	N/A	-15DMB	-20DMB	-25DMB	-35DMB
	Side Brazed DIP	N/A	-15CMB	-20CMB	-25CMB	-35CMB
	CERPACK	N/A	-15FMB	-20FMB	-25FMB	-35FMB
	Solder Seal Flat Pack	N/A	-15FSMB	-20FSMB	-25FSMB	-35FSMB

† P4C168 and P4C169 only.

†† P4C168

\* Military temperature range with MIL-STD-883, Class B processing.

N/A = Not available



**SELECTION GUIDE (CONTINUED)**

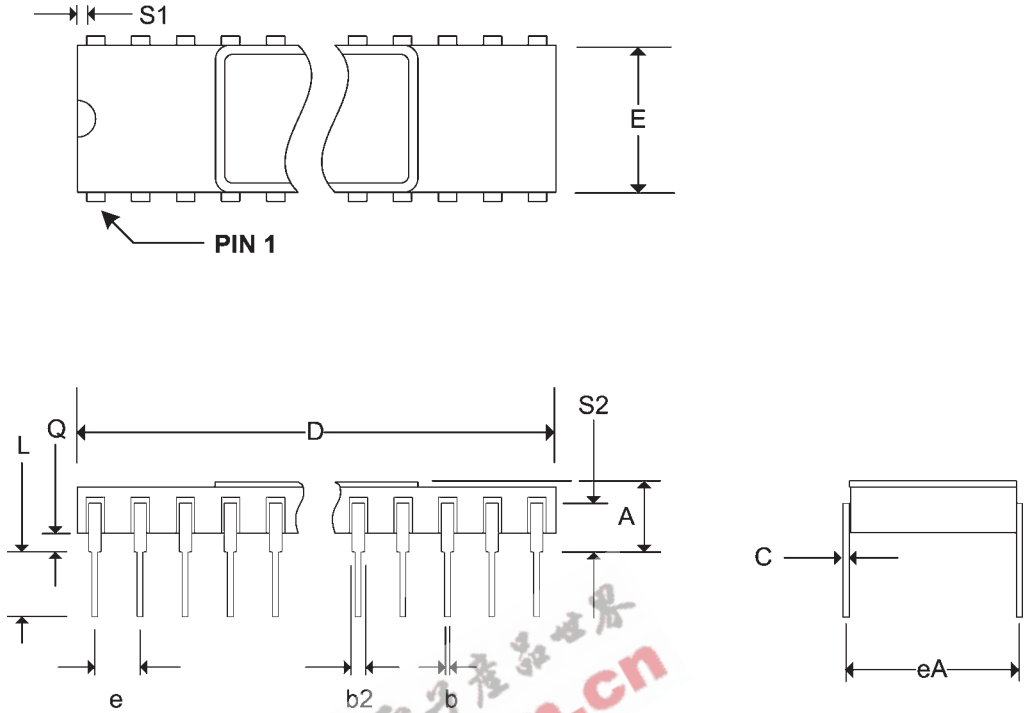
Temperature Range	Package	Speed		
		45	55	70
Military Temperature (P4C168 only)	LCC	-45LM	-55LM	-70LM
	CERDIP	-45DM	-55DM	-70DM
	Side Brazed DIP	-45CM	-55CM	-70CM
	CERPACK	-45FM	-55FM	-70FM
	Solder Seal Flat Pack	-45FSM	-55FSM	-70FSM
Military Processed* (P4C168 only)	LCC	-45LMB	-55LMB	-70LMB
	CERDIP	-45DMB	-55DMB	-70DMB
	Side Brazed DIP	-45CMB	-55CMB	-70CMB
	CERPACK	-45FMB	-55FMB	-70FMB
	Solder Seal Flat Pack	-55FSMB	-55FSMB	-70FSMB

\* Military temperature range with MIL-STD-883, Class B processing.

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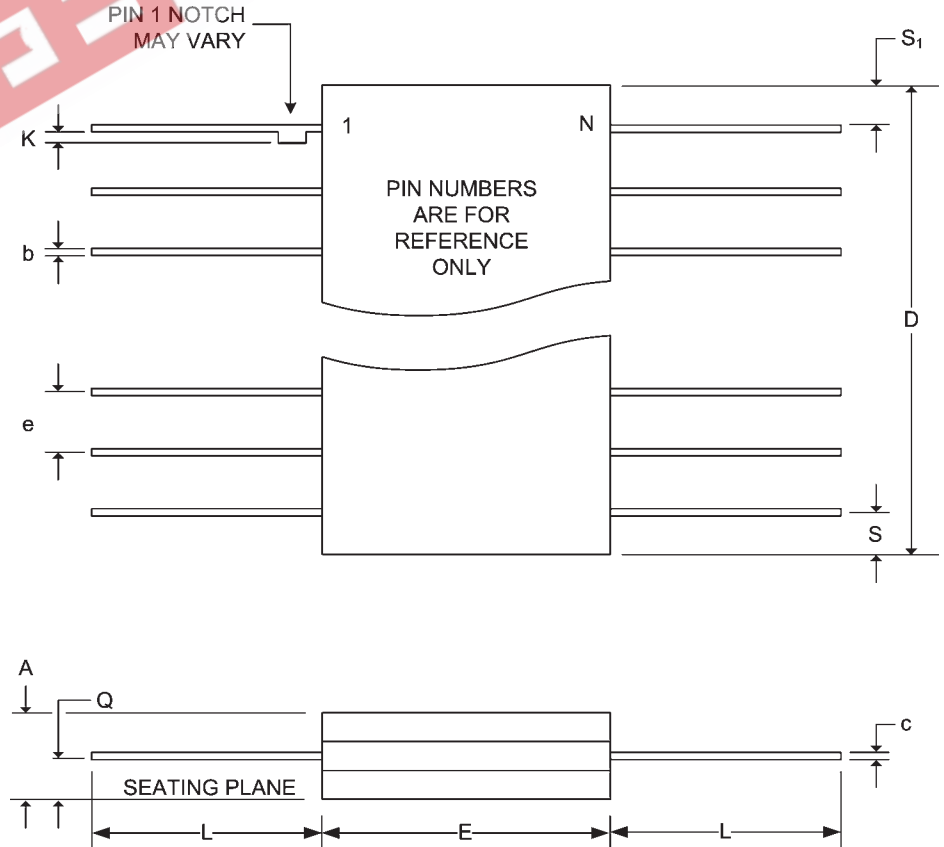
Pkg #	C6	
# Pins	20 (300 mil)	
Symbol	Min	Max
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.060
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-

**SIDE BRAZED DUAL IN-LINE PACKAGE**



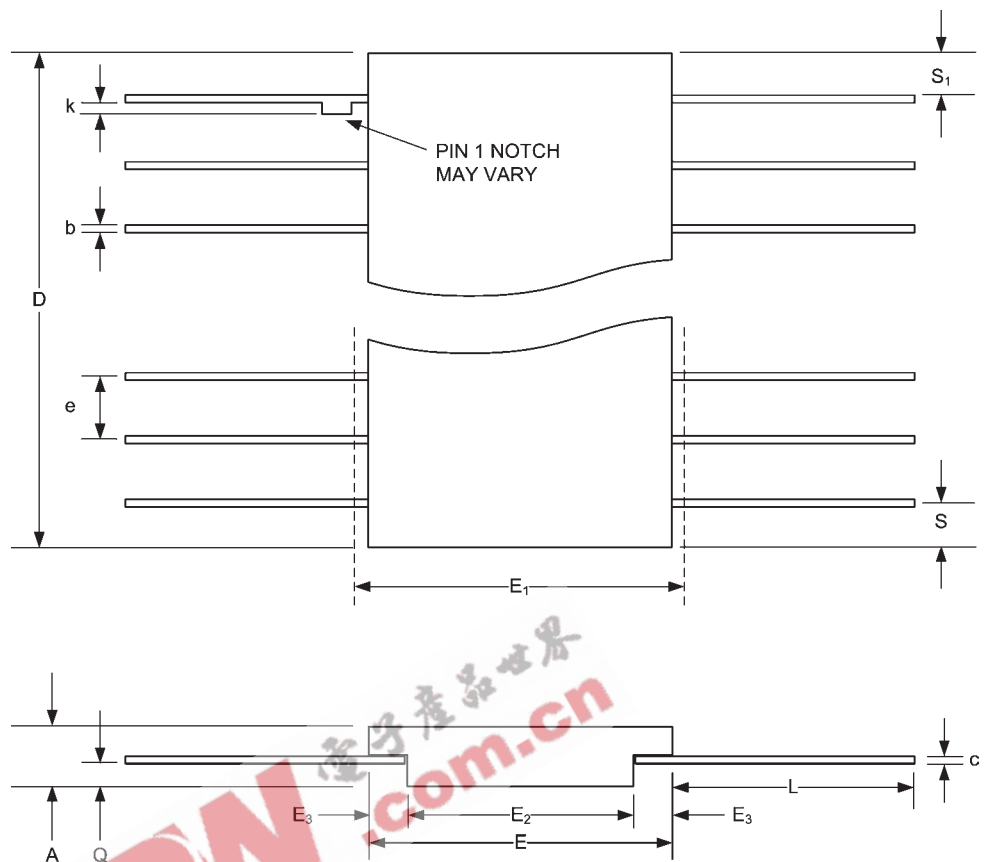
Pkg #	F2	
# Pins	20	
Symbol	Min	Max
A	0.060	0.090
b	0.015	0.022
c	0.004	0.009
D	-	0.530
E	0.305	0.355
e	0.050 BSC	
k	0.005	0.018
L	0.250	0.370
Q	0.026	0.045
S	-	0.085
S1	0.005	-

**CERPACK CERAMIC FLAT PACKAGE**



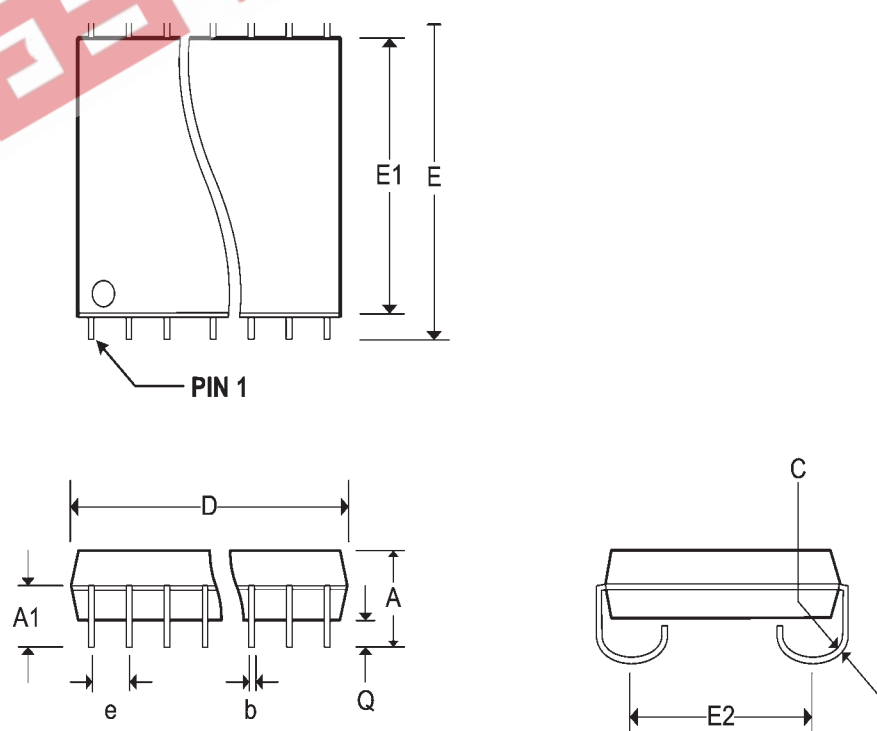
Pkg #	<b>FS-2</b>	
# Pins	20	
Symbol	<b>Min</b>	<b>Max</b>
A	0.045	0.115
b	0.015	0.022
b1	0.015	0.019
c	0.004	0.009
c1	0.004	0.006
D	-	0.540
E	0.245	0.300
E1	-	0.330
E2	0.130	-
E3	0.030	-
e	0.050 BSC	
k	0.008	0.015
L	0.250	0.370
Q	0.026	0.045
S1	0.000	-
M	-	0.0015
N	20	

**SOLDER SEAL FLAT PACKAGE**



Pkg #	<b>J2</b>	
# Pins	20 (300 mil)	
Symbol	<b>Min</b>	<b>Max</b>
A	0.120	0.140
A1	0.080	-
b	0.014	0.020
C	0.008	0.013
D	0.496	0.512
e	0.050 BSC	
E	0.335	0.347
E1	0.292	0.300
E2	0.267 BSC	
Q	0.025	-

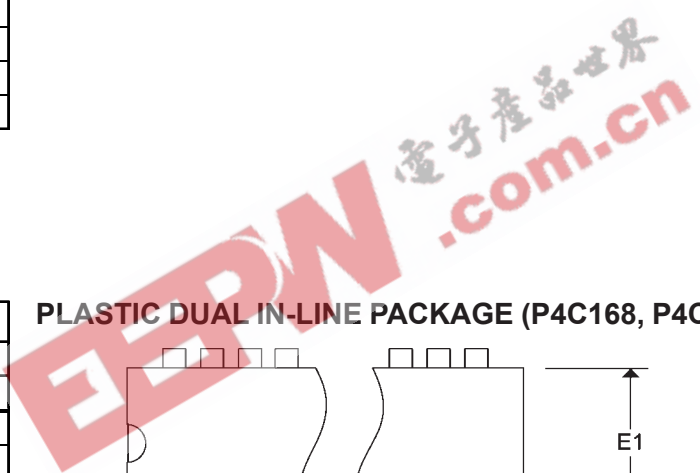
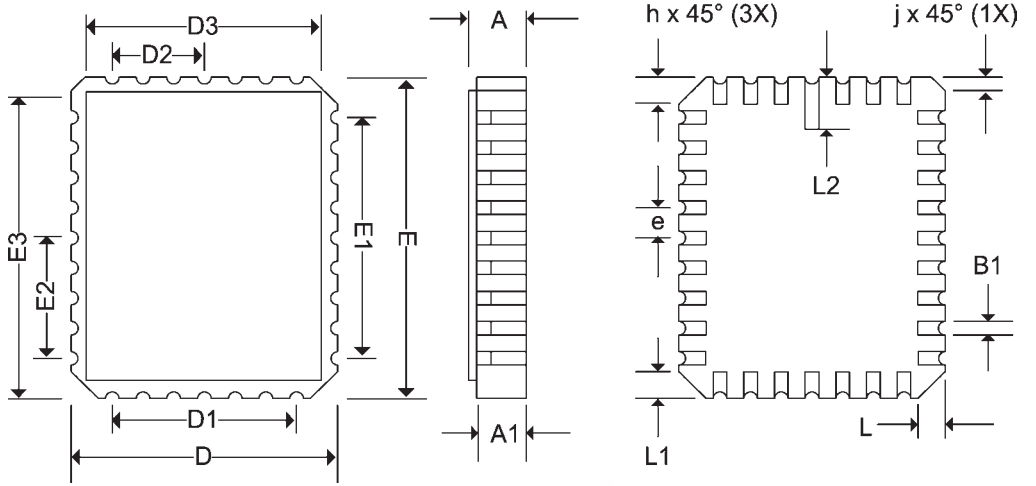
**SOJ SMALL OUTLINE IC PACKAGE**





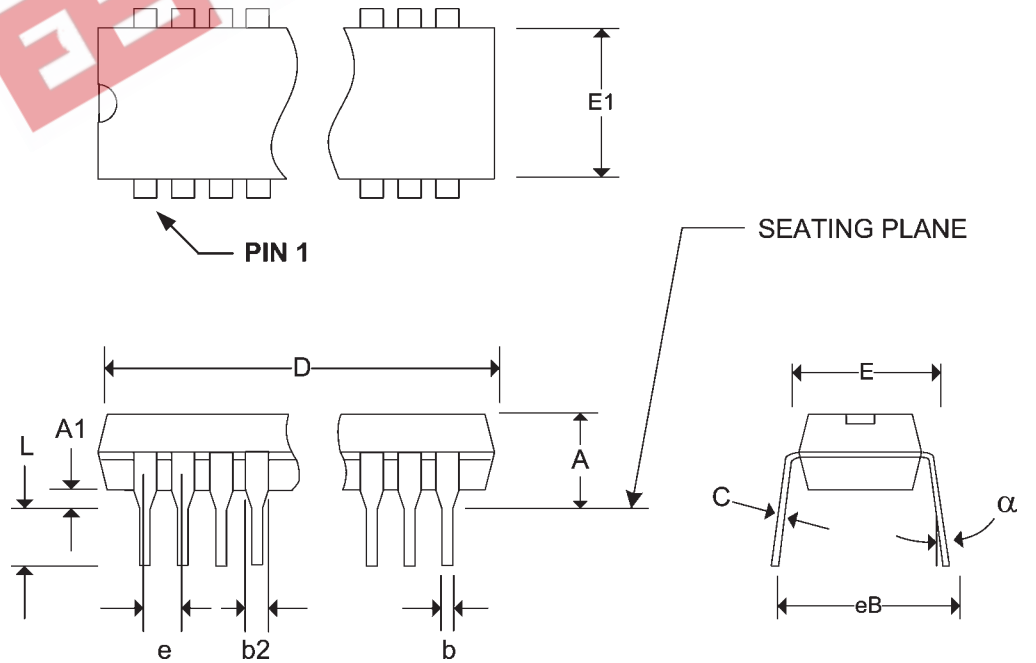
Pkg #	<b>L9</b>	
# Pins	20	
Symbol	<b>Min</b>	<b>Max</b>
A	0.060	0.075
A1	0.050	0.066
B1	0.022	0.028
D	0.280	0.305
D1	0.150 BSC	
D2	0.075 BSC	
D3	-	0.305
E	0.420	0.440
E1	0.250 BSC	
E2	0.125 BSC	
E3	-	0.440
e	0.050 BSC	
h	0.020 REF	
j	0.010 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.098
ND	4	
NE	6	

**RECTANGULAR LEADLESS CHIP CARRIER**



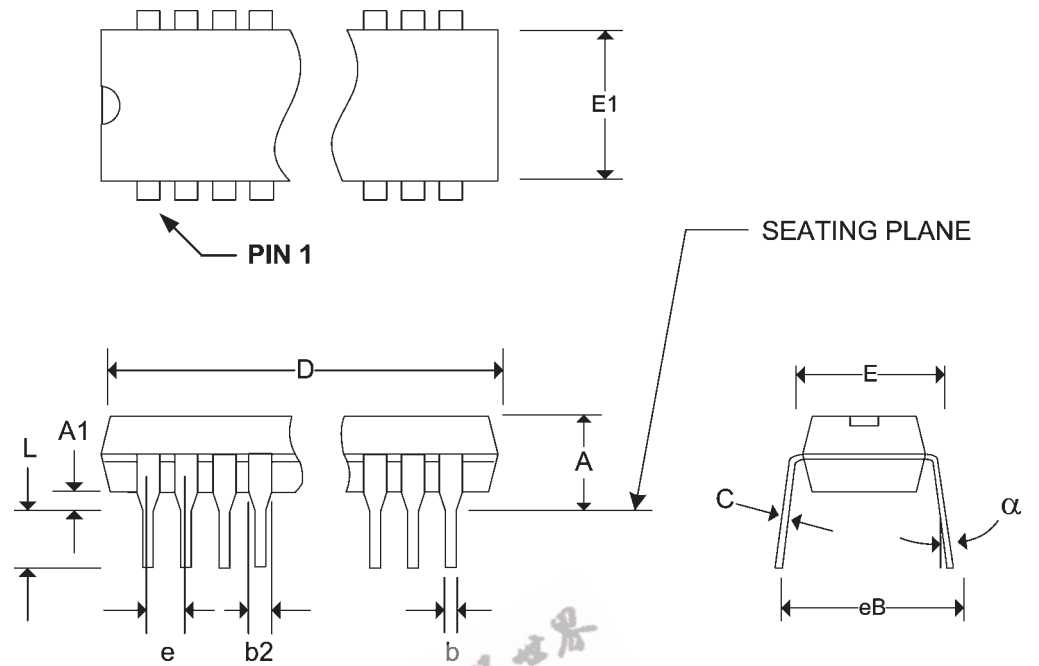
Pkg #	<b>P2</b>	
# Pins	20 (300 mil)	
Symbol	<b>Min</b>	<b>Max</b>
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	0.980	1.060
E1	0.240	0.280
E	0.300	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

**PLASTIC DUAL IN-LINE PACKAGE (P4C168, P4C169)**



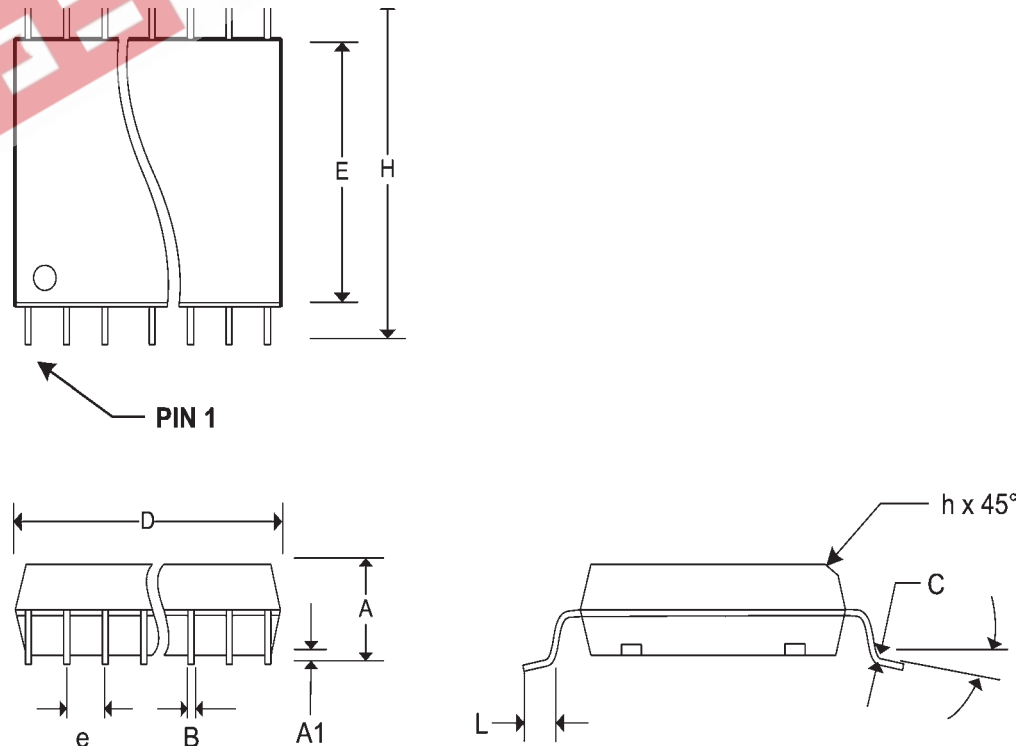
Pkg #	P3	
# Pins	22 (300 Mil)	
Symbol	Min	Max
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	1.145	1.165
E1	0.240	0.280
E	0.300	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
$\alpha$	0°	15°

PLASTIC DUAL IN-LINE PACKAGE (P4C170)



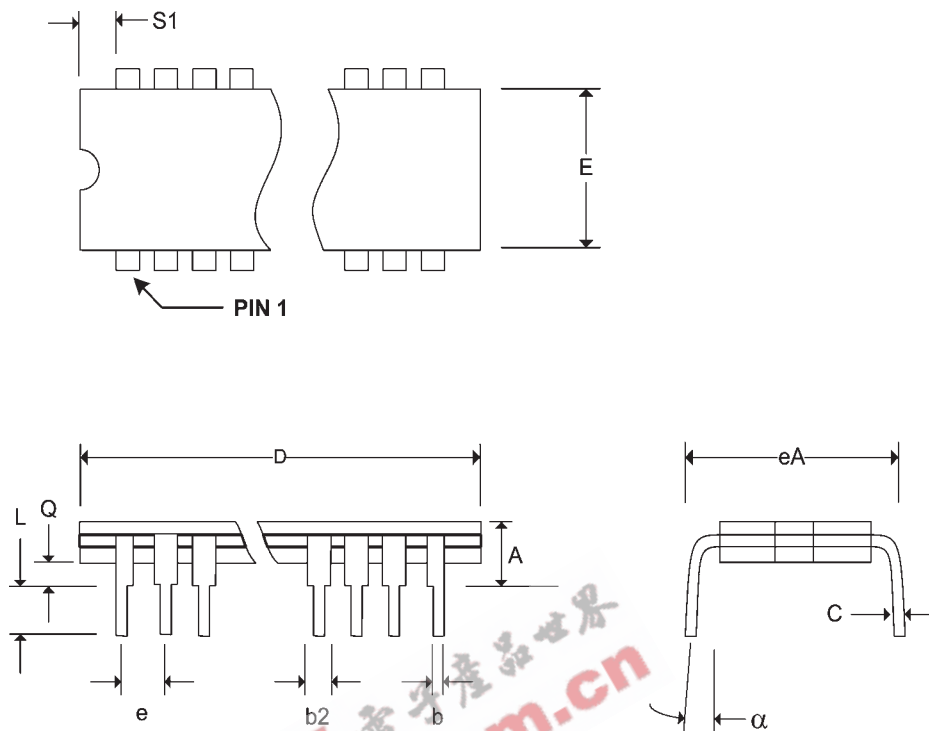
Pkg #	S2	
# Pins	20 (300 mil)	
Symbol	Min	Max
A	0.093	0.104
A1	0.004	0.012
b2	0.013	0.020
C	0.009	0.012
D	0.496	0.511
e	0.050 BSC	
E	0.291	0.299
H	0.394	0.419
h	0.010	0.029
L	0.016	0.050
$\alpha$	0°	8°

SOIC/SOP SMALL OUTLINE IC PACKAGE



Pkg #	D2	
# Pins	20 (300 mil)	
Symbol	Min	Max
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.060
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
$\alpha$	0°	15°

CERDIP DUAL IN-LINE PACKAGE



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### REVISIONS

<b>DOCUMENT NUMBER:</b>		SRAM107	
<b>DOCUMENT TITLE:</b>		P4C168, P4C169, P4C170 ULTRA HIGH SPEED 4K x 4 STATIC CMOS RAMS	
REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-05	JDB	Change logo to Pyramid

