

# P4C422

## HIGH SPEED 256 x 4

### STATIC CMOS RAM

#### FEATURES

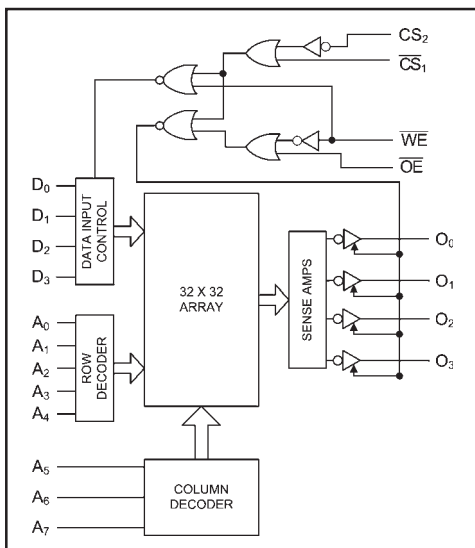
- High Speed (Equal Access and Cycle Times)
  - 10/12/15/20/25/35 ns (Commercial)
  - 15/20/25/35 ns (Military)
- CMOS for Low Power
  - 495 mW Max. - 10/12/15/20/25 (Commercial)
  - 495 mW Max. - 15/20/25/35 (Military)
- Single 5V±10% Power Supply
- Separate I/O
- Fully TTL Compatible Inputs and Outputs
- Resistant to single event upset and latchup resulting from advanced process and design improvements
- Standard 22-pin 400 mil DIP, 24-pin 300 mil SOIC, 24-pin square LCC package and 24-pin CERPACK package

#### DESCRIPTION

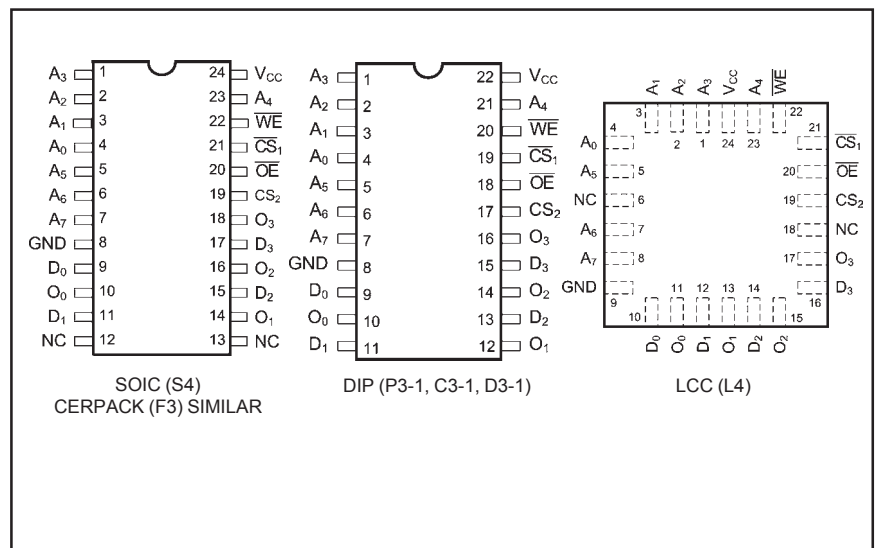
The P4C422 is a 1,024-bit high-speed (10ns) Static RAM with a 256 x 4 organization. The memory requires no clocks or refreshing and has equal access and cycle times. Inputs and outputs are fully TTL compatible. Operation is from a single 5 Volt supply. Easy memory expansion is provided by an active LOW chip select one ( $\overline{CS}_1$ ) and active HIGH chip select two ( $CS_2$ ) as well as 3-state outputs.

In addition to high performance and high density, the device features latch-up protection, single event and upset protection. The P4C422 is offered in several packages: 22-pin 400 mil DIP (plastic and ceramic), 24-pin 300 mil SOIC, 24-pin square LCC and 24-pin CERPACK. Devices are offered in both commercial and military temperature ranges.

#### FUNCTIONAL BLOCK DIAGRAM



#### PIN CONFIGURATIONS



### MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Pin with Respect to GND	-0.5 to +7	V
V <sub>TERM</sub>	Terminal Voltage with Respect to GND (up to 7.0V)	-0.5 to V <sub>CC</sub> +0.5	V
T <sub>A</sub>	Operating Temperature	-55 to +125	°C

Symbol	Parameter	Value	Unit
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	20	mA

### RECOMMENDED OPERATING CONDITIONS

Grade <sup>(2)</sup>	Ambient Temp	Gnd	Vcc
Commercial	0°C to 70°C	0V	5.0V ±10%
Military	-55°C to 125°C	0V	5.0V ±10%

### CAPACITANCES<sup>(4)</sup>

(V<sub>CC</sub> = 5.0V, T<sub>A</sub> = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	5	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	7	pF

### DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage<sup>(2)</sup>

Symbol	Parameter	Test Conditions	P4C422		Unit
			Min	Max	
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -5.2 mA, V <sub>CC</sub> = Min. 2.4		V	
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +8 mA, V <sub>CC</sub> = Min.		0.4	V
V <sub>IH</sub>	Input High Voltage		2.1		V
V <sub>IL</sub>	Input Low Voltage			0.8	V
V <sub>CL</sub>	Input Clamp Diode Voltage	I <sub>IN</sub> = -10 mA	-1.5		V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-10	10	µA
I <sub>OZ</sub>	Output Current (High Z)	V <sub>OL</sub> ≤ V <sub>OUT</sub> ≤ V <sub>OH</sub> , Output Disabled	-10	10	µA
I <sub>OS</sub>	Output Short Circuit Current <sup>(3)</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		90	mA

### POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range							Unit
			-10	-12	-15	-20	-25	-35	
I <sub>CC</sub>	Dynamic Operating Current	Commercial	90	90	90	90	65	65	mA
		Military	N/A	N/A	90	90	90	90	mA

#### Notes:

- Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
- Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
- For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.
- This parameter is sampled and not 100% tested.
- Transition time is ≤ 3ns for 10, 12, and 15 ns products and ≤ 5ns for 20, 25, and 35 ns products, see Fig 1d. Timing is referenced at input and output levels of 1.5V. The output loading is equivalent to the specified I<sub>OL</sub>/I<sub>OH</sub> with a load capacitance of 15 pF (10, 12) or 30 pF (15, 20, 25, 35) as in Fig. 1a and 1b respectively.
- Transition time is ≤ 3ns for 10, 12, and 15 ns products and ≤ 5ns for 20, 25, and 35 ns products, see Fig 1d. Transition is measured at steady state HIGH level -500mV or steady state LOW level +500mV on the output from a level on the input with load shown in Fig. 1c.
- t<sub>w</sub> is measured at t<sub>WSA</sub> = min.; t<sub>WSA</sub> is measured at t<sub>w</sub> = min.

## FUNCTIONAL DESCRIPTION

An active LOW write enable ( $\overline{WE}$ ) controls the writing/reading operation of the memory. When the chip select one ( $\overline{CS}_1$ ) and the write enable ( $\overline{WE}$ ) are LOW and the chip select two ( $CS_2$ ) is HIGH, the information on data inputs ( $D_0$  through  $D_3$ ) is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write

recovery times by eliminating the “write recovery glitch.” Reading is performed with chip select one ( $\overline{CS}_1$ ) LOW, chip select two ( $CS_2$ ) HIGH, write enable ( $\overline{WE}$ ) HIGH and output enable ( $\overline{OE}$ ) LOW. The information stored in the addressed word is read out on the noninverting outputs ( $O_0$  through  $O_3$ ). The outputs of the memory go to an inactive high impedance state whenever chip select one ( $\overline{CS}_1$ ) is HIGH, or during the write operation when write enable ( $\overline{WE}$ ) is LOW.

## TRUTH TABLE

Mode	$CS_2$	$\overline{CS}_1$	$\overline{WE}$	$\overline{OE}$	Output
Standby	L	X	X	X	High Z
Standby	X	H	X	X	High Z
$D_{OUT}$ Disabled	H	L	X	H	High Z
Read	H	L	H	L	$D_{OUT}$
Write	H	L	L	X	High Z

Notes:

H = HIGH

L = Low

X = Don't Care

HIGH Z = Implies outputs are disabled or off. This condition is defined as high impedance state for the P4C422.

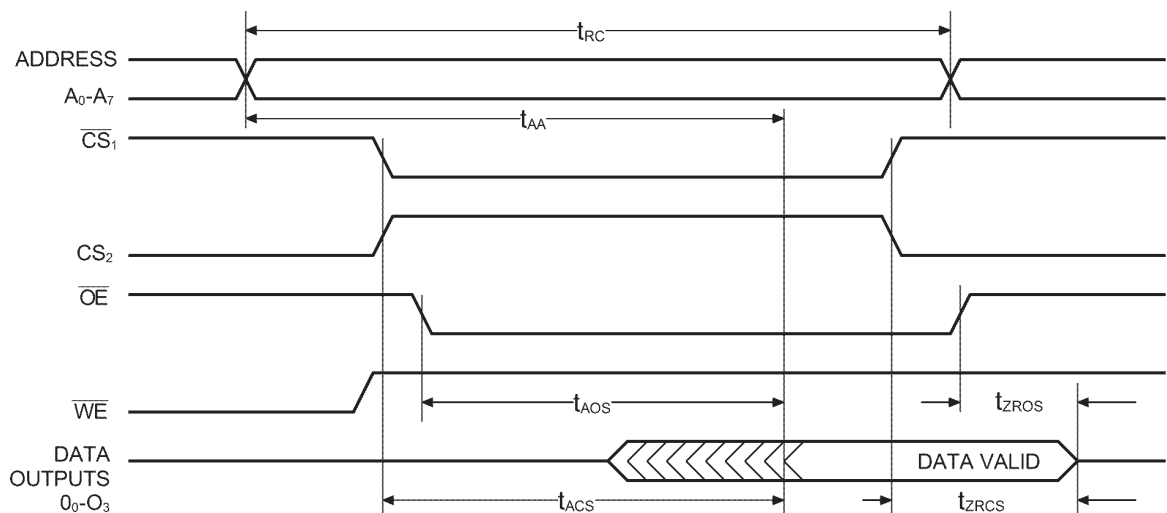
## AC ELECTRICAL CHARACTERISTICS—READ CYCLE

( $V_{CC} = 5V \pm 10\%$  except as noted, All Temperature Ranges)<sup>(2)</sup>

Sym.	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{RC}$	Read Cycle Time <sup>(5)</sup>	12		12		15		20		25		35		ns
$t_{ACS}$	Chip Select Time <sup>(5)</sup>		7.5		8		8		12		15		25	ns
$t_{ZRCS}$	Chip Select to High-Z <sup>(6)</sup>		8		10		12		15		20		30	ns
$t_{AOS}$	Output Enable Time		7.5		8		8		12		15		25	ns
$t_{ZROS}$	Output Enable to High-Z <sup>(6)</sup>		8		10		12		15		20		30	ns
$t_{AA}$	Address Access Time <sup>(5)</sup>		10		12		15		20		25		35	ns

\* $V_{CC} = 5V \pm 5\%$

## TIMING WAVEFORM OF READ CYCLE



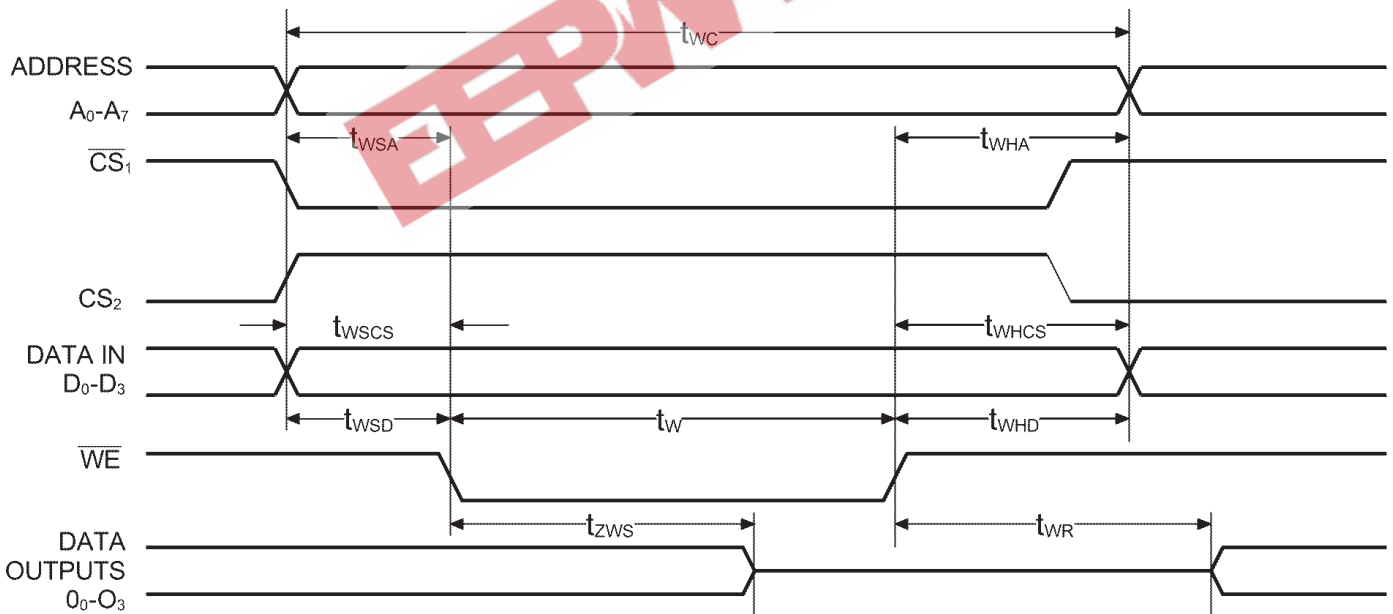
### AC CHARACTERISTICS—WRITE CYCLE

( $V_{CC} = 5V \pm 10\%$  except as noted, All Temperature Ranges)<sup>(2)</sup>

Sym.	Parameter	-10*		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$t_{WC}$	Write Cycle Time <sup>(5)</sup>	10		12		15		20		25		35		ns
$t_{ZWS}$	Write Enable to High-Z <sup>(6)</sup>		8		10		12		15		20		30	ns
$t_{WR}$	Write Recovery Time		8		10		12		15		20		25	ns
$t_W$	Write Pulse Width <sup>(5,7)</sup>	8		9		11		13		15		20		ns
$t_{WSD}$	Data Setup Time Prior to Write <sup>(5)</sup>	0		0		0		2		5		5		ns
$t_{WHD}$	Data Hold Time <sup>(5)</sup>	2		2		2		5		5		5		ns
$t_{WSA}$	Address Setup Time <sup>(5,7)</sup>	0		0		0		2		5		5		ns
$t_{WHA}$	Address Hold Time <sup>(5)</sup>	2		2		4		5		5		5		ns
$t_{WSCS}$	Chip Select Setup Time <sup>(5)</sup>	0		0		0		2		5		5		ns
$t_{WHCS}$	Chip Select Hold Time <sup>(5)</sup>	2		2		2		5		5		5		ns

\* $V_{CC} = 5V \pm 5\%$

### TIMING WAVEFORM OF WRITE CYCLE



**AC TEST LOADS & WAVEFORMS**

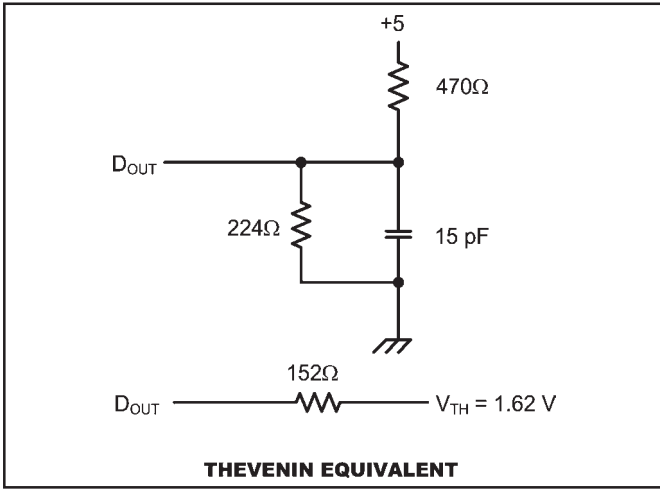


Figure 1a

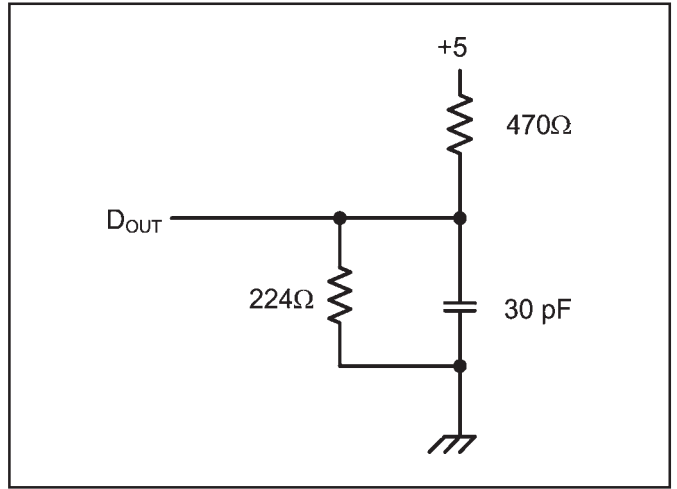


Figure 1b

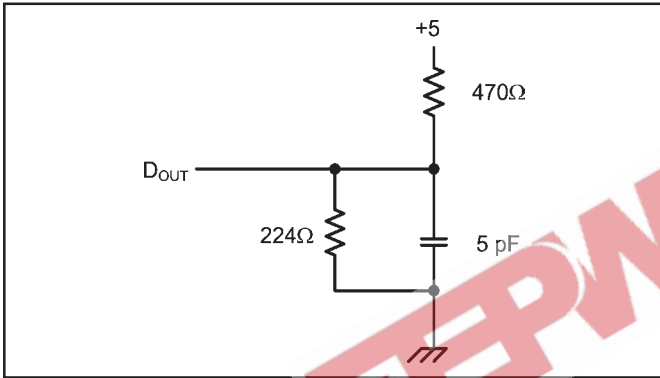


Figure 1c

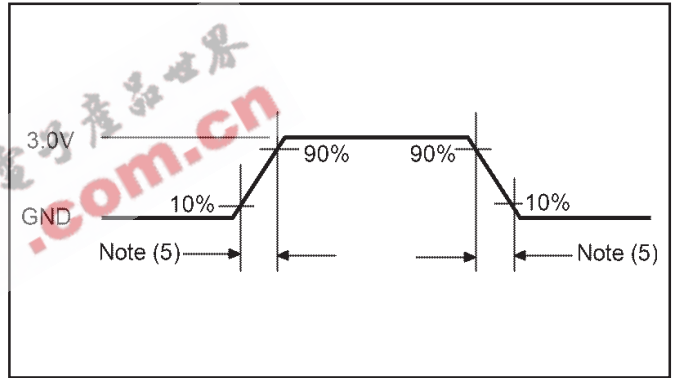
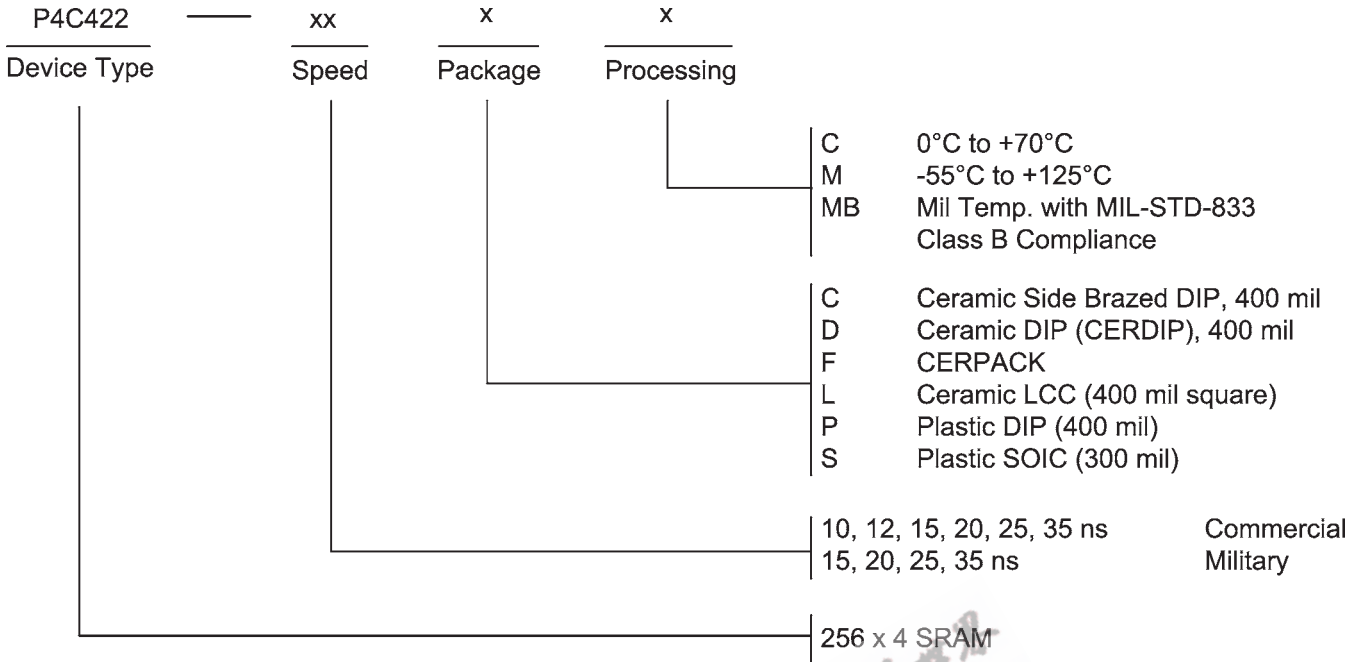


Figure 1d

### ORDERING INFORMATION



### SELECTION GUIDE

The P4C422 is available in the following temperature range, speed, and package options.

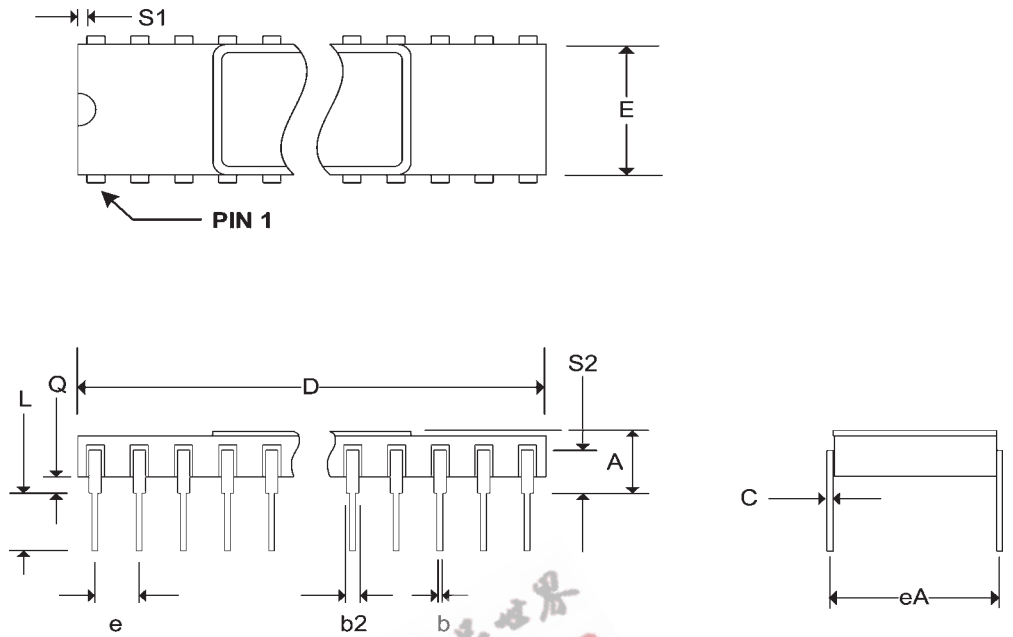
Temperature Range	Package	Speed (ns)					
		10	12	15	20	25	35
Commercial Temperature	Plastic DIP	-10PC	-12PC	-15PC	-20PC	-25PC	-35PC
	SOIC	-10SC	-12SC	-15SC	-20SC	-25SC	-35SC
Military Temperature	Side Brazed DIP	N/A	N/A	-15CM	-20CM	-25CM	-35CM
	CERDIP	N/A	N/A	-15DM	-20DM	-25DM	-35DM
	LCC	N/A	N/A	-15LM	-20LM	-25LM	-35LM
	CERPACK	N/A	N/A	-15FM	-20FM	-25FM	-35FM
Military Processed*	Side Brazed DIP	N/A	N/A	-15CMB	-20CMB	-25CMB	-35CMB
	CERDIP	N/A	N/A	-15DMB	-20DMB	-25DMB	-35DMB
	LCC	N/A	N/A	-15LMB	-20LMB	-25LMB	-35LMB
	CERPACK	N/A	N/A	-15FMB	-20FMB	-25FMB	-35FMB

\*Military temperature range with MIL-STD-883, Class B compliance.

N/A = Not Available

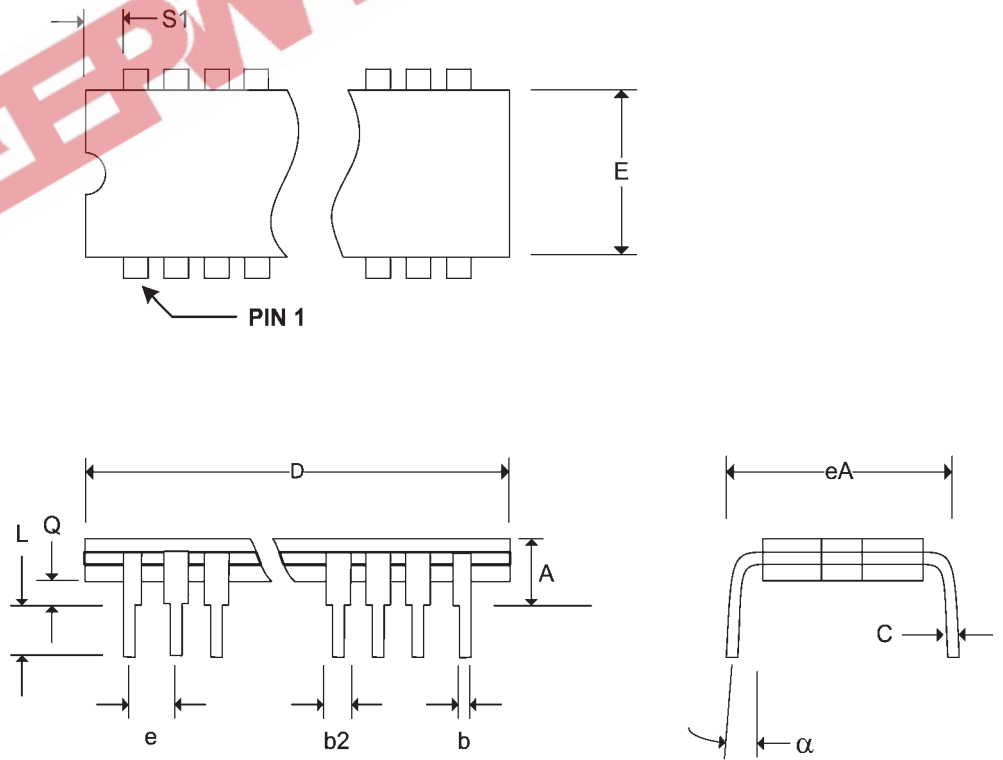
Pkg #	<b>C3-1</b>	
# Pins	22 (400 Mil)	
Symbol	<b>Min</b>	<b>Max</b>
A	-	0.200
b	0.014	0.026
b2	0.035	0.060
C	0.008	0.015
D	-	1.100
E	0.360	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

**SIDE BRAZED DUAL IN-LINE PACKAGE**



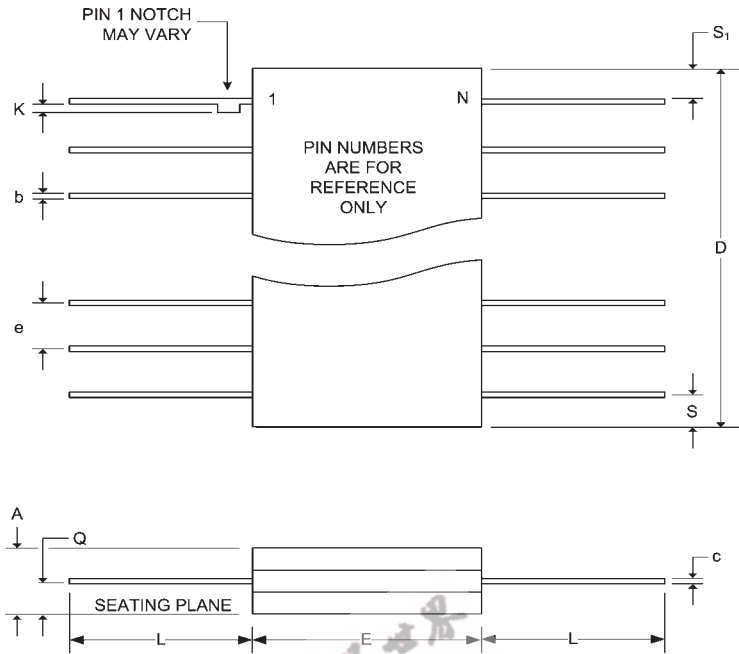
Pkg #	<b>D3-1</b>	
# Pins	22 (400 Mil)	
Symbol	<b>Min</b>	<b>Max</b>
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.111
E	0.350	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
$\alpha$	0°	15°

**CERDIP DUAL IN-LINE PACKAGE**



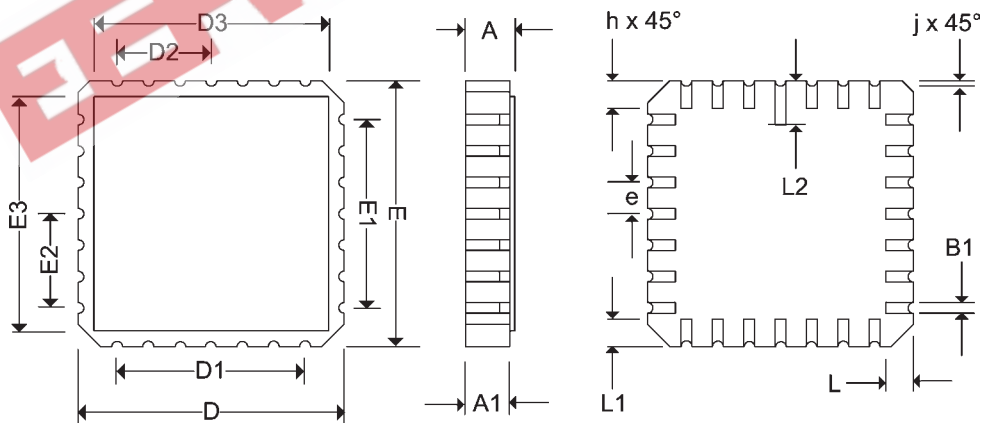
Pkg #	<b>F3</b>	
# Pins	24	
Symbol	<b>Min</b>	<b>Max</b>
A	0.060	0.090
b	0.015	0.022
c	0.004	0.009
D	-	0.630
E	0.330	0.380
e	0.050 BSC	
k	0.008	0.015
L	0.250	0.370
Q	0.026	0.045
S	-	0.085
S1	0.005	-

**CERPACK CERAMIC FLAT PACKAGE**



Pkg #	<b>L4</b>	
# Pins	24	
Symbol	<b>Min</b>	<b>Max</b>
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D/E	0.395	0.410
D1/E1	0.250 BSC	
D2/E2	0.125 BSC	
D3/E3	-	0.410
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	6	
NE	6	

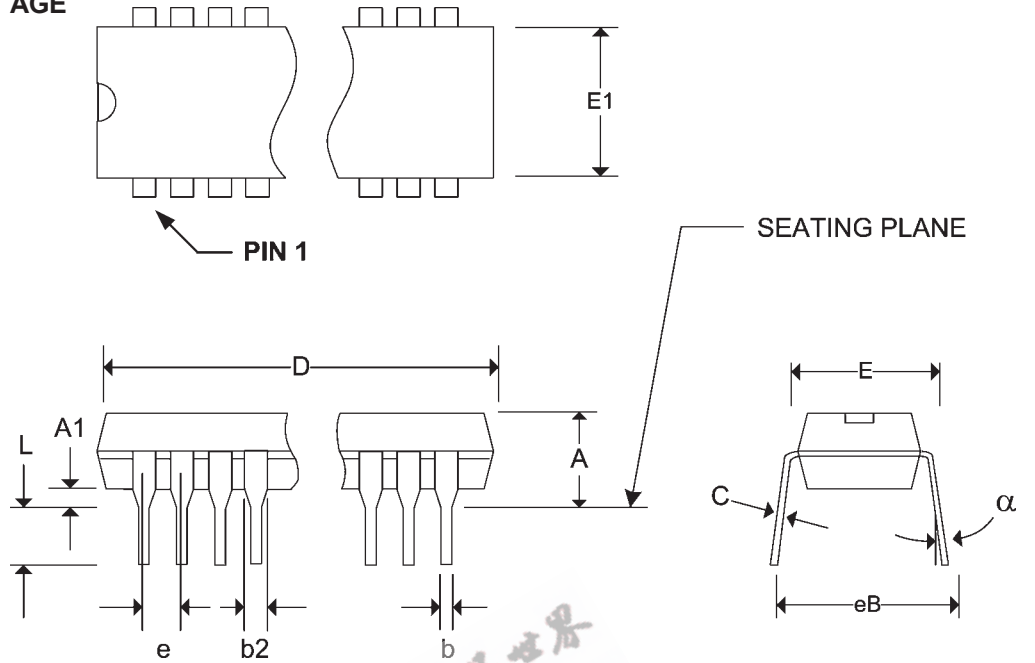
**SQUARE LEADLESS CHIP CARRIER**





Pkg #	P3-1	
# Pins	22 (400 Mil)	
Symbol	Min	Max
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.065
C	0.009	0.015
D	1.065	1.120
E1	0.330	0.390
E	0.390	0.425
e	0.100 BSC	
eB	-	0.500
L	0.115	0.160
$\alpha$	0°	15°

**PLASTIC DUAL IN-LINE PACK-AGE**



Pkg #	S4	
# Pins	24 (300 Mil)	
Symbol	Min	Max
A	0.093	0.104
A1	0.004	0.012
b2	0.013	0.020
C	0.009	0.012
D	0.598	0.614
e	0.050 BSC	
E	0.291	0.299
H	0.394	0.419
h	0.010	0.029
L	0.016	0.050
$\alpha$	0°	8°

**SMALL OUTLINE IC PLASTIC PACKAGE**

