4-Bit D-Type Register with Three-State Outputs

The MC14076B 4—Bit Register consists of four D—type flip—flops operating synchronously from a common clock. OR gated output—disable inputs force the outputs into a high—impedance state for use in bus organized systems. OR gated data—disable inputs cause the Q outputs to be fed back to the D inputs of the flip—flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master root is provided to clear all four flip—flops simultaneously independent of the clock or disable inputs.

- Three–State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1.)

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P _D	Power Dissipation, per Package (Note 2.)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature (8–Second Soldering)	260	°C

- Maximum Ratings are those values beyond which damage to the device may occur.
- 2. Temperature Derating:

Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}.$

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



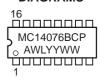
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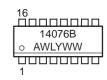


PDIP-16 P SUFFIX CASE 648





SOIC-16 D SUFFIX CASE 751B



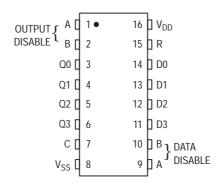
A = Assembly Location

WL or L = Wafer Lot YY or Y = Year WW or W = Work Week

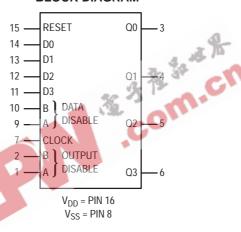
ORDERING INFORMATION

Device	Package	Shipping		
MC14076BCP	PDIP-16	2000/Box		
MC14076BD	SOIC-16	2400/Box		
MC14076BDR2	SOIC-16	2500/Tape & Reel		

PIN ASSIGNMENT



BLOCK DIAGRAM



FUNCTION TABLE

		Data D	isable	Data	Output
Reset	Clock	A B		D	Q
1	Х	Х	Х	Х	0
0	0	Х	Х	Х	Qn
0		1	Х	Х	Qn
0		Х	1	Х	Qn
0		0	0	0	0
0		0	0	1	1

When either output disable A or B (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected. X = Don't Care.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

		V _{DD}	- 5	5°C		25°C		125	5°C	
Characteristic	Symbol	Vdc	Min	Max	Min	Тур ^(3.)	Max	Min	Max	Unit
Output Voltage "0" Level V _{in} = V _{DD} or 0	V _{OL}	5.0 10 15	_ _ _	0.05 0.05 0.05	_ _ _	0 0 0	0.05 0.05 0.05	_ _ _	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$ "1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	_ _ _	4.95 9.95 14.95	5.0 10 15	_ _ _	4.95 9.95 14.95	_ _ _	Vdc
Input Voltage "0" Level (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0 10 15	_ _ _	1.5 3.0 4.0		2.25 4.50 6.75	1.5 3.0 4.0		1.5 3.0 4.0	Vdc
"1" Level $(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$	V _{IH}	5.0 10 15	3.5 7.0 11	_ _ _	3.5 7.0 11	2.75 5.50 8.25	_ _ _	3.5 7.0 11	_ _ _	Vdc
Output Drive Current $(V_{OH} = 2.5 \text{ Vdc}) \qquad \text{Source}$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$	I _{OH}	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	_ _ _ _	- 2.4 - 0.51 - 1.3 - 3.4	-4.2 -0.88 -2.25 -8.8	_ _ _ _	- 1.7 - 0.36 - 0.9 - 2.4	_ _ _ _	mAdc
$(V_{OL} = 0.4 \text{ Vdc})$ Sink $(V_{OL} = 0.5 \text{ Vdc})$ $(V_{OL} = 1.5 \text{ Vdc})$	l _{OL}	5.0 10 15	0.64 1.6 4.2	-	0.51 1.3 3.4	0.88 2. 25 8.8	_ _ _	0.36 0.9 2.4	_ _ _	mAdc
Input Current	l _{in}	15	A	± 0.1	© , ∪,	±0.00001	± 0.1	_	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}			- 1	_	5.0	7.5	_	_	pF
Quiescent Current (Per Package)	I _{DD}	5.0 10 15	_	5.0 10 20	_ _ _	0.005 0.010 0.015	5.0 10 20	_ _ _	150 300 600	μAdc
Total Supply Current (4.) (5.) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15			$I_{T} = (1$.75 μΑ/kHz) .50 μΑ/kHz) .25 μΑ/kHz)	f + I _{DD}			μAdc
Three-State Leakage Current	I _{TL}	15	_	± 0.1	_	± 0.0001	± 0.1	_	± 3.0	μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

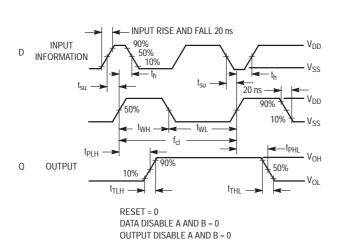
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (6.) (C $_L$ = 50 pF, T_A = 25 $^{\circ}$ C)

Characteristic	Symbol	V _{DD} Vdc	Min	Тур ^(7.)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) \text{ C}_{L} + 25 \text{ ns} \\ t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) \text{ C}_{L} + 12.5 \text{ ns} \\ t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) \text{ C}_{L} + 9.5 \text{ ns} \\ \end{cases}$	t _{TLH} , t _{THL}	5.0 10 15	_ _ _	100 50 40	200 100 80	ns
Propagation Delay Time Clock to Q $t_{PLH},t_{PHL}=(1.7\;\text{ns/pF})\;C_L+215\;\text{ns} \\ t_{PLH},t_{PHL}=(0.66\;\text{ns/pF})\;C_L+92\;\text{ns} \\ t_{PLH},t_{PHL}=(0.5\;\text{ns/pF})\;C_L+65\;\text{ns} \\ \end{cases}$	t _{PLH} , t _{PHL}	5.0 10 15	_ _ _	300 125 90	600 250 180	ns
Reset to Q t_{PLH} , t_{PHL} = (1.7 ns/pF) C_L + 215 ns t_{PLH} , t_{PHL} = (0.66 ns/pF) C_L + 92 ns t_{PLH} , t_{PHL} = (0.5 ns/pF) C_L + 65 ns		5.0 10 15	_ _ _	300 125 90	600 250 180	
3–State Propagation Delay, Output "1" or "0" to High Impedance	t _{PHZ} , t _{PLZ}	5.0 10 15	_ _ _	150 60 45	300 120 90	ns
3–State Propagation Delay, High Impedance to "1" or "0" Level	t _{PZH} , t _{PZL}	5.0 10 15	3	200 80 60	400 160 120	ns
Clock Pulse Width	t _{WH}	5.0 10 1 5	260 110 80	130 55 40	_ _ _	ns
Reset Pulse Width	t _{WH}	5.0 10 15	370 150 110	185 75 55	_ _ _	ns
Data Setup Time	t _{su}	5.0 10 15	30 10 4	15 5 2	_ _ _	ns
Data Hold Time	t _h	5.0 10 15	130 60 50	65 30 25	_ _ _	ns
Data Disable Setup Time	t _{su}	5.0 10 15	220 80 50	110 40 25	_ _ _	ns
Clock Pulse Rise and Fall Time	t _{TLH} , t _{THL}	5.0 10 15	_ _ _	_ _ _	15 5 4	μs
Clock Pulse Frequency	f _{cl}	5.0 10 15	_ _ _	3.6 9.0 12	1.8 4.5 6.0	MHz

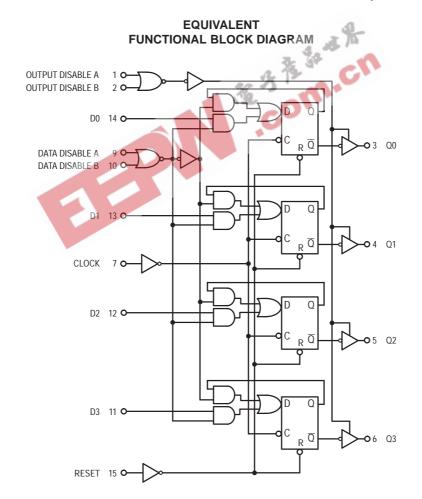
^{6.} The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



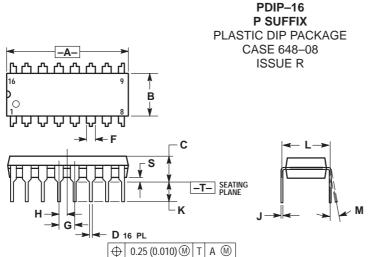
← 20 ns **∠**20 ns OUTPUT V_{DD} 90% DISABLE 10% A OR B V_{SS} — t_{PZL} V_{OH} ANY Q ≈ 2.5 V @ $V_{DD} = 5$ V, OUTPUT 10% 10 V, AND 15 V ≈ 2 V @ V_{DD} = 5 V ► t_{PHZ} t_{P7H} \approx 6 V @ V_{DD} = 10 V 90% ANY Q $\approx 10 \text{ V } @ V_{DD} = 15 \text{ V}$ OUTPUT V_{OL} OUTPUTS OUTPUTS — OUTPUTS — CONNECTED CONNECTED DISCONNECTED ANY Q OUTPUT OTHER OTHER | 8 $R_L=1\,k\Omega$ $\begin{array}{l} R_L = 1 \text{ k}\Omega \\ \hline \\ V_{SS} \text{ FOR t}_{PLZ} \text{ AND t}_{PZL} \\ \end{array}$ MC14076B 立_Cr OUTPUT o DISABLE A OR B

Figure 1. Timing Diagram

Figure 2. Three–State Propagation Delay Waveshape and Circuit



PACKAGE DIMENSIONS



NOTES:

- NOTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: INCH.

 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.

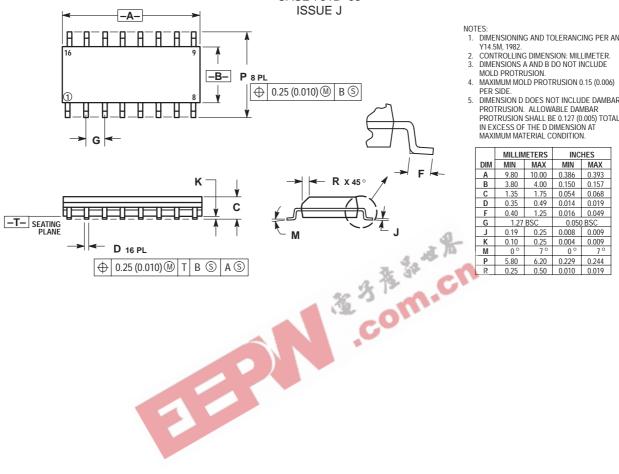
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	METERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
Н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
K	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
M	0°	10 °	0°	10 °	
S	0.020	0.040	0.51	1.01	

PACKAGE DIMENSIONS

SOIC-16 **D SUFFIX** PLASTIC SOIC PACKAGE CASE 751B-05



⊕ 0.25 (0.010) M T B S A S

NOTES:

- NOTES:
 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2 CONTROLLING DIMENSION: MILLIMETER.
 3 DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4 MAXIMUM MOLD PROTRUSION 0.15 (0.006) PED SIGE.
- 4. MAXIMUM MOLLP PROTROSION 0.15 (0.006)
 PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	1.27 BSC		BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7°	0 °	7°
Р	5.80	6.20	0.229	0.244
D	0.25	0.50	0.010	0.010



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