# MC14076B

# 4-Bit D-Type Register with Three-State Outputs

The MC14076B 4–Bit Register consists of four D–type flip–flops operating synchronously from a common clock. OR gated output–disable inputs force the outputs into a high–impedance state for use in bus organized systems. OR gated data–disable inputs cause the Q outputs to be fed back to the D inputs of the flip–flops. Thus they are inhibited from changing state while the clocking process remains undisturbed. An asynchronous master root is provided to clear all four flip–flops simultaneously independent of the clock or disable inputs.

- Three–State Outputs with Gated Control Lines
- Fully Independent Clock Allows Unrestricted Operation for the Two Modes: Parallel Load and Do Nothing
- Asynchronous Master Reset
- Four Bus Buffer Registers
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

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## MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$) (Note 1.)

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{DD}$ | DC Supply Voltage Range | −0.5 to +18.0 | V |
| $V_{in}$, $V_{out}$ | Input or Output Voltage Range (DC or Transient) | −0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$, $I_{out}$ | Input or Output Current (DC or Transient) per Pin | ±10 | mA |
| $P_D$ | Power Dissipation, per Package (Note 2.) | 500 | mW |
| $T_A$ | Ambient Temperature Range | −55 to +125 | °C |
| $T_{stg}$ | Storage Temperature Range | −65 to +150 | °C |
| $T_L$ | Lead Temperature (8–Second Soldering) | 260 | °C |

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
   Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
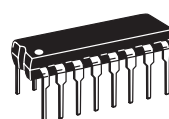
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.
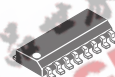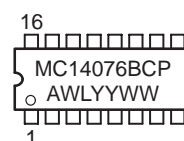
# MC14076B

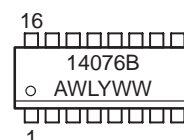## PIN ASSIGNMENT



```
                    ┌────────┐
OUTPUT   A  [ 1 ●   │    16 ]  V_DD
DISABLE  B  [ 2     │    15 ]  R
         Q0 [ 3     │    14 ]  D0
         Q1 [ 4     │    13 ]  D1
         Q2 [ 5     │    12 ]  D2
         Q3 [ 6     │    11 ]  D3
         C  [ 7     │    10 ]  B   DATA
         V_SS [ 8   │     9 ]  A   DISABLE
                    └────────┘
```

## BLOCK DIAGRAM



```
15 ──── RESET         Q0 ──── 3
14 ──── D0
13 ──── D1
12 ──── D2           Q1 ──── 4
11 ──── D3
10 ──── B  DATA
 9 ──── A  DISABLE    Q2 ──── 5
 7 ──── CLOCK
 2 ──── B  OUTPUT
 1 ──── A  DISABLE    Q3 ──── 6
```
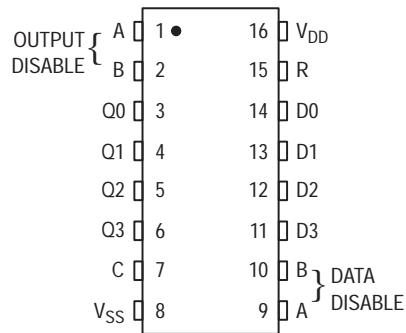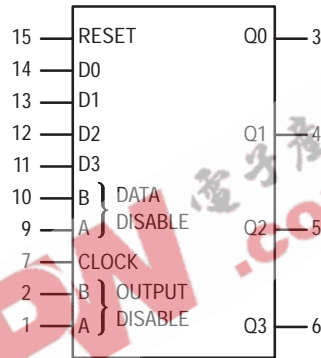
V_DD = PIN 16
V_SS = PIN 8

## FUNCTION TABLE

| Inputs | | | | | Output |
| --- | --- | --- | --- | --- | --- |
| | | Data Disable | | Data | |
| Reset | Clock | A | B | D | Q |
| 1 | X | X | X | X | 0 |
| 0 | 0 | X | X | X | $Q_n$ |
| 0 | ⌐ | 1 | X | X | $Q_n$ |
| 0 | ⌐ | X | 1 | X | $Q_n$ |
| 0 | ⌐ | 0 | 0 | 0 | 0 |
| 0 | ⌐ | 0 | 0 | 1 | 1 |

When either output disable A or B (or both) is (are) high the output is disabled to the high–impedance state; however sequential operation of the flip–flops is not affected.
X = Don't Care.

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## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | −55°C Min | −55°C Max | 25°C Min | 25°C Typ [3.] | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage                    "0" Level <br> $V_{in} = V_{DD}$ or 0 | $V_{OL}$ | 5.0 <br> 10 <br> 15 | — <br> — <br> — | 0.05 <br> 0.05 <br> 0.05 | — <br> — <br> — | 0 <br> 0 <br> 0 | 0.05 <br> 0.05 <br> 0.05 | — <br> — <br> — | 0.05 <br> 0.05 <br> 0.05 | Vdc |
| "1" Level <br> $V_{in} = 0$ or $V_{DD}$ | $V_{OH}$ | 5.0 <br> 10 <br> 15 | 4.95 <br> 9.95 <br> 14.95 | — <br> — <br> — | 4.95 <br> 9.95 <br> 14.95 | 5.0 <br> 10 <br> 15 | — <br> — <br> — | 4.95 <br> 9.95 <br> 14.95 | — <br> — <br> — | Vdc |
| Input Voltage                     "0" Level <br> ($V_O = 4.5$ or 0.5 Vdc) <br> ($V_O = 9.0$ or 1.0 Vdc) <br> ($V_O = 13.5$ or 1.5 Vdc) | $V_{IL}$ | <br> 5.0 <br> 10 <br> 15 | <br> — <br> — <br> — | <br> 1.5 <br> 3.0 <br> 4.0 | <br> — <br> — <br> — | <br> 2.25 <br> 4.50 <br> 6.75 | <br> 1.5 <br> 3.0 <br> 4.0 | <br> — <br> — <br> — | <br> 1.5 <br> 3.0 <br> 4.0 | Vdc |
| "1" Level <br> ($V_O = 0.5$ or 4.5 Vdc) <br> ($V_O = 1.0$ or 9.0 Vdc) <br> ($V_O = 1.5$ or 13.5 Vdc) | $V_{IH}$ | <br> 5.0 <br> 10 <br> 15 | <br> 3.5 <br> 7.0 <br> 11 | <br> — <br> — <br> — | <br> 3.5 <br> 7.0 <br> 11 | <br> 2.75 <br> 5.50 <br> 8.25 | <br> — <br> — <br> — | <br> 3.5 <br> 7.0 <br> 11 | <br> — <br> — <br> — | Vdc |
| Output Drive Current <br> ($V_{OH} = 2.5$ Vdc)       Source <br> ($V_{OH} = 4.6$ Vdc) <br> ($V_{OH} = 9.5$ Vdc) <br> ($V_{OH} = 13.5$ Vdc) | $I_{OH}$ | <br> 5.0 <br> 5.0 <br> 10 <br> 15 | <br> −3.0 <br> −0.64 <br> −1.6 <br> −4.2 | <br> — <br> — <br> — <br> — | <br> −2.4 <br> −0.51 <br> −1.3 <br> −3.4 | <br> −4.2 <br> −0.88 <br> −2.25 <br> −8.8 | <br> — <br> — <br> — <br> — | <br> −1.7 <br> −0.36 <br> −0.9 <br> −2.4 | <br> — <br> — <br> — <br> — | mAdc |
| ($V_{OL} = 0.4$ Vdc)       Sink <br> ($V_{OL} = 0.5$ Vdc) <br> ($V_{OL} = 1.5$ Vdc) | $I_{OL}$ | 5.0 <br> 10 <br> 15 | 0.64 <br> 1.6 <br> 4.2 | — <br> — <br> — | 0.51 <br> 1.3 <br> 3.4 | 0.88 <br> 2.25 <br> 8.8 | — <br> — <br> — | 0.36 <br> 0.9 <br> 2.4 | — <br> — <br> — | mAdc |
| Input Current | $I_{in}$ | 15 | — | ±0.1 | — | ±0.00001 | ±0.1 | — | ±1.0 | µAdc |
| Input Capacitance <br> ($V_{in} = 0$) | $C_{in}$ | — | — | — | — | 5.0 | 7.5 | — | — | pF |
| Quiescent Current <br> (Per Package) | $I_{DD}$ | 5.0 <br> 10 <br> 15 | — <br> — <br> — | 5.0 <br> 10 <br> 20 | — <br> — <br> — | 0.005 <br> 0.010 <br> 0.015 | 5.0 <br> 10 <br> 20 | — <br> — <br> — | 150 <br> 300 <br> 600 | µAdc |
| Total Supply Current [4.] [5.] <br> (Dynamic plus Quiescent, <br> Per Package) <br> ($C_L = 50$ pF on all outputs, all <br> buffers switching) | $I_T$ | 5.0 <br> 10 <br> 15 | $I_T = (0.75\ \mu A/kHz)\ f + I_{DD}$ <br> $I_T = (1.50\ \mu A/kHz)\ f + I_{DD}$ <br> $I_T = (2.25\ \mu A/kHz)\ f + I_{DD}$ | | | | | | | µAdc |
| Three−State Leakage Current | $I_{TL}$ | 15 | — | ±0.1 | — | ±0.0001 | ±0.1 | — | ±3.0 | µAdc |

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L − 50)\ Vfk$$

where: $I_T$ is in µA (per package), $C_L$ in pF, $V = (V_{DD} − V_{SS})$ in volts, f in kHz is input frequency, and k = 0.002.

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## SWITCHING CHARACTERISTICS [6.] ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ [7.] | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time<br>$t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns<br>$t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns<br>$t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 9.5 ns | $t_{TLH}$, $t_{THL}$ | 5.0<br>10<br>15 | —<br>—<br>— | 100<br>50<br>40 | 200<br>100<br>80 | ns |
| Propagation Delay Time<br>Clock to Q<br>$t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 215 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 92 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 65 ns | $t_{PLH}$, $t_{PHL}$ | 5.0<br>10<br>15 | —<br>—<br>— | 300<br>125<br>90 | 600<br>250<br>180 | ns |
| Reset to Q<br>$t_{PLH}$, $t_{PHL}$ = (1.7 ns/pF) $C_L$ + 215 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.66 ns/pF) $C_L$ + 92 ns<br>$t_{PLH}$, $t_{PHL}$ = (0.5 ns/pF) $C_L$ + 65 ns | | 5.0<br>10<br>15 | —<br>—<br>— | 300<br>125<br>90 | 600<br>250<br>180 | |
| 3–State Propagation Delay, Output "1" or "0"<br>to High Impedance | $t_{PHZ}$, $t_{PLZ}$ | 5.0<br>10<br>15 | —<br>—<br>— | 150<br>60<br>45 | 300<br>120<br>90 | ns |
| 3–State Propagation Delay, High Impedance<br>to "1" or "0" Level | $t_{PZH}$, $t_{PZL}$ | 5.0<br>10<br>15 | —<br>—<br>— | 200<br>80<br>60 | 400<br>160<br>120 | ns |
| Clock Pulse Width | $t_{WH}$ | 5.0<br>10<br>15 | 260<br>110<br>80 | 130<br>55<br>40 | —<br>—<br>— | ns |
| Reset Pulse Width | $t_{WH}$ | 5.0<br>10<br>15 | 370<br>150<br>110 | 185<br>75<br>55 | —<br>—<br>— | ns |
| Data Setup Time | $t_{su}$ | 5.0<br>10<br>15 | 30<br>10<br>4 | 15<br>5<br>2 | —<br>—<br>— | ns |
| Data Hold Time | $t_h$ | 5.0<br>10<br>15 | 130<br>60<br>50 | 65<br>30<br>25 | —<br>—<br>— | ns |
| Data Disable Setup Time | $t_{su}$ | 5.0<br>10<br>15 | 220<br>80<br>50 | 110<br>40<br>25 | —<br>—<br>— | ns |
| Clock Pulse Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0<br>10<br>15 | —<br>—<br>— | —<br>—<br>— | 15<br>5<br>4 | μs |
| Clock Pulse Frequency | $f_{cl}$ | 5.0<br>10<br>15 | —<br>—<br>— | 3.6<br>9.0<br>12 | 1.8<br>4.5<br>6.0 | MHz |

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
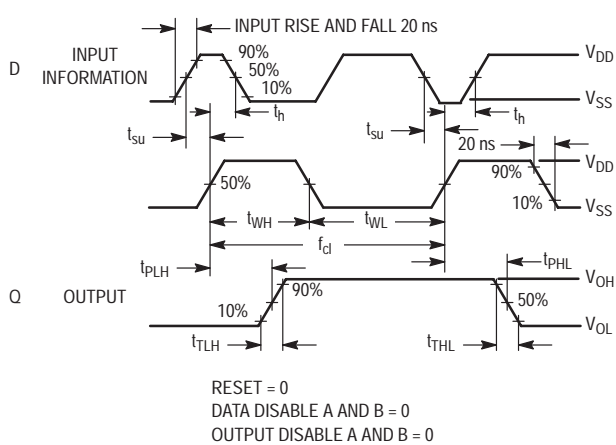
# MC14076B



RESET = 0
DATA DISABLE A AND B = 0
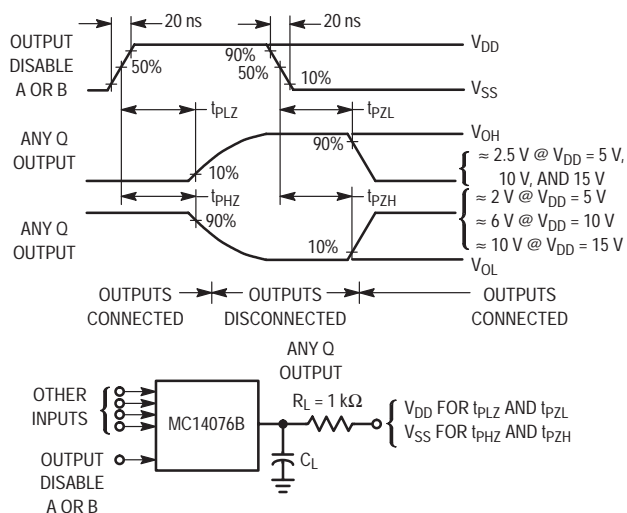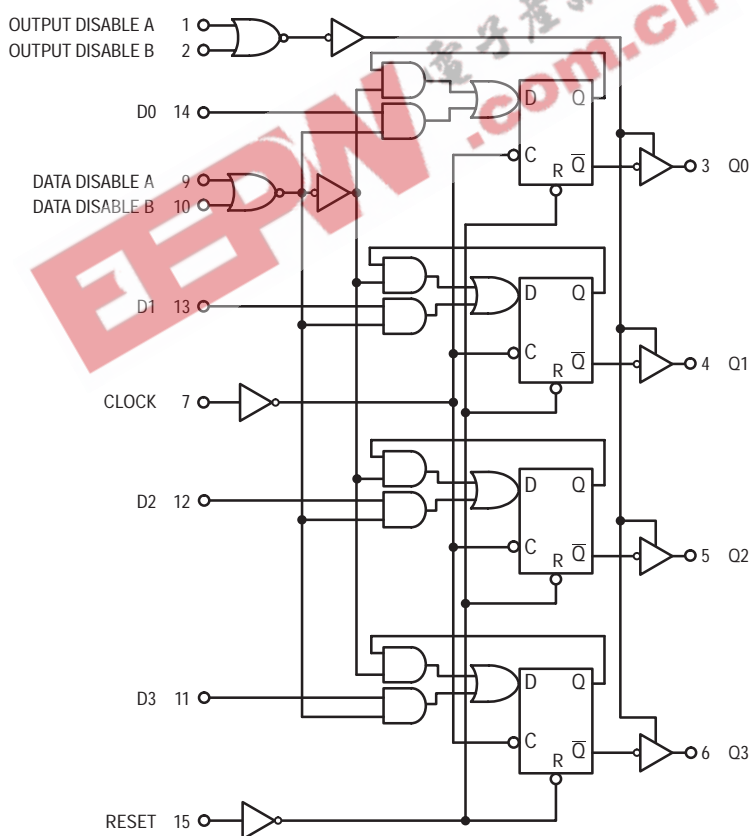OUTPUT DISABLE A AND B = 0

**Figure 1. Timing Diagram**



**Figure 2. Three–State Propagation Delay
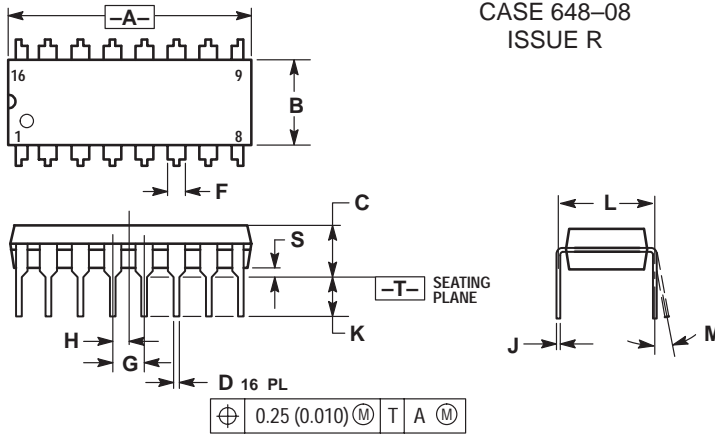Waveshape and Circuit**

## EQUIVALENT
## FUNCTIONAL BLOCK DIAGRAM

# MC14076B

## PACKAGE DIMENSIONS

**PDIP−16**
**P SUFFIX**
PLASTIC DIP PACKAGE
CASE 648−08
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|--------|
|     | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.70 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

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## PACKAGE DIMENSIONS

**SOIC–16**
**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
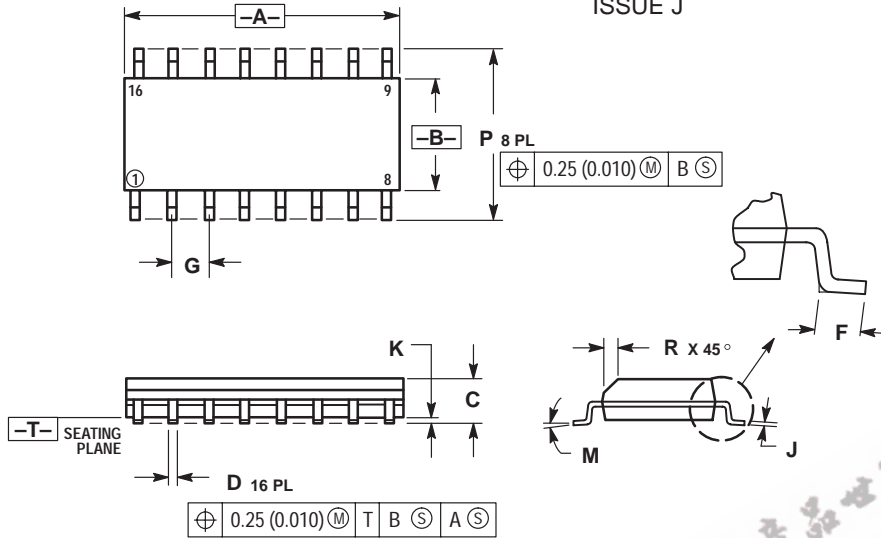
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-----|-----|-----|-----|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0 ° | 7 ° | 0 ° | 7 ° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

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