

DATA SHEET

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74F583

4-bit BCD adder

Product specification

1989 Apr 06

IC15 Data Handbook

4-bit BCD adder

74F583

FEATURES

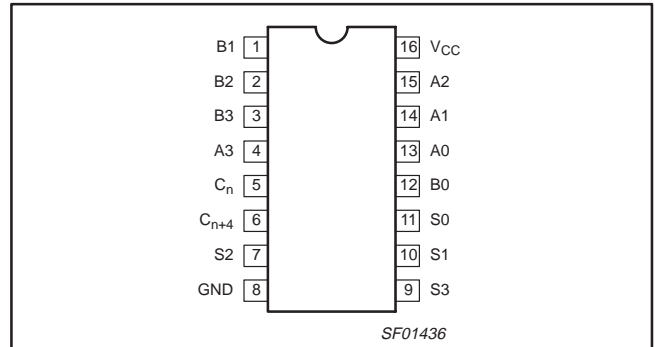
- Adds two decimal numbers
- Full internal look-ahead
- Fast ripple carry for economical expansion
- Sum output delay 19.5 ns max.
- Ripple carry delay 8.5 ns max.
- Input to ripple delay 13.0 ns max.
- Supply current 60 mA max.

DESCRIPTION

The 74F583 4-bit coded (BCD) full adder performs the addition of two decimal numbers (A0–A3, B0–B3). The look-ahead generates BCD carry terms internally, allowing the 74F583 to then do BCD addition correctly. For BCD numbers 0 through 9 at A and B inputs, the BCD sum forms at the output.

In addition of two BCD numbers totalling a number greater than 9, a valid BCD number and carry will result. For input values larger than 9, the number is converted from binary to BCD. Binary to BCD conversion occurs by grounding one set of inputs, An or Bn, and applying a 4-bit binary number to the other set of inputs. If the input is between 0 and 9, a BCD number occurs at the output. If the binary input falls between 10 and 15, a carry term is generated. Both the carry term and the sum are the BCD equivalent of the binary input. Converting binary numbers greater than 16 may be achieved by cascading 74F583s.

PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F583	9.0 ns	45 mA

ORDERING INFORMATION

PACKAGE	COMMERCIAL RANGE V _{CC} = 5 V ±10% T _{amb} = 0°C to +70°C	DRAWING NUMBER
16-pin plastic DIP	N74F583N	SOT38-4
16-pin plastic SO	N74F583D	SOT109-1

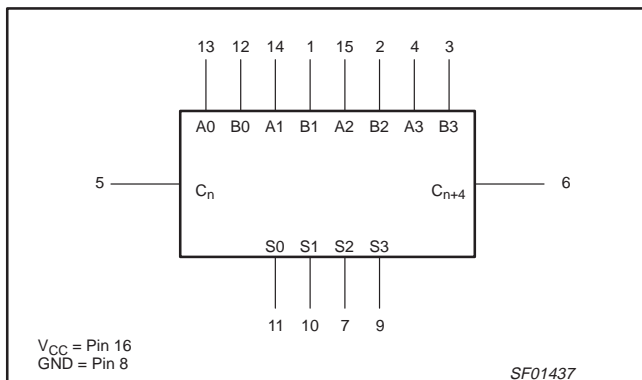
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH / LOW	LOAD VALUE HIGH / LOW
A0–A3	A operand inputs	1.0 / 2.0	20 μA / 1.2 mA
B0–B3	B operand inputs	1.0 / 2.0	20 μA / 1.2 mA
C _n	Carry input	1.0 / 1.0	20 μA / 0.6 mA
C _{n+4}	Carry output	50 / 33	1.0 mA / 20 mA
S0–S3	Sum outputs	50 / 33	1.0 mA / 20 mA

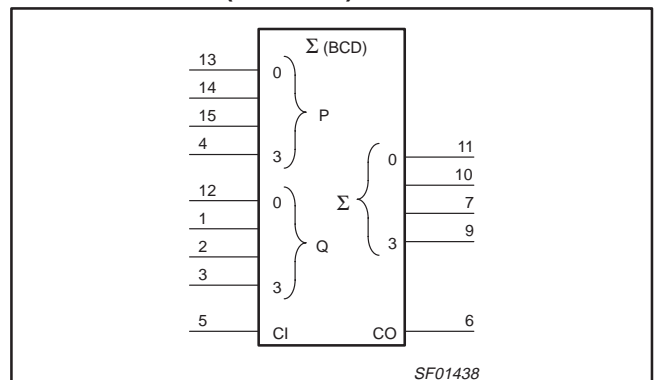
NOTE:

One (1.0) FAST Unit Load is defined as 20 μA in the High state and 0.6 mA in the Low state.

LOGIC SYMBOL



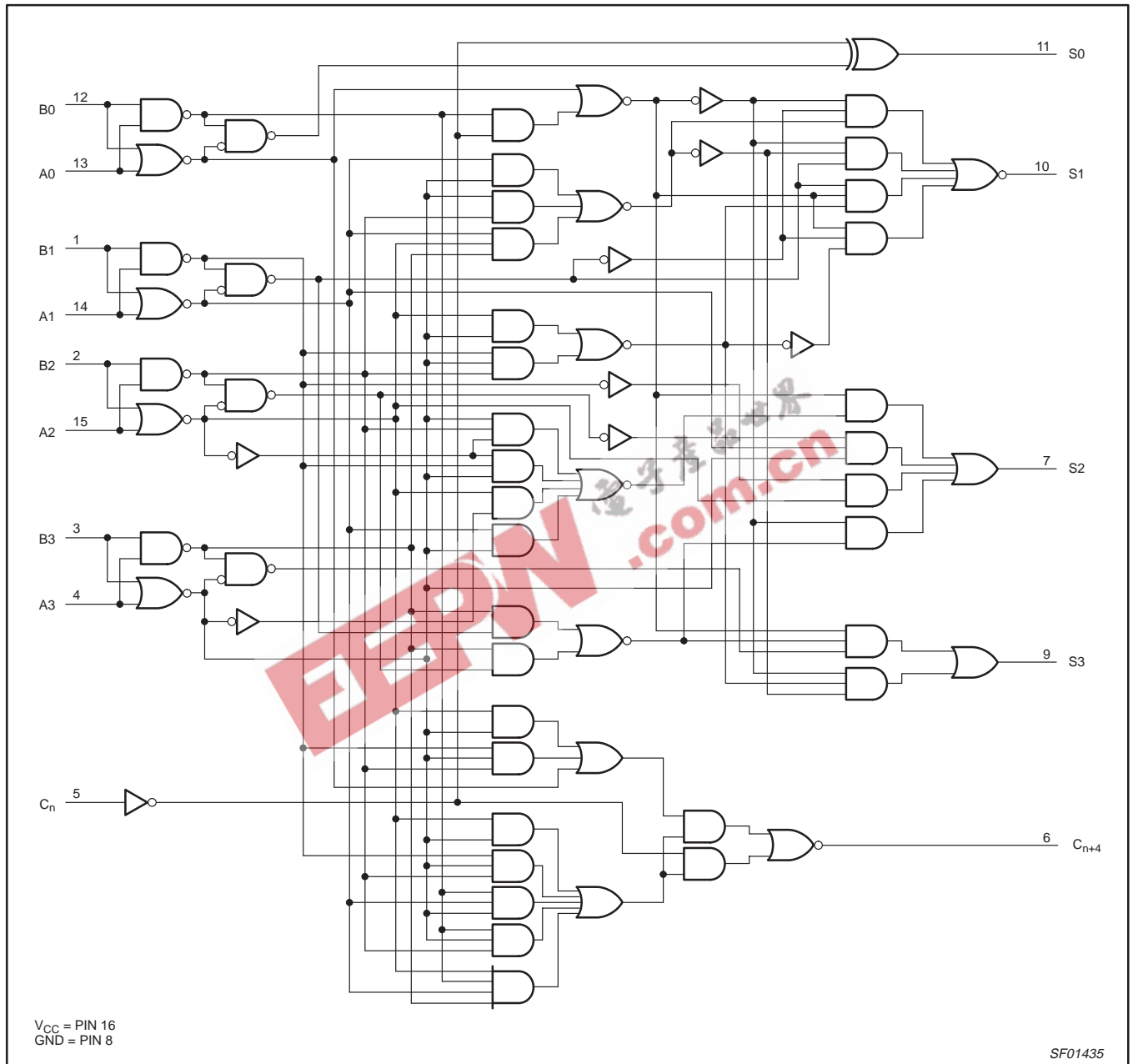
LOGIC SYMBOL (IEEE/IEC)



4-bit BCD adder

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LOGIC DIAGRAM



4-bit BCD adder

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ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted, these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to $+V_{CC}$	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS ¹	LIMITS			UNIT	
			MIN	TYP ²	MAX		
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}, I_{OH} = \text{MAX}$	$\pm 10\% V_{CC}$	2.5		V	
			$\pm 5\% V_{CC}$	2.7	3.4	V	
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}$ $V_{IH} = \text{MIN}, I_{OL} = \text{MAX}$	$\pm 10\% V_{CC}$		0.30	0.50	V
			$\pm 5\% V_{CC}$		0.30	0.50	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V	
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0 \text{ V}$			100	μA	
I_{IH}	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20	μA	
I_{IL}	Low-level input current	C_n only			-0.6	mA	
		A_n and B_n			-1.2	mA	
I_{OS}	Short circuit output current ³	$V_{CC} = \text{MAX}$	-60		-150	mA	
I_{CC}	Supply current (total)	$V_{CC} = \text{MAX}$		45	60	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5 \text{ V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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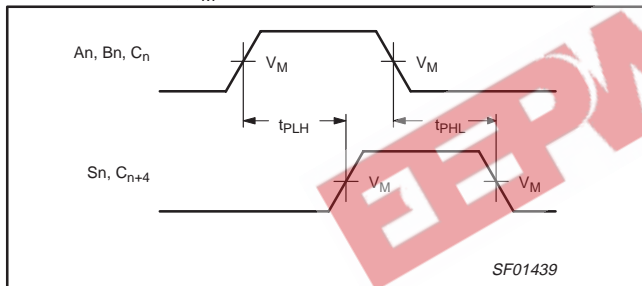
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AC ELECTRICAL CHARACTERISTICS

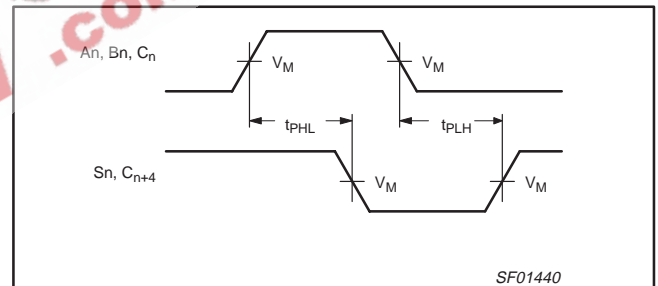
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = 5 V C _L = 50 pF; R _L = 500 Ω			T _{amb} = 0°C to +70°C V _{CC} = 5 V ±10% C _L = 50 pF; R _L = 500 Ω		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay An or Bn to Sn	Waveform 1	5.0 5.0	13.0 10.5	17.0 14.0	5.0 5.0	18.0 15.0	ns
t _{PLH} t _{PHL}	Propagation delay An or Bn to Sn (INV)	Waveform 2	6.0 4.0	11.0 8.0	18.0 12.0	5.0 4.0	19.5 12.5	ns
t _{PLH} t _{PHL}	Propagation delay C _n to C _{n+4}	Waveform 1, 2	3.5 2.5	5.0 4.0	8.0 7.0	3.0 2.0	8.5 7.0	ns
t _{PLH} t _{PHL}	Propagation delay An or Bn to C _{n+4}	Waveform 1, 2	5.0 5.0	8.0 7.5	11.5 10.5	4.5 4.5	13.0 11.5	ns
t _{PLH} t _{PHL}	Propagation delay C _n to Sn	Waveform 1	4.0 3.5	12.0 8.0	15.5 12.5	3.5 3.0	17.0 13.5	ns
t _{PLH} t _{PHL}	Propagation delay C _n to Sn (INV)	Waveform 2	6.0 3.5	9.5 8.0	13.0 11.5	5.0 3.0	14.5 12.0	ns

AC WAVEFORMS

For all waveforms, V_M = 1.5 V.



Waveform 1. Propagation delay for non-inverting outputs



Waveform 2. Propagation delay for inverting outputs

TEST CIRCUIT AND WAVEFORMS

Test Circuit for Totem-Pole Outputs

Input Pulse Definition

DEFINITIONS:

- R_L = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C_L = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	V _M	rep. rate	t _w	t _{TLH}	t _{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

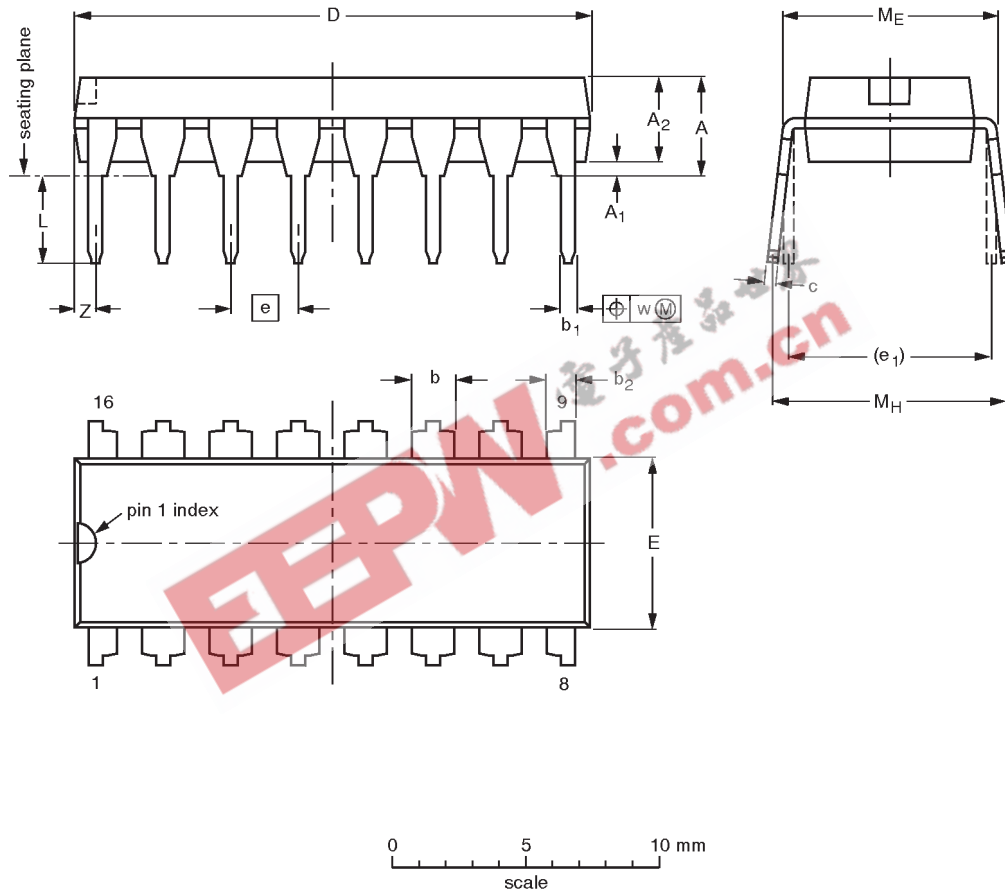
SF00006

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

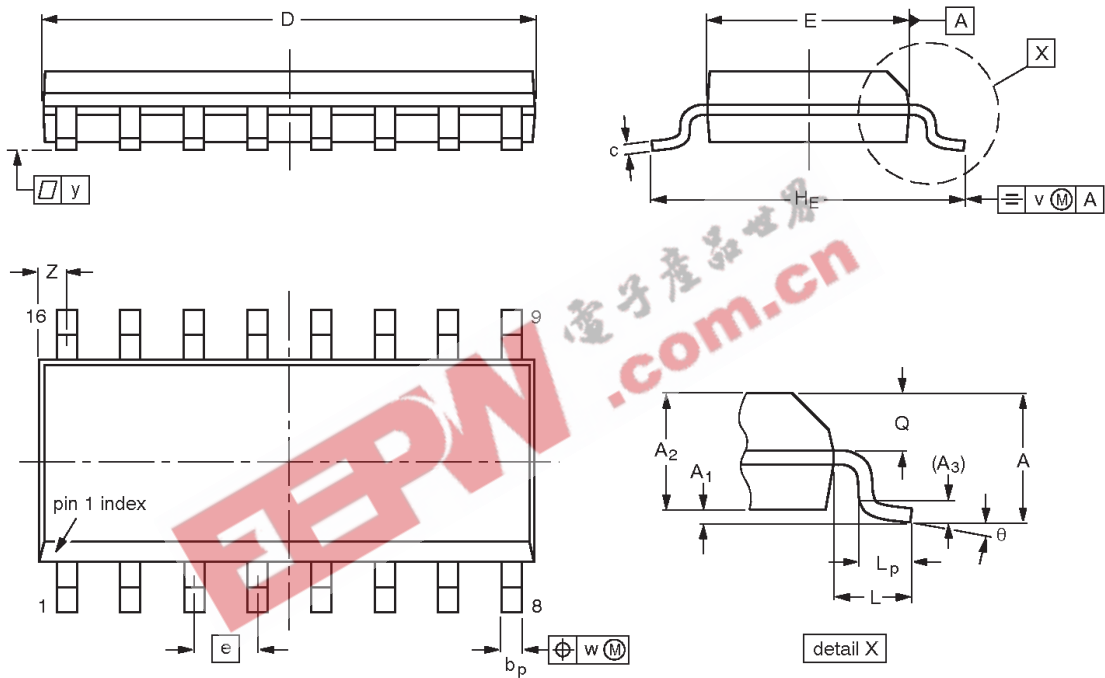
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				97-05-22 99-12-27

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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