

# DATA SHEET

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**74F393**

Dual 4-bit binary ripple counter

Product specification

1988 Nov 01

IC15 Data Handbook

# Dual 4-bit binary ripple counter

# 74F393

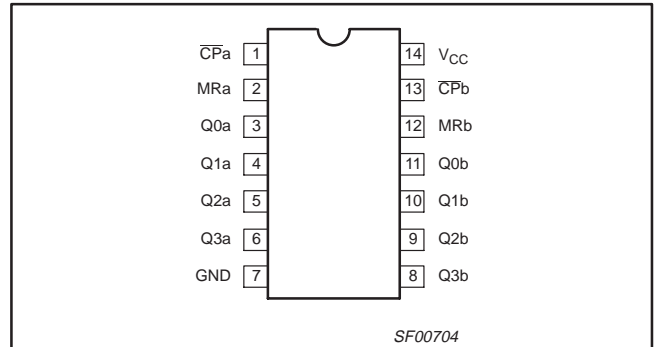
## FEATURES

- Two 4-bit binary counters
- Two Master Resets to clear each 4-bit counter individually

## DESCRIPTION

The 74F393 is a Dual Ripple Counter with separate Clock ( $\overline{CP}_n$ ) and Master Reset (MR) inputs to each counter. The two counters are identified by the "a" and "b" suffixes in the pin configuration. The operation of each half of the 74F393 is the same. The counters are triggered by a High-to-Low transition of the Clock ( $\overline{CP}_a$  and  $\overline{CP}_b$ ) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding. The Master Resets ( $MR_a$  and  $MR_b$ ) are active High asynchronous inputs; one for each 4-bit counter. A High level in the MR input overrides the Clock and sets the outputs Low.

## PIN CONFIGURATION



TYPE	TYPICAL $f_{MAX}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F393	125MHz	40mA

## ORDERING INFORMATION

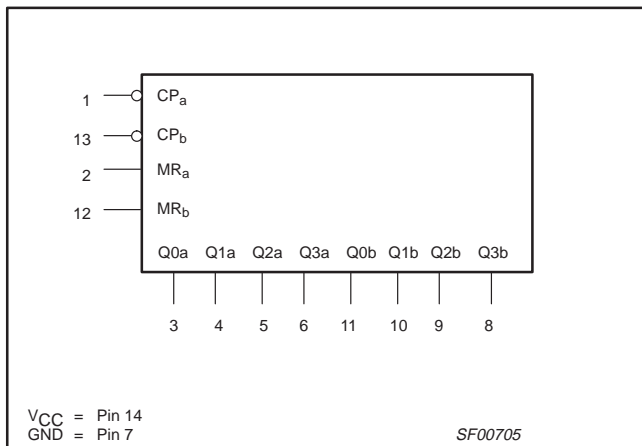
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^\circ C$ to $+70^\circ C$	PKG DWG #
14-pin plastic DIP	N74F393N	SOT27-1
14-pin plastic SO	N74F393D	SOT108-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

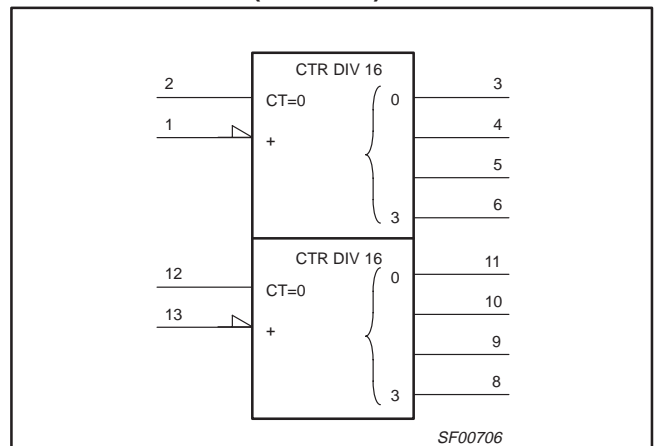
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CP}_a, \overline{CP}_b$	Clock inputs	1.0/1.0	20 $\mu$ A/0.6mA
$MR_a, MR_b$	Master Reset inputs	1.0/1.0	20 $\mu$ A/0.6mA
$Q_{na} - Q_{nb}$	Data outputs	50/33.3	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## LOGIC SYMBOL



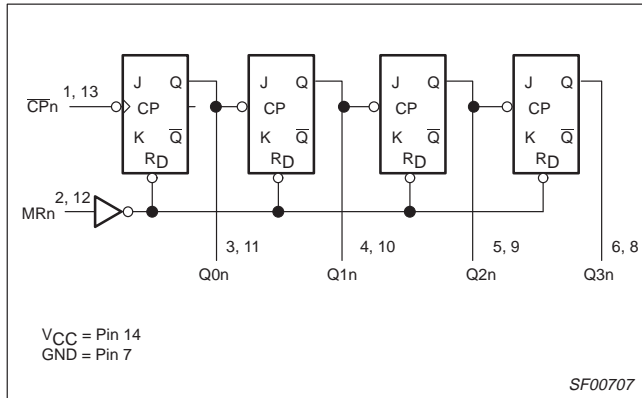
## IEC/IEEE SYMBOL (IEEE/IEC)



# Dual 4-bit binary ripple counter

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## LOGIC DIAGRAM



## FUNCTION TABLE

COUNT	OUTPUTS			
	Q <sub>0n</sub>	Q <sub>1n</sub>	Q <sub>2n</sub>	Q <sub>3n</sub>
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = High voltage level transition  
L = Low voltage level

## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	40	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature range	-65 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT	
			MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>	2.5		V	
		V <sub>IH</sub> = MIN, I <sub>OH</sub> = MAX	±5%V <sub>CC</sub>	2.7	3.4		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX	±10%V <sub>CC</sub>		0.30	V	
		V <sub>IH</sub> = MIN, I <sub>OL</sub> = MAX	±5%V <sub>CC</sub>		0.30		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>		-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V			100	μA	
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V			20	μA	
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V			-0.6	mA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX		-60	-150	mA	
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX		25	36	mA
		I <sub>CCL</sub>			42	58	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum clock frequency	Waveform 1	100	130		100		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>n</sub> to Q0a or Q0b	Waveform 1	3.5 5.0	5.5 7.0	8.0 10.0	3.5 5.0	9.0 10.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>n</sub> to Q1a, Q1b	Waveform 1	5.0 7.5	7.0 9.5	10.0 12.0	4.5 7.0	13.0 13.0	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>n</sub> to Q2a, Q2b	Waveform 1	8.0 9.5	10.0 11.5	13.0 14.5	7.0 9.0	15.0 15.5	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP <sub>n</sub> to Q3a, Q3b	Waveform 1	10.5 12.0	12.5 14.0	15.5 16.5	10.0 11.5	17.0 17.5	ns
t <sub>PHL</sub>	Propagation delay MR to Qna, Qnb	Waveform 2	4.0	6.0	9.0	4.0	9.0	ns

# Dual 4-bit binary ripple counter

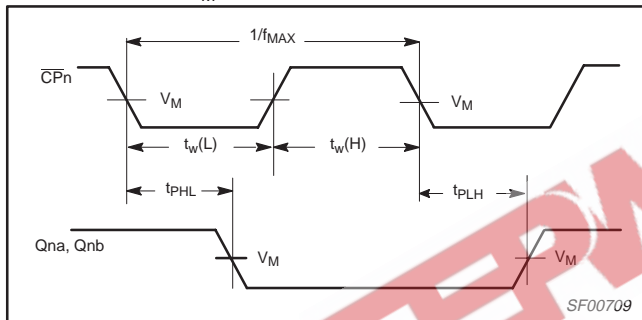
74F393

## AC SETUP REQUIREMENTS

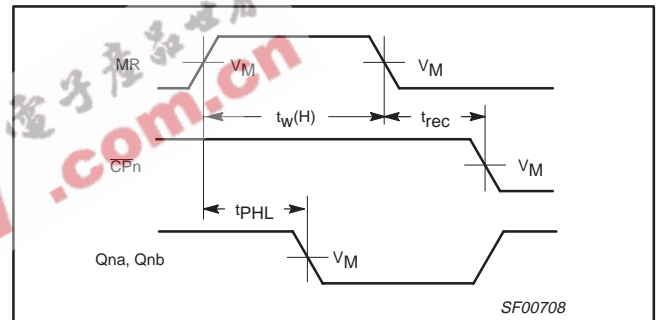
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>W(H)</sub> t <sub>W(L)</sub>	CPn Pulse width High or Low	Waveform 1	4.5 3.5			5.0 4.0		ns
t <sub>W(H)</sub>	MR Pulse width High	Waveform 2	3.5			4.5		ns
t <sub>REC</sub>	Recovery time MR to CPn	Waveform 2	2.5			3.0		ns

## AC WAVEFORMS

For all waveforms, V<sub>M</sub> = 1.5V.



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Clock Recovery Time

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for Totem-Pole Outputs**

**DEFINITIONS:**

- R<sub>L</sub> = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

**Input Pulse Definition**

family	INPUT PULSE REQUIREMENTS					
	amplitude	V <sub>M</sub>	rep. rate	t <sub>w</sub>	t <sub>TLH</sub>	t <sub>THL</sub>
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

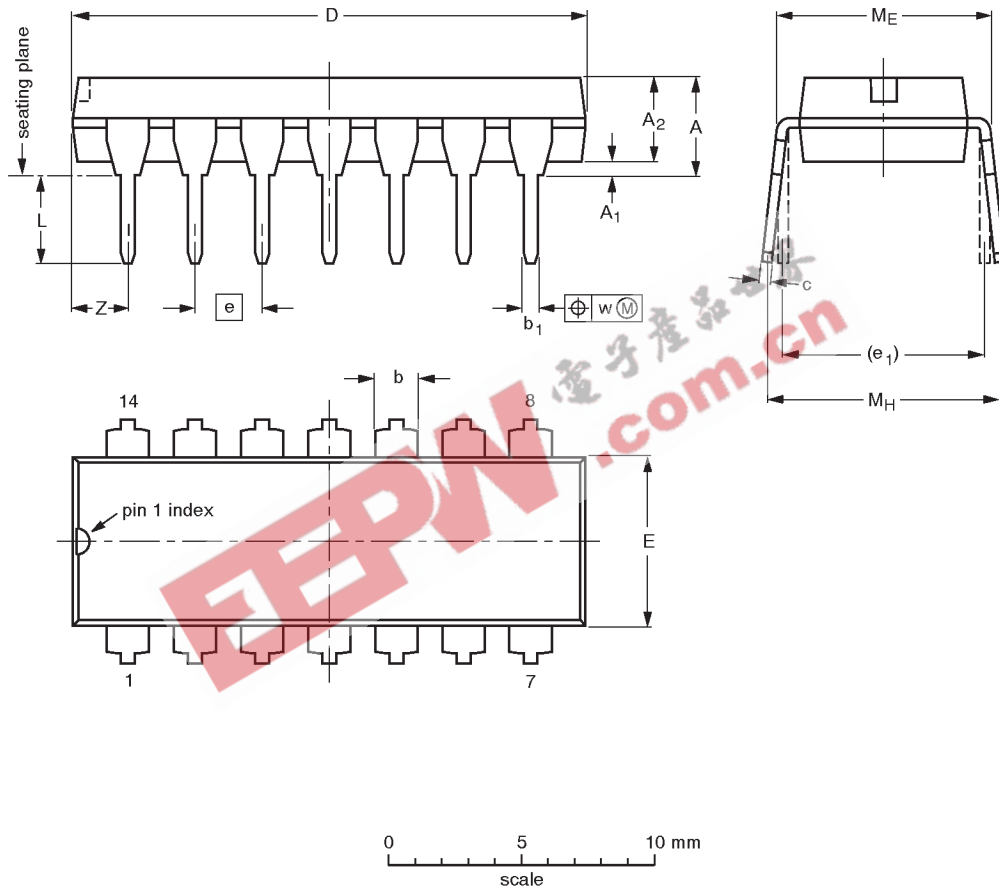
SF00006

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

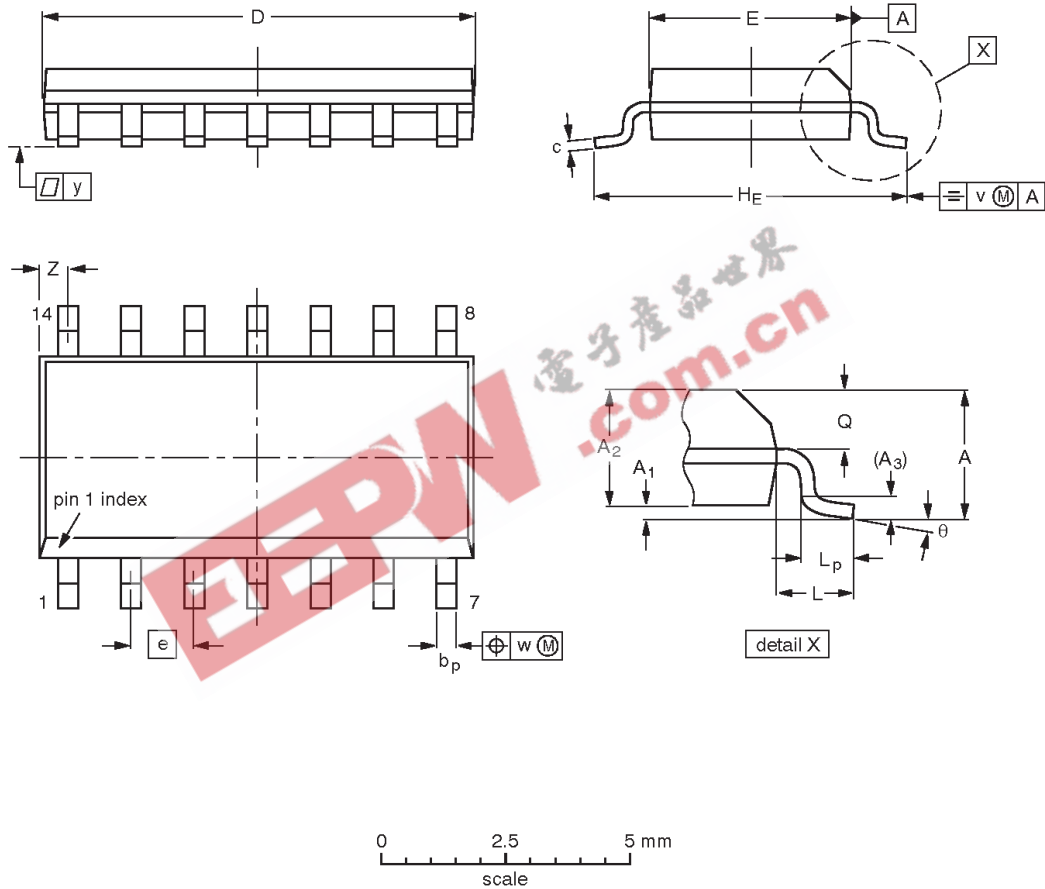
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-20 97-05-22

## Dual 4-bit binary ripple counter

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code

Date of release: 10-98

Document order number:

9397-750-05125

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