P4C198/P4C198L, P4C198A/P4C198AL
ULTRA HIGH SPEED 16K x 4
STATIC CMOS RAMS

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15/20/25 ns (Commercial)**
  - **– 12/15/20/25/35 ns (Industrial)**
  - **– 15/20/25/35/45 ns (Military)**
- **Low Power Operation (Commercial/Military)**
- **5V ± 10% Power Supply**
- **Data Retention, 10 µA Typical Current from 2.0V P4C198L/198AL (Military)**
- **Output Enable & Chip Enable Control Functions**
  - **– Single Chip Enable P4C198**
  - **– Dual Chip Enable P4C198A**
- **Common Inputs and Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 24-Pin 300 mil DIP**
  - **– 24-Pin 300 mil SOJ**
  - **– 28-Pin 350 x 550 mil LCC**

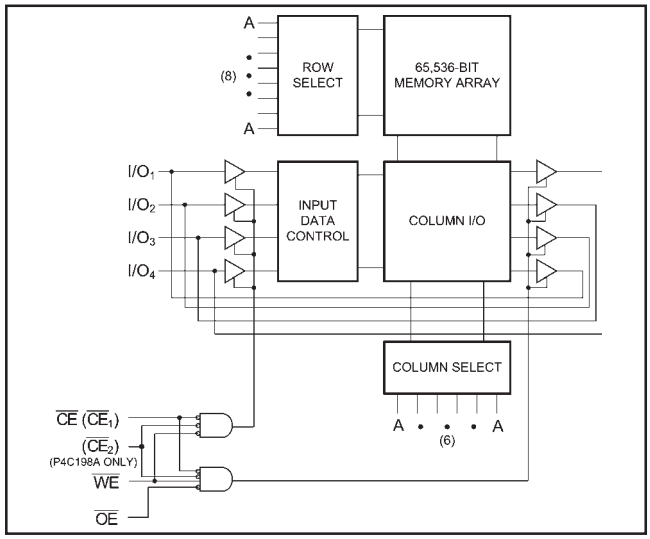
DESCRIPTION

The P4C198/L and P4C198A/L are 65,536-bit ultra high-speed static RAMs organized as 16K x 4. Each device features an active low Output Enable control to eliminate data bus contention. The P4C198/L also have an active low Chip Enable (the P4C198A/L have two Chip Enables, both active low) for easy system expansion. The CMOS memories require no clocks or refreshing and have equal access and cycle times. Inputs are fully TTL-compatible. The RAMs operate from a single 5V ± 10% tolerance power supply. Data integrity is maintained with supply voltages down to 2.0V. Current drain is typically 10 µA from a 2.0V supply.

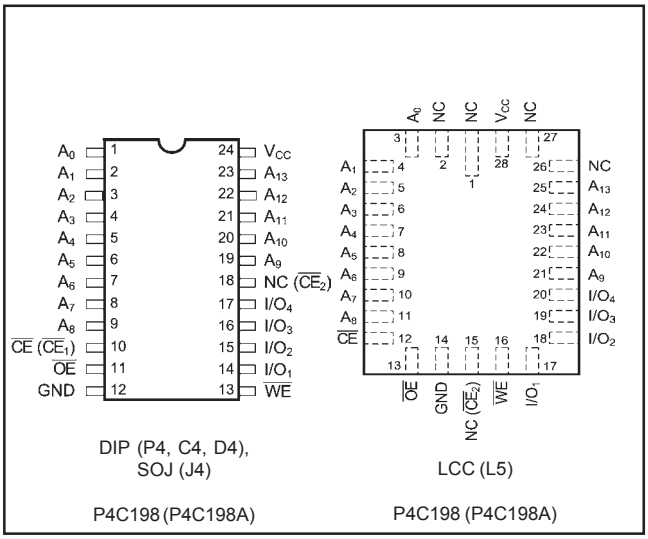
Access times as fast as 12 nanoseconds are available, permitting greatly enhanced system operating speeds. CMOS is used to reduce power consumption to a low 715 mW active, 193 mW standby.

The P4C198/L and P4C198A/L are available in 24-pin 300 mil DIP and SOJ, and 28-pin 350 x 550 mil LCC packages providing excellent board level densities.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P4, C4, D4), SOJ (J4)

P4C198 (P4C198A)

LCC (L5)

P4C198 (P4C198A)

MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade(2)	Ambient Temperature	GND	V_{CC}
Military	–55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	–40°C to +85°C	0V	5.0V ± 10%

CAPACITANCES[4]

V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage[2]

Symbol	Parameter	Test Conditions	P4C198 / 198A		P4C198L / 198AL		Unit
			Min	Max	Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC} +0.5	2.2	V_{CC} +0.5	V
V_{IL}	Input Low Voltage		–0.5[3]	0.8	–0.5[3]	0.8	V
V_{HC}	CMOS Input High Voltage		V_{CC} –0.2	V_{CC} +0.5	V_{CC} –0.2	V_{CC} +0.5	V
V_{LC}	CMOS Input Low Voltage		–0.5[3]	0.2	–0.5[3]	0.2	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA		–1.2		–1.2	V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +10 mA, V_{CC} = Min. I_{OL} = +8 mA, V_{CC} = Min.	0.5	 0.4	0.5	 0.4	V V
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.	2.4		2.4		V
I_{LI}	Input Leakage Current	V_{CC} = Max. Mil. V_{IN} = GND to V_{CC} Ind./Com'l.	–10 –5	+10 +5	–5 n/a	+5 n/a	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CE}$ = V_{IH}, Mil. V_{OUT} = GND to V_{CC} Ind./Com'l.	–10 –5	+10 +5	–5 n/a	+5 n/a	µA
I_{SB}	Standby Power Supply Current (TTL Input Levels)	$\overline{CE}_1$, $\overline{CE}_2$ ≥ V_{IH} Mil. V_{CC} = Max ., Ind./Com'l. f = Max., Outputs Open	—— ——	40 35	—— ——	40 n/a	mA
I_{SB1}	Standby Power Supply Current (CMOS Input Levels)	$\overline{CE}_1$, $\overline{CE}_2$ ≥ V_{IH} Mil. V_{CC} = Max., Ind./Com'l. f = 0, Outputs Open V_{IN} ≤ V_{LC} or V_{IN} ≥ V_{HC}	—— ——	20 15	—— ——	1.5 n/a	mA

n/a = Not Applicable

Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM ratingconditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	–10	–12	–15	–20	–25	–35	–45	Unit
I_{CC}	Dynamic Operating Current*	Commercial	180	170	160	155	150	N/A	N/A	mA
		Industrial	N/A	180	170	160	155	150	N/A	mA
		Military	N/A	N/A	170	160	155	150	145	mA

*V_{CC} = 5.5V. Tested with outputs open. f = Max. Switching inputs are 0V and 3V.

198: $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}

198A: $\overline{CE_1}$ = V_{IL}, $\overline{CE_2}$ = V_{IL}. $\overline{OE}$ = V_{IH}

DATA RETENTION CHARACTERISTICS (P4C198L/P4C198AL Military Temperature Only)

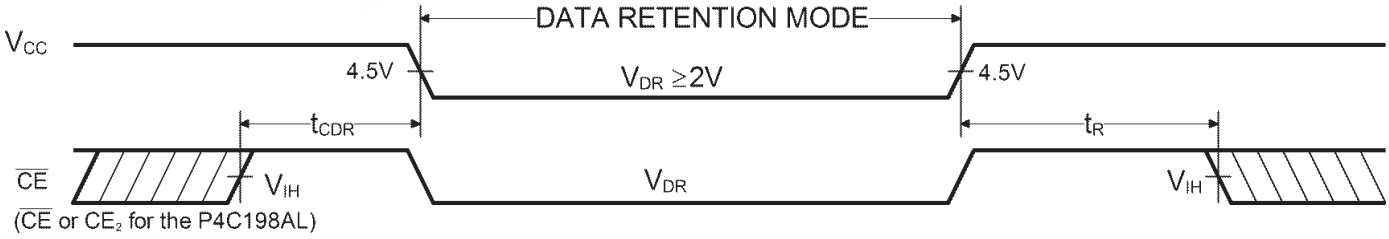
Symbol	Parameter	Test Condition	Min	Typ.* V_{CC}= 2.0V	Typ.* V_{CC}= 3.0V	Max V_{CC}= 2.0V	Max V_{CC}= 3.0V	Unit
V_{DR}	V_{CC} for Data Retention		2.0					V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$		10	15	600	900	µA
t_{CDR}	Chip Deselect to Data Retention Time		0					ns
t_R†	Operation Recovery Time		t_{RC}§					ns

*T_A = +25°C

§t_{RC} = Read Cycle Time

†This parameter is guaranteed but not tested.

DATA RETENTION WAVEFORM

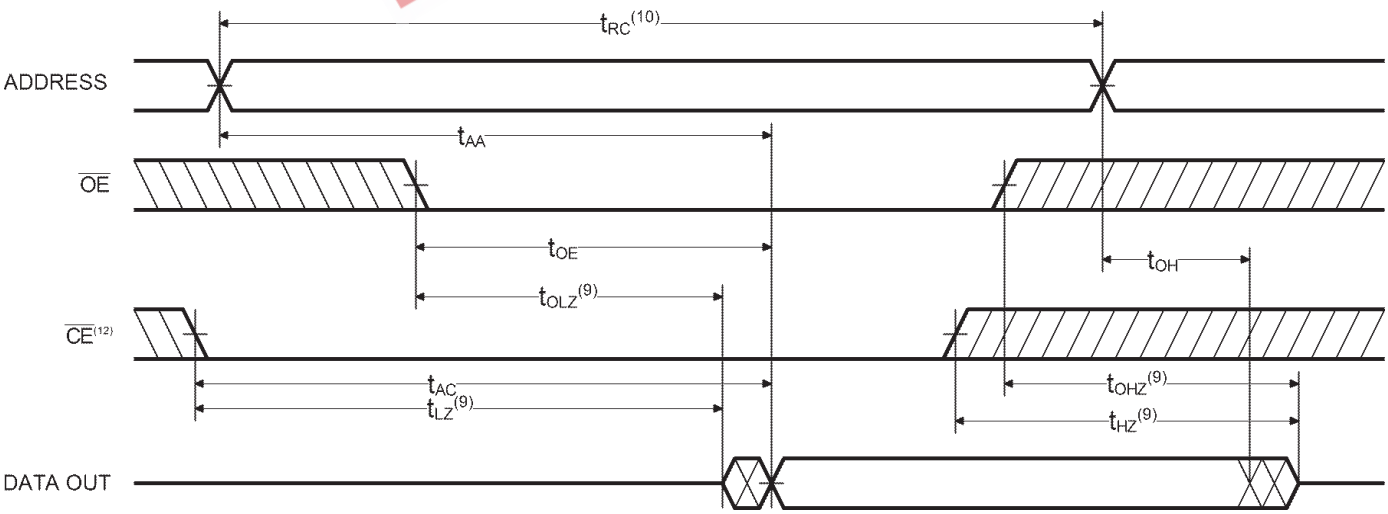


AC CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-10		-12		-15		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	10		12		15		20		25		35		45		ns
t_{AA}	Address Access Time		10		12		15		20		25		35		45	ns
t_{AC}	Chip Enable Access Time		10		12		15		20		25		35		45	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		2		2		2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		6		7		8		10		10		14		15	ns
t_{OE}	Output Enable Low to Data Valid		6		7		9		12		15		25		30	ns
t_{OLZ}	Output Enable to Output in Low Z	2		2		2		2		2		2		2		ns
t_{OHZ}	Output Disable to Output in High Z		6		7		9		9		10		14		15	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		10		12		15		20		25		35		45	ns

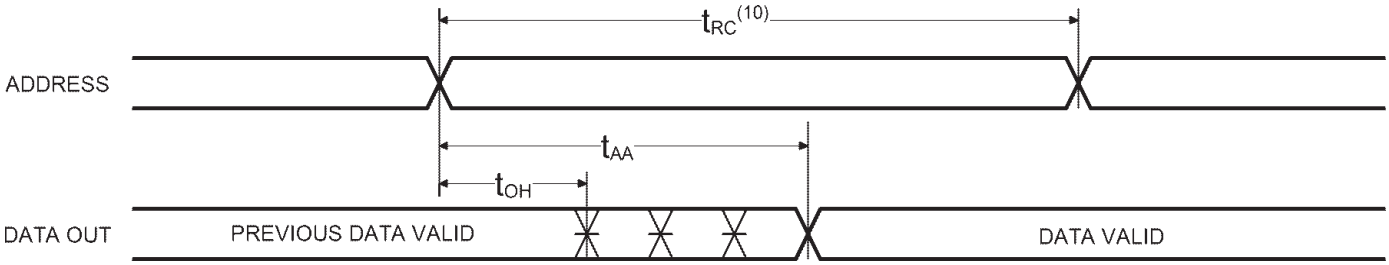
READ CYCLE NO.1 ($\overline{OE}$ controlled)[5]



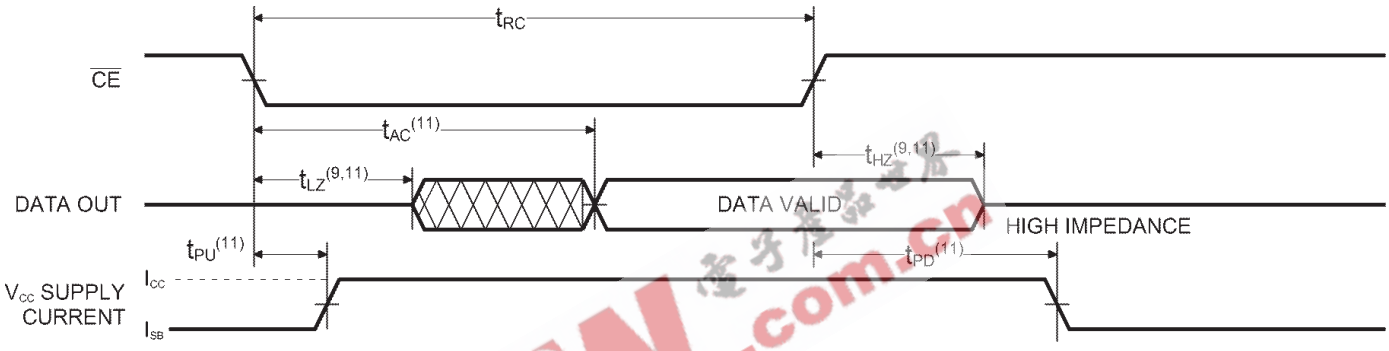
Notes:

5. $\overline{WE}$ is HIGH for READ cycle.

READ CYCLE NO. 2 (ADDRESS Controlled)[5,6]



READ CYCLE NO. 3 ($\overline{CE}$[12] Controlled)[5,7,8]



Notes:

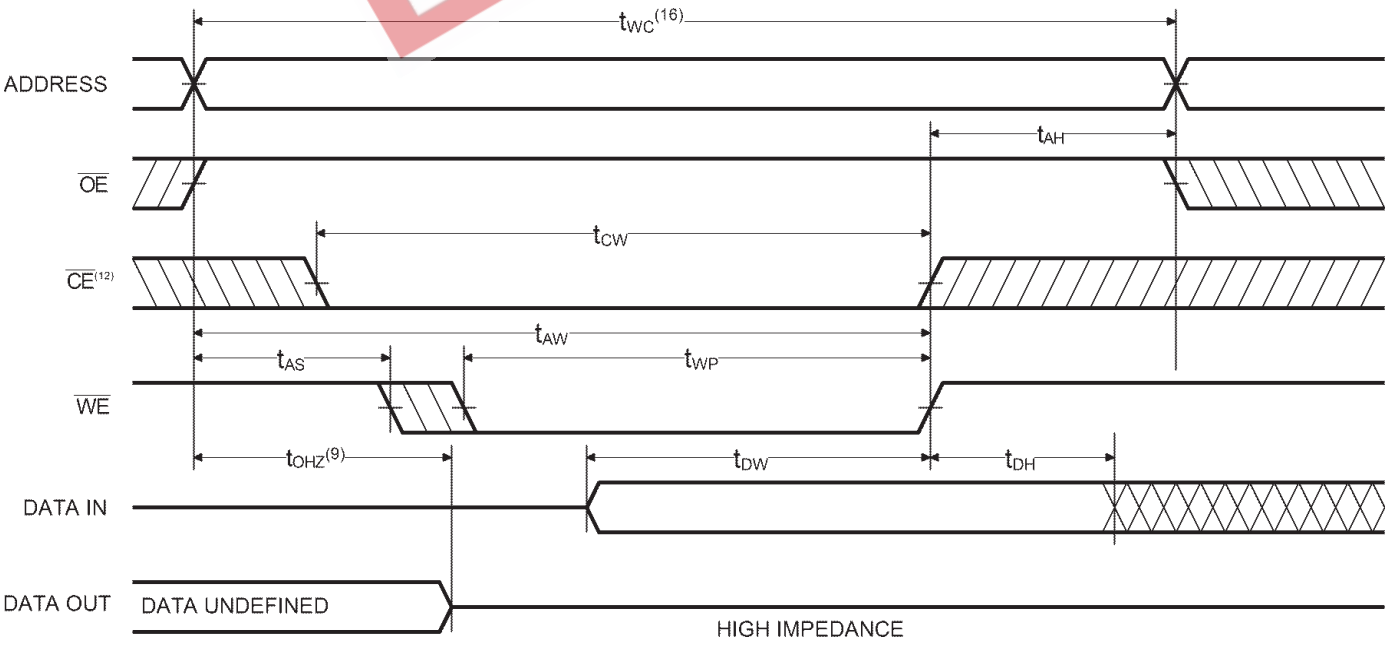
6. $\overline{CE}$ ($\overline{CE_1}$, $\overline{CE_2}$ for P4C198A/L) and $\overline{OE}$ are LOW READ cycle.
7. $\overline{OE}$ is LOW for the cycle.
8. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ ($\overline{CE_1}$ and $\overline{CE_2}$ for P4C198A/L) transition LOW.
9. Transition is measured ± 200mV from steady state voltage prior to change, with loading as specified in Figure 1.
10. Read Cycle Time is measured from the last valid address to the first transitioning address.
11. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE_1}$ or $\overline{CE_2}$ causes them (P4C198A/L).
12. $\overline{CE_1}$, $\overline{CE_2}$ for P4C198A/L.

AC CHARACTERISTICS—WRITE CYCLE

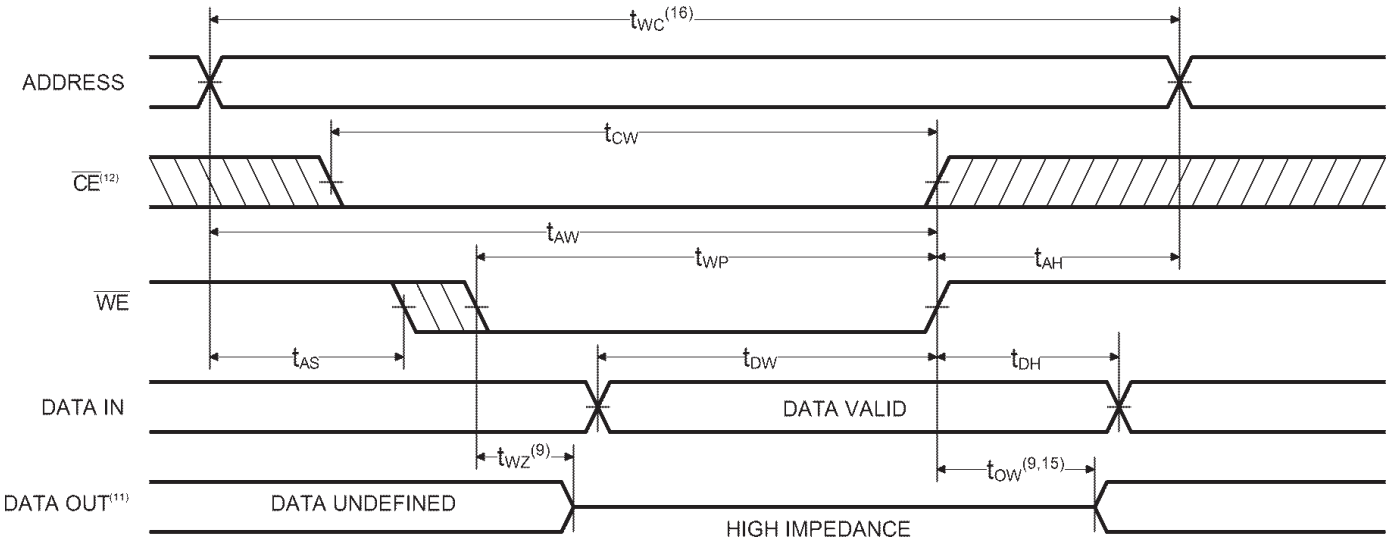
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-10		-12		-15		-20		-25		-35		-45		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		13		15		20		30		40		ns
t_{CW}	Chip Enable Time to End of Write	7		8		10		15		20		30		35		ns
t_{AW}	Address Valid to End of Write	8		8		10		15		20		25		35		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	8		9		10		12		20		25		35		ns
t_{AH}	Address Hold Time from End of Write	0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	7		6		7		10		13		15		20		ns
t_{DH}	Data Hold Time	0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		7		6		7		8		10		10		15	ns
t_{OW}	Output Active from End of Write	3		3		3		3		3		3		3		ns

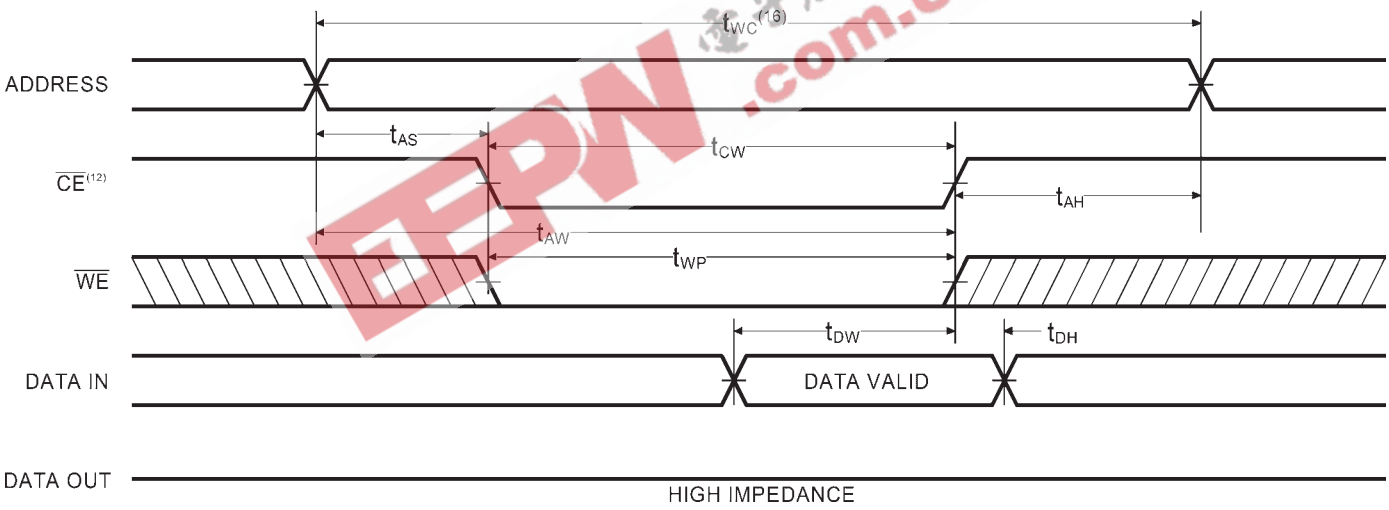
WRITE CYCLE NO. 1 (With $\overline{OE}$ high)



WRITE CYCLE NO. 2 ($\overline{WE}$ CONTROLLED)[13,14]



WRITE CYCLE NO. 3 ($\overline{CE}$[12] CONTROLLED)[13,14]



Notes:
13. $\overline{CE}$ ($\overline{CE_1}$, $\overline{CE_2}$ for P4C198A/L) and $\overline{WE}$ must be LOW for WRITE cycle.
14. $\overline{OE}$ is LOW for this WRITE cycle.
15. If $\overline{CE}$ ($\overline{CE_1}$ or $\overline{CE_2}$ for P4C198A/L) goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
16. Write Cycle Time is measured from the last valid address to the first transitioning address.

TRUTH TABLES

P4C198/L

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Mode	Output
H	X	X	Standby	High Z
L	H	H	Output Inhibit	High Z
L	H	L	READ	D_{OUT}
L	L	X	WRITE	D_{IN}

P4C198A/L

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	$\overline{OE}$	Mode	Output
H	X	X	X	Standby	High Z
X	H	X	X	Standby	High Z
L	L	H	H	Output Inhibit	High Z
L	L	H	L	READ	D_{OUT}
L	L	L	X	WRITE	D_{IN}

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

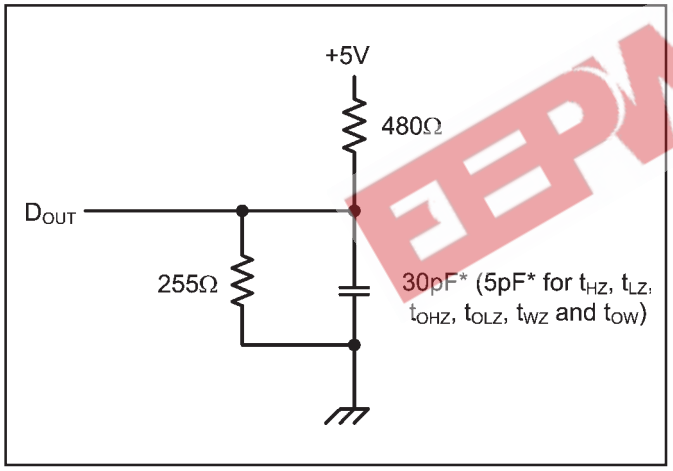


Figure 1. Output Load

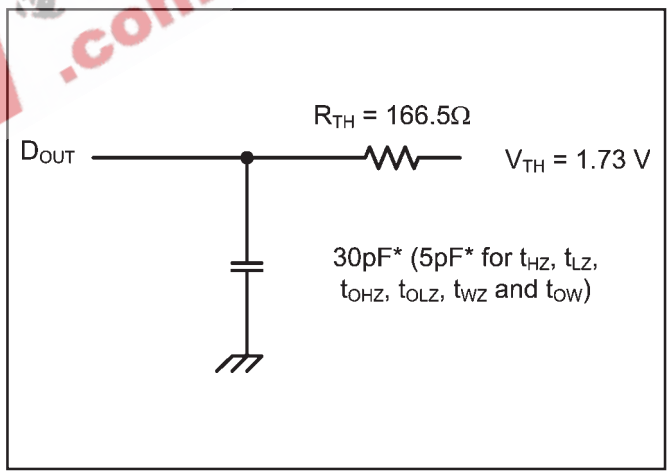
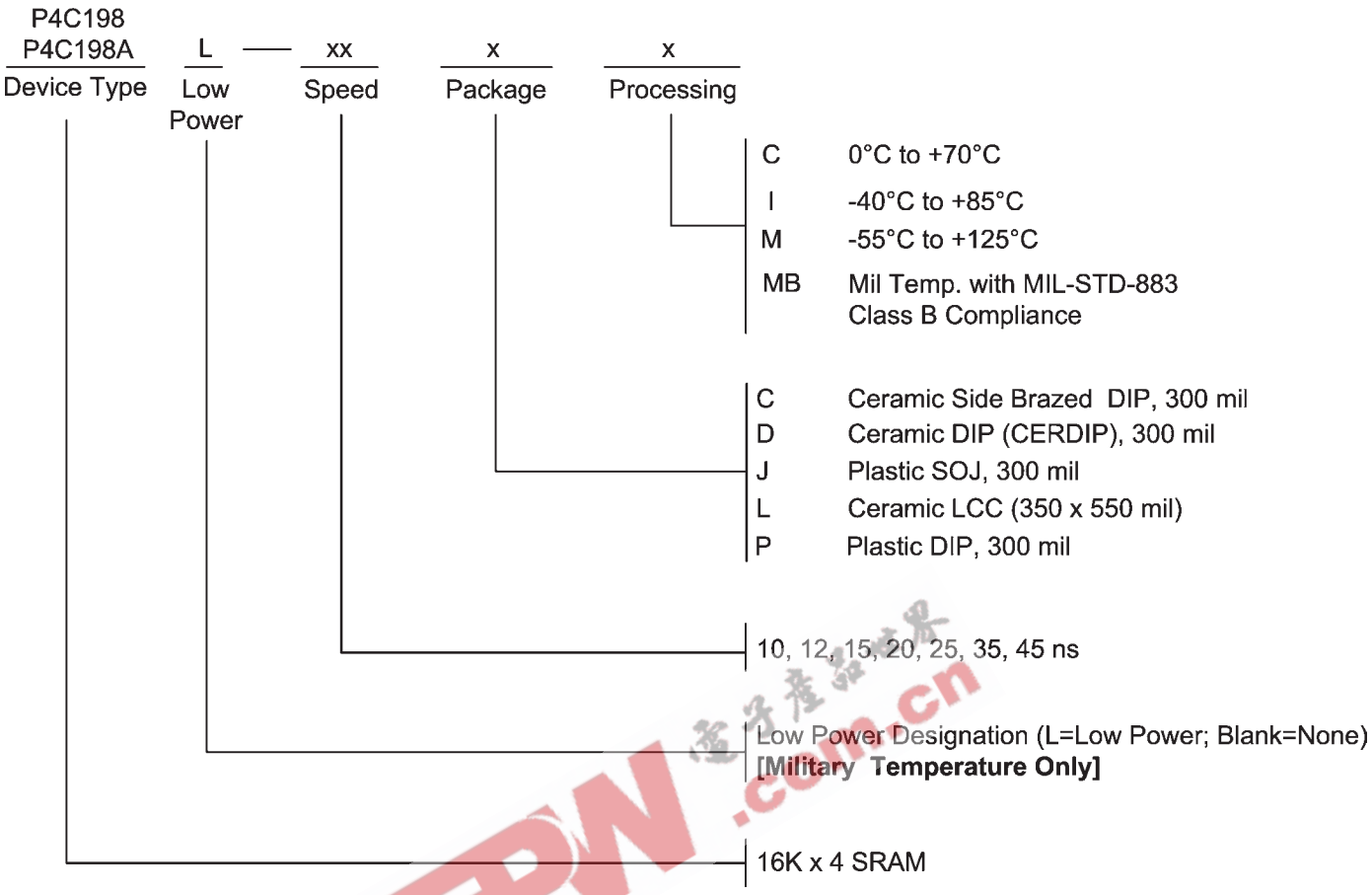


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C198/L and P4C198A/L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



SELECTION GUIDE

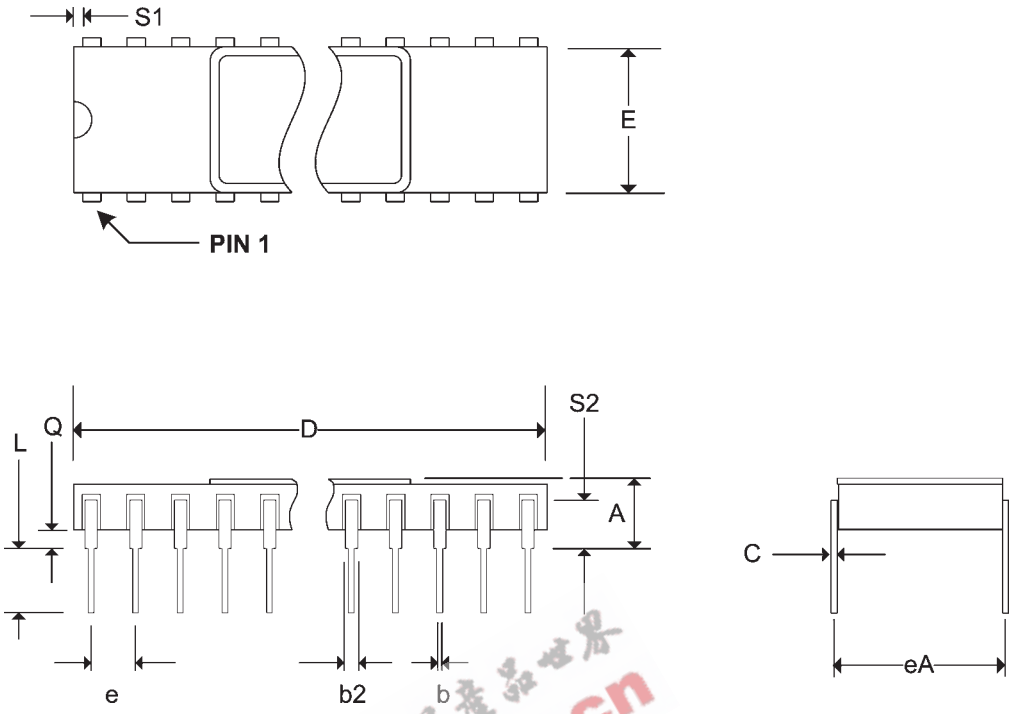
The P4C198 and P4C198A are available in the following temperature, speed and package options.

Temperature Range	Package	Speed (ns)						
		10	12	15	20	25	35	45
Commercial	Plastic DIP	-10PC	-12PC	-15PC	-20PC	-25PC	N/A	N/A
	Plastic SOJ	-10JC	-12JC	-15JC	-20JC	-25JC	N/A	N/A
Industrial	Plastic DIP	N/A	-12PI	-15PI	-20PI	-25PI	-35PI	N/A
	Plastic SOJ	N/A	-12JI	-15JI	-20JI	-25JI	-35JI	N/A
Military Temperature	Side Brazed DIP	N/A	N/A	-15CM	-20CM	-25CM	-35CM	-45CM
	CERDIP	N/A	N/A	-15DM	-20DM	-25DM	-35DM	-45DM
	LCC	N/A	N/A	-15LM	-20LM	-25LM	-35LM	-45LM
Military Processed*	Side Brazed DIP	N/A	N/A	-15CMB	-20CMB	-25CMB	-35CMB	-45CMB
	CERDIP	N/A	N/A	-15DMB	-20DMB	-25DMB	-35DMB	-45DMB
	LCC	N/A	N/A	-15LMB	-20LMB	-25LMB	-35LMB	-45LMB

* Military temperature range with MIL-STD-883, Class B processing.
N/A = Not available

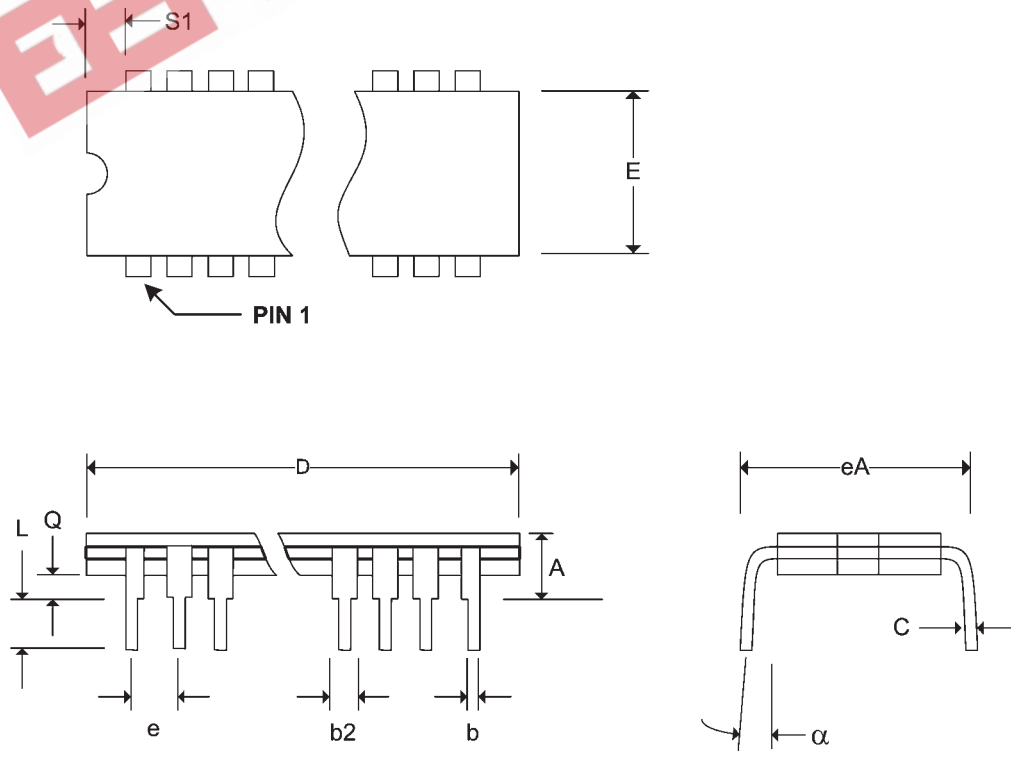
Pkg #	C4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDE BRAZED DUAL IN-LINE PACKAGE



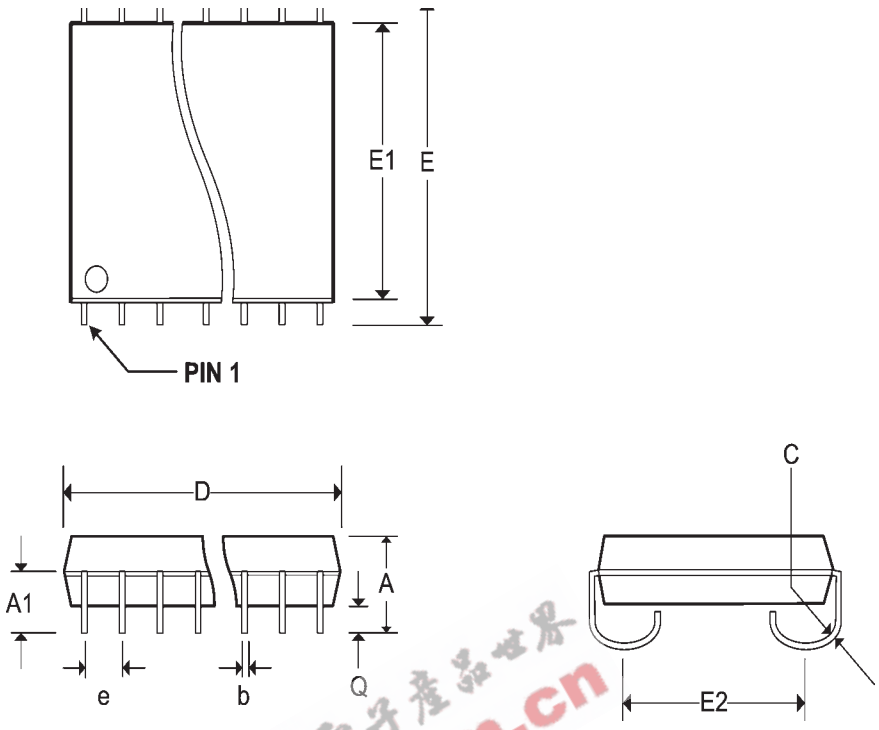
Pkg #	D4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
α	0°	15°

CERDIP DUAL IN-LINE PACKAGE



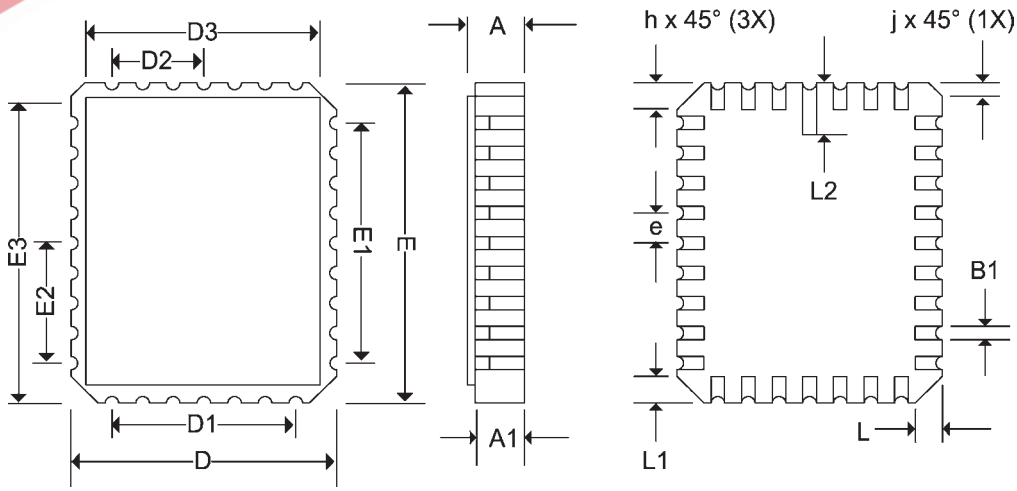
Pkg #	J4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.016	0.020
C	0.007	0.010
D	0.620	0.630
e	0.050 BSC	
E	0.335 BSC	
E1	0.292	0.300
E2	0.267 BSC	
Q	0.025	-

SOJ SMALL OUTLINE IC PACKAGE



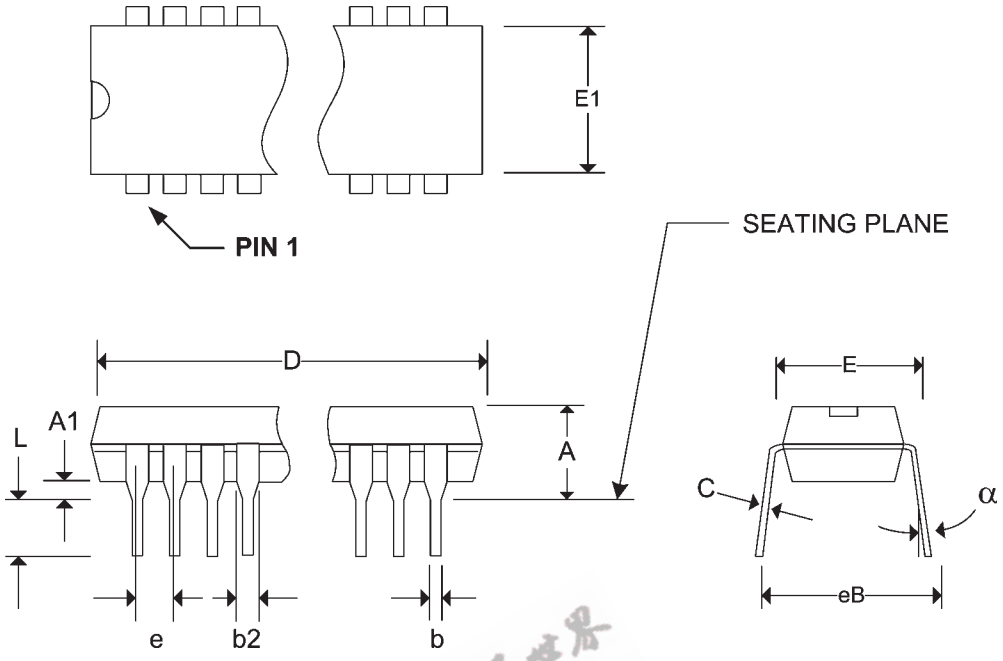
Pkg #	L5	
# Pins	28	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	-	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER



Pkg #	P4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	1.230	1.280
E1	0.240	0.280
E	0.300	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



REVISIONS

DOCUMENT NUMBER:	SRAM113
DOCUMENT TITLE:	P4C198 / P4C198L, P4C198A / P4C198AL ULTRA HIGH SPEED 16K x 4 STATIC CMOS RAMS

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-05	JDB	Change logo to Pyramid