512K × 4 BANKS × 32 BITS SDRAM

GENERAL DESCRIPTION

W986432DH is a high-speed synchronous dynamic random access memory (SDRAM), organized as 512K words × 4 banks × 32 bits. Using pipelined architecture and 0.175 µm process technology, W986432DH delivers a data bandwidth of up to 800M bytes per second (5). For different application, W986432DH is sorted into four speed grades: -5, -55, -6, -7,-8.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W986432DH is ideal for main memory in high performance applications.

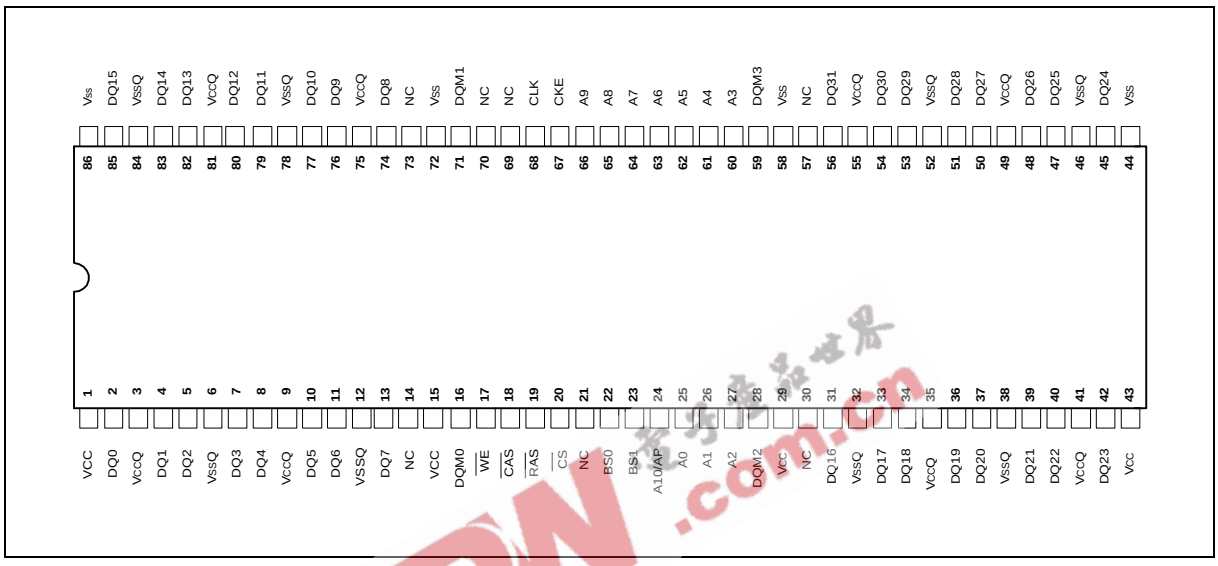
FEATURES

- 3.3V ±0.3V power supply
- 524288 words × 4 banks × 32 bits organization
- Auto Refresh and Self Refresh
- CAS latency: 2 and 3
- Burst Length: 1, 2, 4, 8, and full page
- Sequential and Interleave burst
- Burst read, single write operation
- Byte data controlled by DQM
- Power-down Mode
- Auto-precharge and controlled precharge
- 4K refresh cycles/64 mS
- Interface: LVTTL
- Packaged in 86-pin TSOP II, 400 mil - 0.50

Winbond Electronics Corp.

512K × 4 BANKS × 32 BITS SDRAM

PIN CONFIGURATION

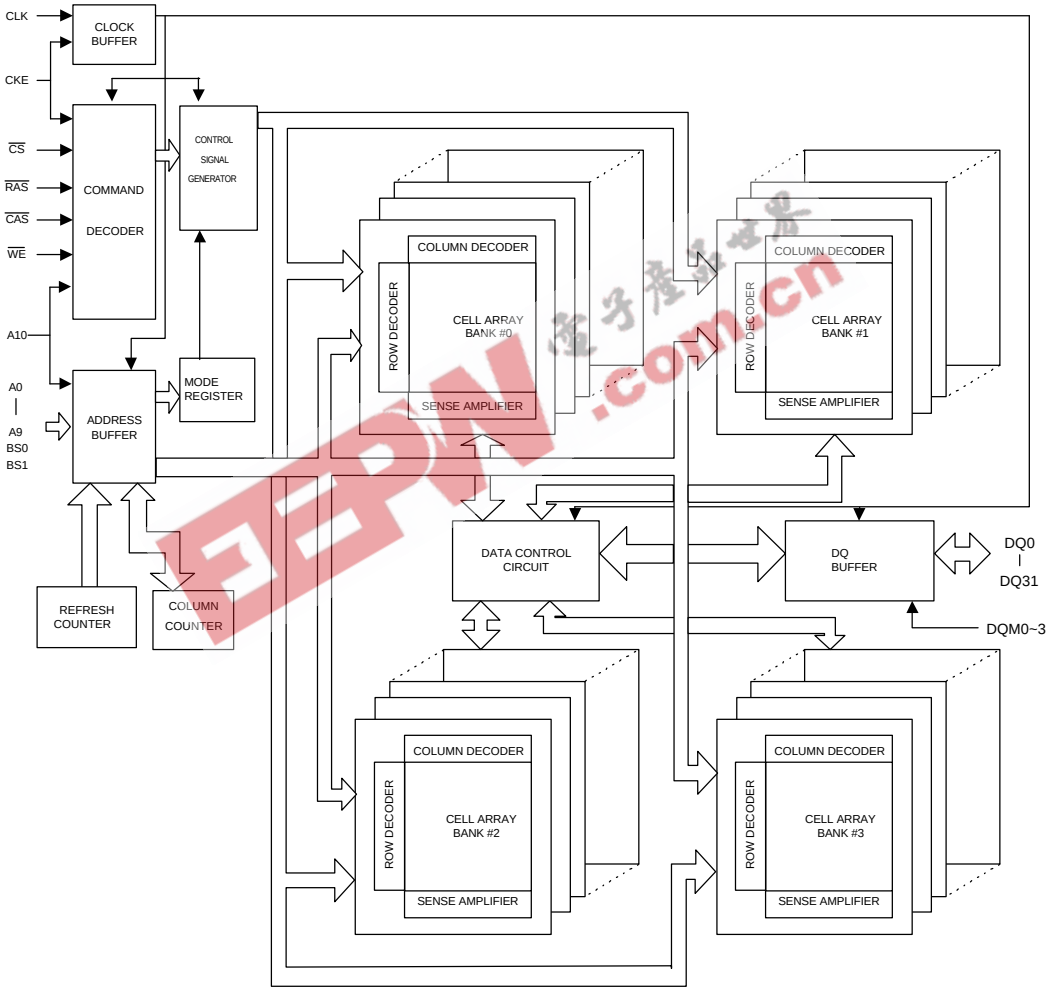


PIN DESCRIPTION

PIN NAME	FUNCTION	DESCRIPTION
A0–A10	Address	Multiplexed pins for row and column address. Row address: A0–A10. Column address: A0–A7. A10 is sampled during a precharge command to determine if all banks are to be precharged or bank selected by BS0, BS1.
BS0, BS1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
DQ0–DQ31	Data Input/ Output	Multiplexed pins for data output and input.
$\overline{CS}$	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
$\overline{RAS}$	Row Address Strobe	Command input. When sampled at the rising edge of the clock $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed.
$\overline{CAS}$	Column Address Strobe	Referred to $\overline{RAS}$
$\overline{WE}$	Write Enable	Referred to $\overline{RAS}$

DQM0– DQM3	Input/output mask	The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
V_{CC}	Power (+3.3V)	Power for input buffers and logic circuit inside DRAM.
V_{SS}	Ground	Ground for input buffers and logic circuit inside DRAM.
V_{CCQ}	Power (+3.3V) for I/O buffer	Separated power from Vcc, to improve DQ noise immunity.
V_{SSQ}	Ground for I/O buffer	Separated ground from Vss, to improve DQ noise immunity.
NC	No Connection	No connection

BLOCK DIAGRAM



NOTE:
The cell array configuration is 2048 * 256 * 32

DC CHARACTERISTICS

Absolute Maximum Rating

PARAMETER	SYM.	RATING	UNIT	NOTES
Input, Column Output Voltage	V_{IN}, V_{OUT}	-0.3 – V_{CC} +0.3	V	1
Power Supply Voltage	V_{CC}, V_{CCQ}	-0.3 – 4.6	V	1
Operating Temperature	T_{OPR}	0 – 70	°C	1
Storage Temperature	T_{STG}	-55 – 150	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70°C)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	NOTES
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	2
Power Supply Voltage (for I/O Buffer)	V_{CCQ}	3.0	3.3	3.6	V	2
Input High Voltage	V_{IH}	2.0	-	V_{CC} +0.3	V	2
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	2

Note: V_{IH} (max.) = V_{CC}/V_{CC}Q+1.2V for pulse width ≤ 5 nS

V_{IL} (min.) = V_{SS}/V_{SS}Q-1.2V for pulse width ≤ 5 nS

CAPACITANCE

(V_{DD} = 3.3V, T_A = 25 °C, f = 1 MHz)

PARAMETER	SYM.	MIN.	MAX.	UNIT
Input Capacitance (A0 to A11, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, CKE)	C_i	2.5	4	pf
Input Capacitance (CLK)	C_{CLK}	2.5	4	pf
Input/Output capacitance (DQ0–DQ31)	C_o	4	6.5	pf

Note: These parameters are periodically sampled and not 100% tested

DC CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, T_A = 0°~70°C)

PARAMETER		SYM.	-5	-55	-6	-7	-8	UNIT	NOTES
			MAX.	MAX.	MAX.	MAX.	MAX.		
Operating Current t_{CK} = min., t_{RC} = min. Active precharge command cycling without burst operation	1 bank operation	I_{CC1}	TBD	TBD	TBD	TBD	TBD		3
Standby Current t_{CK} = min., $\overline{CS}$ = V_{IH} $V_{IH/L}$ = V_{IH} (min.)/V_{IL} (max.) Bank: inactive state	CKE = V_{IH}	I_{CC2}	TBD	TBD	TBD	TBD	TBD		3
	CKE = V_{IL} (Power Down mode)	I_{CC2P}	TBD	TBD	TBD	TBD	TBD		3
Standby Current CLK = V_{IL}, $\overline{CS}$ = V_{IH} $V_{IH/L}$=V_{IH} (min.)/V_{IL} (max.) BANK: inactive state	CKE = V_{IH}	I_{CC2S}	TBD	TBD	TBD	TBD	TBD		
	CKE = V_{IL} (Power Down mode)	I_{CC2P} S	TBD	TBD	TBD	TBD	TBD	mA	
No Operating Current t_{CK} = min., $\overline{CS}$ = V_{IH} (min.) BANK: active state (4 banks)	CKE = V_{IH}	I_{CC3}	TBD	TBD	TBD	TBD	TBD		
	CKE = V_{IL} (Power Down mode)	I_{CC3P}	TBD	TBD	TBD	TBD	TBD		
Burst Operating Current Read/Write command cycling	(t_{CK} = min.)	I_{CC4}	TBD	TBD	TBD	TBD	TBD		3, 4
Auto Refresh Current Auto refresh command cycling	(t_{CK} = min.)	I_{CC5}	TBD	TBD	TBD	TBD	TBD		3
Self Refresh Current Self refresh mode	(CKE = 0.2V)	I_{CC6}	TBD	TBD	TBD	TBD	TBD		

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTES
Input Leakage Current (0V ≤ V_{IN} ≤ V_{CC}, all other pins not under test = 0V)	I_I(L)	-5	5	µA	
Output Leakage Current 7(Output disable, 0V ≤ V_{OUT} ≤ V_{CC}Q)	V_O(L)	-5	5	µA	
LVTTL Output "H" Level Voltage (I_{OUT} = -2 mA)	V_{OH}	2.4	-	V	
LVTTL Output "L" Level Voltage (I_{OUT} = 2 mA)	V_{OL}	-	0.4	V	

AC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = 0 to 70 °C) (Notes: 5, 6.)

PARAMETER	Symbol	-5		-55		-6		UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
Ref/Active to Ref/Active Command Period	tRC	54		55		60		ns	
Active to precharge Command Period	tRAS	40	100000	40	100000	42	100000		
Active to Read/Write Command Delay Time	tRCD	14		15		18			
Read/Write(a) to Read/Write(b)Command Period	tCCD	1		1		1		Cycle	
Precharge to Active(b) Command Period	tRP	14		15		18		ns	
Active(a) to Active(b) Command Period	tRRD	10		10.8		12			
Write Recovery Time CL* = 2	tWR	7		7.5		7.5			
CL* = 3		5		5.4		6			
CLK Cycle Time CL* = 2	tCK	7	1000	7.5	1000	7.5	1000		
CL* = 3		5	1000	5.4	1000	6	1000		
CLK High Level	tCH	2		2		2			
CLK Low Level	tCL	2		2		2			
Access Time from CLK CL* = 2	tAC		4.5		5.5		5.5		
CL* = 3			4.5		5		5		
Output Data Hold Time	tOH	2.75		2.75		2.75			
Output Data High Impedance Time	tHZ	2.75	5	2.75	5.4	2.75	6		
Output Data Low Impedance Time	tLZ	0		0		0			
Power Down Mode Entry Time	tSB	0	5	0	5.4	0	6		
Transition Time of CLK (Rise and Fall)	tT	0.5	10	0.5	10	0.5	10		
Data-in-Set-up Time	tDS	1		1.5		1.5			
Data-in Hold Time	tDH	0.5		0.5		0.5			
Address Set-up Time	tAS	1.3		1.5		1.5			
Address Hold Time	tAH	0.8		1		0.5			
CKE Set-up Time	tCKS	1.3		1.5		1.5			
CKE Hold Time	tCKH	0.8		1		0.5			
Command Set-up Time	tCMS	1		1.5		1.5			
Command Hold Time	tCMH	0.5		0.5		0.5			
Refresh Time	tREF		64		64		64	ms	
Mode Register Set Cycle Time	tRSC	10		10.8		12		ns	

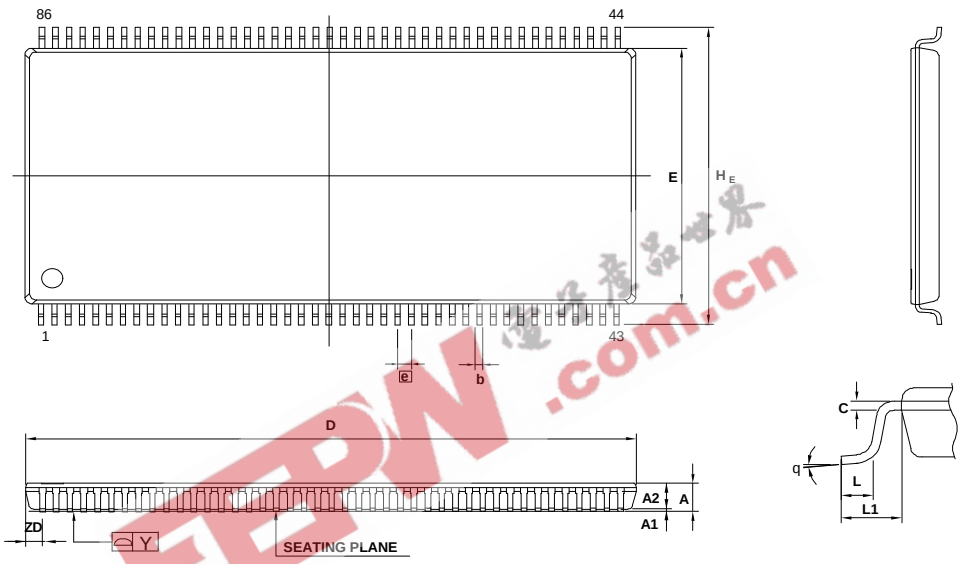
AC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, Ta = 0 to 70 °C) (Notes: 5, 6.)

PARAMETER	Symbol	-7		-8				UNIT	NOTE
		MIN	MAX	MIN	MAX	MIN	MAX		
Ref/Active to Ref/Active Command Period	tRC	65		68				ns	
Active to precharge Command Period	tRAS	45	100000	48	100000				
Active to Read/Write Command Delay Time	tRCD	20		20					
Read/Write(a) to Read/Write(b)Command Period	tCCD	1		1				Cycle	
Precharge to Active(b) Command Period	tRP	20		20				ns	
Active(a) to Active(b) Command Period	tRRD	14		20					
Write Recovery Time CL* = 2	tWR	7.5		10					
CL* = 3		7		8					
CLK Cycle Time CL* = 2	tCK	7.5	1000	10	1000				
CL* = 3		7	1000	8	1000				
CLK High Level	tCH	2		3					
CLK Low Level	tCL	2		3					
Access Time from CLK CL* = 2	tAC		5.5		6				
CL* = 3			5		6				
Output Data Hold Time	tOH	3		3					
Output Data High Impedance Time	tHZ	3	7	3	8				
Output Data Low Impedance Time	tLZ	0		0					
Power Down Mode Entry Time	tSB	0	7	0	8				
Transition Time of CLK (Rise and Fall)	tT	0.5	10	0.5	10				
Data-in-Set-up Time	tDS	0.5		2					
Data-in Hold Time	tDH	1		1					
Address Set-up Time	tAS	0.5		2					
Address Hold Time	tAH	1		1					
CKE Set-up Time	tCKS	0.5		2					
CKE Hold Time	tCKH	1		1					
Command Set-up Time	tCMS	0.5		2					
Command Hold Time	tCMH	1		1					
Refresh Time	tREF		64		64			ms	
Mode Register Set Cycle Time	tRSC	14		16				ns	

PACKAGE DIMENSIONS

86L TSOP (II)-400 mil



Controlling Dimension: Millimeters

SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	—	1.00	—	—	0.039	—
b	0.17	—	0.27	0.007	—	0.011
c	0.12	—	0.21	0.005	—	0.008
D	22.12	22.22	22.62	0.871	0.875	0.905
E	10.06	10.16	10.26	0.396	0.400	0.404
H E	11.56	11.76	11.96	0.455	0.463	0.471
e	—	0.50	—	—	0.020	—
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	—	0.80	—	—	0.032	—
Y	—	—	0.10	—	—	0.004
ZD	—	0.61	—	—	0.024	—

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