TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

# 4-MBIT (512K × 8 BITS / 256K × 16 BITS) CMOS FLASH MEMORY

## DESCRIPTION

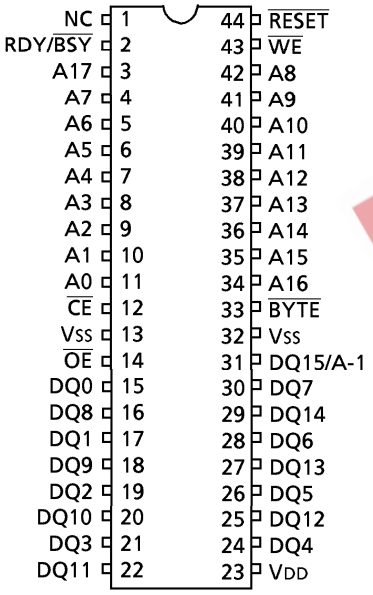
The TC58FVT400/B400 is a 4,194,304 - bit, 3.0-V read-only electrically erasable and programmable flash memory organized as 524,288 words × 8 bits or as 262,144 words × 16 bits. The TC58FVT400/B400 features commands for Read, Program and Erase operations to allow easy interfacing with microprocessors. The commands are based on the JEDEC standard. The Program and Erase operations are automatically executed in the chip. The device has Chip, Block and Multi - Block Erase capability.

The TC58FVT400/B400 is available in either a 44-pin plastic SOP, a 48-pin TSOP package to suit a variety of design applications.

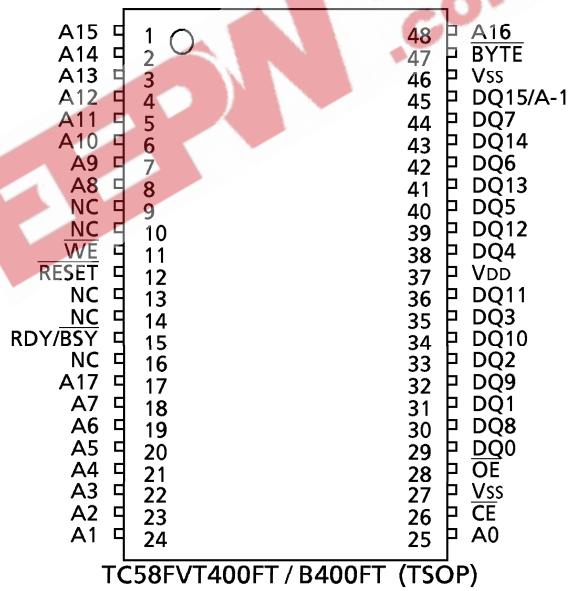
## FEATURES

- Power Supply
  $V_{DD}$ = 2.7 V to 3.6 V
- Organization
  512K × 8 bits / 256K × 16 bits
- Modes
  Auto Program, Auto Chip Erase
  Auto Block Erase, Auto Multiple Block Erase
  Erase Suspend / Resume, Block Protection
  Data Polling / Toggle Bit
- Block Erase Architecture
  1 × 16 Kbytes / 2 × 8 Kbytes /
  1 × 32 Kbytes / 7 × 64 Kbytes
- Boot Block Architecture
  TC58FVT400F/FT ····· Top Boot Block
  TC58FVB400F/FT ····· Bottom Boot Block
- Mode Control
  Compatible with JEDEC standard commands
- Erase / Program Cycles
  $10^5$ Cycles typ.
- Access Time
  85 ns ($V_{DD}$ = 3.0 V to 3.6 V)
  100 ns / 120 ns ($V_{DD}$ = 2.7 V to 3.0 V)
- Power Dissipation
  250 μA (Standby TTL level)
  10 μA (Standby CMOS level)
  30 mA (Read operation)
  40 mA (Program / Erase Operations)
- Package
  TC58FVT400F/B400F : SOP44 - P - 600 - 1.27
  (Weight: 2.05 g typ.)
  TC58FVT400FT/B400FT : TSOP I 48 - P - 1220 - 0.50
  (Weight: 0.53 g typ.)

## PIN ASSIGNMENT (TOP VIEW)




TC58FVT400F/B400F (SOP)



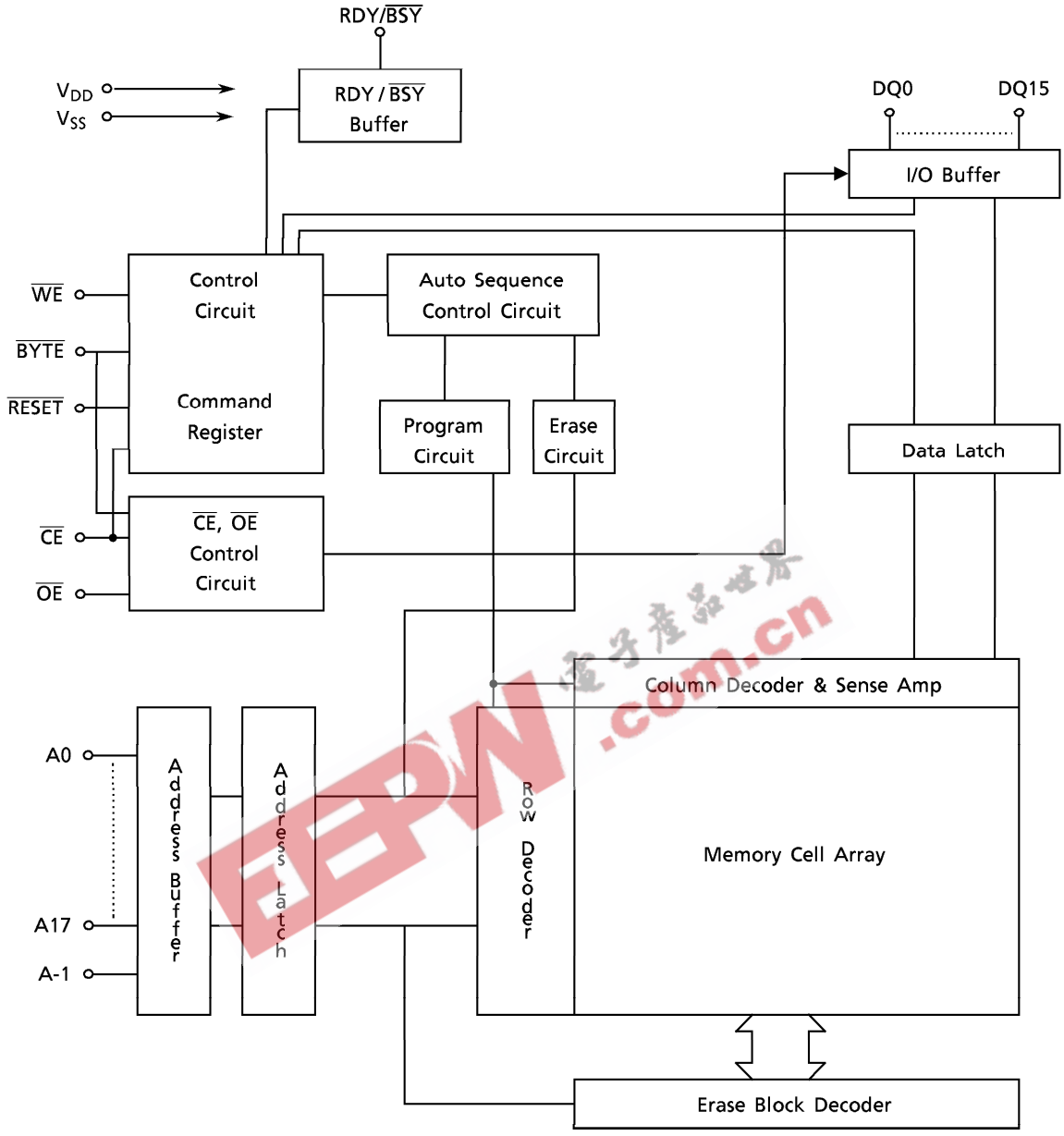

TC58FVT400FT / B400FT (TSOP)

## PIN NAMES

| | |
|---|---|
| A0 to A17 | Address Input |
| DQ0 to DQ14 | Data Input / Output |
| DQ15/A-1 | Output (Input) / Address Input |
| $\overline{CE}$ | Chip Enable Input |
| $\overline{OE}$ | Output Enable Input |
| $\overline{BYTE}$ | Word/Byte Select Input |
| $\overline{WE}$ | Write Enable Input |
| RDY/$\overline{BSY}$ | Ready/Busy Output |
| $\overline{RESET}$ | Hardware Reset Input |
| NC | No Connection |
| $V_{DD}$ | Power Supply |
| $V_{SS}$ | Ground |

961001EBA1

## BLOCK DIAGRAM



## MODE SELECTION

| | | | | | | | | | BYTE MODE | WORD MODE |
|---|---|---|---|---|---|---|---|---|---|---|
| MODE | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | A9 | A6 | A1 | A0 | $\overline{RESET}$ | DQ0 to DQ7 [1] | DQ0 to DQ15 |
| Read | L | L | H | A9 | A6 | A1 | A0 | H | Dout | Dout |
| ID Read (Manufacturer Code) | L | L | H | $V_{ID}$ | L | L | L | H | Code | Code |
| ID Read (Device Code) | L | L | H | $V_{ID}$ | L | L | H | H | Code | Code |
| Standby | H | * | * | * | * | * | * | H | High-Z | High-Z |
| Output Disable | * | H | H | * | * | * | * | * | High-Z | High-Z |
| Write | L | H | L | A9 | A6 | A1 | A0 | H | Din | Din |
| Block Protect | L | $V_{ID}$ | L | $V_{ID}$ | L | H | L | H | * | * |
| Verify Block Protect | L | L | H | $V_{ID}$ | L | H | L | H | Code | Code |
| Temporary Block Unprotect | * | * | * | * | * | * | * | $V_{ID}$ | * | * |
| Hardware Reset / Standby | * | * | * | * | * | * | * | L | High-Z | High-Z |

Notes: * : $V_{IH}$ or $V_{IL}$
1) DQ8 to DQ15 are High-Z in Byte mode.

## ID CODE TABLE

| CODE TYPE | | A17 to A12 | A6 | A1 | A0 | CODE (HEX) [1] |
|---|---|---|---|---|---|---|
| Manufacturer Code | | * | $V_{IL}$ | $V_{IL}$ | $V_{IL}$ | 0098H |
| Device Code | TC58FVT400 | * | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 0CDH |
| | TC58FVB400 | * | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | 004CH |
| Verify Block Protect | | BA [2] | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Data [3] |

Notes: * : $V_{IH}$ or $V_{IL}$
1) DQ8 to DQ15 are High-Z in Byte mode
2) BA: Block Address
3) 0001H – Protected Block
0000H – Unprotected Block
$\overline{BYTE}$ = $V_{IL}$ : Byte mode
$\overline{BYTE}$ = $V_{IH}$ : Word mode

## COMMAND DEFINITIONS

| COMMAND SEQUENCE | | BUS WRITE CYCLES REQ'D | FIRST BUS WRITE CYCLE | | SECOND BUS WRITE CYCLE | | THIRD BUS WRITE CYCLE | | FOURTH BUS READ/WRITE CYCLE | | FIFTH BUS WRITE CYCLE | | SIXTH BUS WRITE CYCLE | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data | Addr. | Data |
| Read/Reset | | 1 | XXXXH | F0H | | | | | | | | | | |
| Read/Reset | Word | 3 | 5555H | AAH | 2AAAH | 55H | 5555H | F0H | RA [1] | RD [2] | | | | |
| | Byte | | AAAAH | | 5555H | | AAAAH | | | | | | | |
| ID Read/ Verify Block Protect | Word | 3 | 5555H | AAH | 2AAAH | 55H | 5555H | 90H | IA [3] | ID [4] | | | | |
| | Byte | | AAAAH | | 5555H | | AAAAH | | | | | | | |
| Auto Program | Word | 4 | 5555H | AAH | 2AAAH | 55H | 5555H | A0H | PA [5] | PD [6] | | | | |
| | Byte | | AAAAH | | 5555H | | AAAAH | | | | | | | |
| Auto Chip Erase | Word | 6 | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | 5555H | 10H |
| | Byte | | AAAAH | | 5555H | | AAAAH | | AAAAH | | 5555H | | AAAAH | |
| Auto Block Erase | Word | 6 | 5555H | AAH | 2AAAH | 55H | 5555H | 80H | 5555H | AAH | 2AAAH | 55H | BA [7] | 30H |
| | Byte | | AAAAH | | 5555H | | AAAAH | | AAAAH | | 5555H | | | |
| Block Protect | Word | 6 | 5555H | AAH | 2AAAH | 55H | 5555H | 9AH | 5555H | AAH | 2AAAH | 55H | 5555H | 9AH |
| | Byte | | AAAAH | | 5555H | | AAAAH | | AAAAH | | 5555H | | AAAAH | |
| Block Erase Suspend | | | Addr: $V_{IH}$ or $V_{IL}$, Data: B0H | | | | | | | | | | | |
| Block Erase Resume | | | Addr: $V_{IH}$ or $V_{IL}$, Data: 30H | | | | | | | | | | | |

Notes: The system should generate the following address patterns:
Word mode: 5555H or 2AAAH to addresses A14 to A0
Byte mode: AAAAH or 5555H to addresses A14 to A-1

DQ8 to DQ15 are ignored in Word mode.

1) RA : Read Address
2) RD : Read Data
3) IA : ID Address (A6, A1, A0)
00H = Manufacturer Code
01H = Device Code
02H = Verify Block Protect (A17 to A12 = Block Address)

4) ID : ID Data
0098H – Manufacturer Code
00CDH – Device Code (TC58FVT400)
004CH – Device Code (TC58FVB400)
0001H – Protected Block
0000H – Unprotected Block

5) PA : Program Address
6) PD : Program Data
7) BA : Block Address

Addresses are A17 : A1 in Byte mode ($\overline{BYTE}$ = $V_{IL}$)
Addresses are A17 : A0 in Word mode ($\overline{BYTE}$ = $V_{IH}$)

## HARDWARE STATUS FLAGS

| STATUS | | DQ7 | DQ6 | DQ5 | DQ3 | RDY/$\overline{BSY}$ |
|---|---|---|---|---|---|---|
| In Progress | Auto Programming | $\overline{DQ7}$ | Toggle | 0 | 0 | 0 |
| | Auto Erase (Erase Hold Time) | 0 | Toggle | 0 | 0 | 0 |
| | Auto Erase | 0 | Toggle | 0 | 1 | 0 |
| Time Limits Exceeded | Auto Programming | $\overline{DQ7}$ | Toggle | 1 | 1 | 0 |
| | Auto Erase | 0 | Toggle | 1 | 1 | 0 |

Notes: 1. DQ outputs cell data and RDY/$\overline{BSY}$ outputs 1 when the operation has completed.
2. DQ0, DQ1 and DQ2 pins are reserved for future use.
3. DQ8 to DQ15 : Output 0 or 1 in Word mode.
4. DQ0 to DQ2 and DQ4 : Output 0.

## BLOCK ERASE ADDRESS TABLES

TC58FVT400 (Top Boot Block)

| BLOCK # | A17 | A16 | A15 | A14 | A13 | A12 | BYTE MODE | | WORD MODE | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | ADDRESS RANGE | SIZE | ADDRESS RANGE | SIZE |
| BA0 | L | L | L | * | * | * | 00000h to 0FFFFh | 64 K byte | 00000h to 07FFFh | 32 K word |
| BA1 | L | L | H | * | * | * | 10000h to 1FFFFh | 64 K byte | 08000h to 0FFFFh | 32 K word |
| BA2 | L | H | L | * | * | * | 20000h to 2FFFFh | 64 K byte | 10000h to 17FFFh | 32 K word |
| BA3 | L | H | H | * | * | * | 30000h to 3FFFFh | 64 K byte | 18000h to 1FFFFh | 32 K word |
| BA4 | H | L | L | * | * | * | 40000h to 4FFFFh | 64 K byte | 20000h to 27FFFh | 32 K word |
| BA5 | H | L | H | * | * | * | 50000h to 5FFFFh | 64 K byte | 28000h to 2FFFFh | 32 K word |
| BA6 | H | H | L | * | * | * | 60000h to 6FFFFh | 64 K byte | 30000h to 37FFFh | 32 K word |
| BA7 | H | H | H | L | * | * | 70000h to 77FFFh | 32 K byte | 38000h to 3BFFFh | 16 K word |
| BA8 | H | H | H | H | L | L | 78000h to 79FFFh | 8 K byte | 3C000h to 3CFFFh | 4 K word |
| BA9 | H | H | H | H | L | H | 7A000h to 7BFFFh | 8 K byte | 3D000h to 3DFFFh | 4 K word |
| BA10 | H | H | H | H | H | * | 7C000h to 7FFFFh | 16 K byte | 3E000h to 3FFFFh | 8 K word |

* : $V_{IH}$ or $V_{IL}$

TC58FVB400 (Bottom Boot Block)

| BLOCK # | A17 | A16 | A15 | A14 | A13 | A12 | BYTE MODE | | WORD MODE | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | ADDRESS RANGE | SIZE | ADDRESS RANGE | SIZE |
| BA0 | L | L | L | L | L | * | 00000h to 03FFFh | 16 K byte | 00000h to 01FFFh | 8 K word |
| BA1 | L | L | L | L | H | L | 04000h to 05FFFh | 8 K byte | 02000h to 02FFFh | 4 K word |
| BA2 | L | L | L | L | H | H | 06000h to 07FFFh | 8 K byte | 03000h to 03FFFh | 4 K word |
| BA3 | L | L | L | H | * | * | 08000h to 0FFFFh | 32 K byte | 04000h to 07FFFh | 16 K word |
| BA4 | L | L | H | * | * | * | 10000h to 1FFFFh | 64 K byte | 08000h to 0FFFFh | 32 K word |
| BA5 | L | H | L | * | * | * | 20000h to 2FFFFh | 64 K byte | 10000h to 17FFFh | 32 K word |
| BA6 | L | H | H | * | * | * | 30000h to 3FFFFh | 64 K byte | 18000h to 1FFFFh | 32 K word |
| BA7 | H | L | L | * | * | * | 40000h to 4FFFFh | 64 K byte | 20000h to 27FFFh | 32 K word |
| BA8 | H | L | H | * | * | * | 50000h to 5FFFFh | 64 K byte | 28000h to 2FFFFh | 32 K word |
| BA9 | H | H | L | * | * | * | 60000h to 6FFFFh | 64 K byte | 30000h to 37FFFh | 32 K word |
| BA10 | H | H | H | * | * | * | 70000h to 7FFFFh | 64 K byte | 38000h to 3FFFFh | 32 K word |

* : $V_{IH}$ or $V_{IL}$

The Addresses are A17 : A-1 in Byte Mode ($\overline{BYTE} = V_{IL}$)
The Addresses are A17 : A0 in Word Mode ($\overline{BYTE} = V_{IH}$)

## ABSOLUTE MAXIMUM RATINGS

| SYMBOL | PARAMETER | RANGE | UNIT |
|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ Supply Voltage | −0.6 to 4.6 | V |
| $V_{IN}$ | Input Voltage | −0.6 to $V_{DD}$ + 0.5 (≦4.6) | V |
| $V_{DQ}$ | Input / Output Voltage | −0.6 to $V_{DD}$ + 0.5 (≦4.6) | V |
| $P_D$ | Power Dissipation | 0.6 | W |
| $T_{SOLDER}$ | Soldering Temperature (10 s) | 260 | °C |
| $T_{STG}$ | Storage Temperature | −55 to 150 | °C |
| $T_{OPR}$ | Operating Temperature | −40 to 85 | °C |
| $N_{EW}$ | Erase / Program Cycling Capability | 100,000 | Cycles |
| $V_{IDH}$ | Maximum Input Voltage 1) | 13.0 | V |
| $I_{OSHORT}$ | Output Short Circuit Current 2) | 100 | mA |

1) $V_{IDH}$ supply for more than 10 seconds is not recommended. The device could be damaged.
2) Outputs should be shorted for no more than one second.
No more than one output should be shorted at a time.

## CAPACITANCE (Ta = 25°C, f = 1 MHz)

| SYMBOL | PARAMETER | CONDITION | TYP. | MAX | UNIT |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Pin Capacitance | $V_{IN}$ = 0 V | 4 | 8 | pF |
| $C_{OUT}$ | Output Pin Capacitance | $V_{OUT}$ = 0 V | 10 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 V | 8 | 10 | pF |

This parameter is periodically sampled and is not tested for every device.

## RECOMMENDED DC OPERATING CONDITIONS (Ta = −40 to 85°C)

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ Supply Voltage | 2.7 | 3.6 | V |
| $V_{IH}$ | Input High Level Voltage | 0.7 $V_{DD}$ | $V_{DD}$ + 0.5 | |
| $V_{IL}$ | Input Low Level Voltage | −0.3 1) | 0.8 | |
| $V_{ID}$ | Voltage for ID Read and Block Protect 2) | 11.4 | 12.6 | |

1) −2 V (pulse width of 20 ns Max)
2) $V_{IDH}$ supply for more than 10 seconds is not recommended. The device could be damaged.

## DC CHARACTERISTICS (Ta = –40 to 85°C, $V_{DD}$ = 2.7 to 3.6 V)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | 0 V ≦ $V_{IN}$ ≦ $V_{DD}$ | – | ± 1 | μA |
| $I_{LO}$ | Output Leakage Current | 0 V ≦ $V_{OUT}$ ≦ $V_{DD}$ | – | ± 1 | |
| $V_{OH1}$ | Output High Voltage (TTL) | $I_{OH}$ = –0.4 mA | 2.4 | – | V |
| $V_{OH2}$ | Output High Voltage (CMOS) | $I_{OH}$ = –0.1 mA | $V_{DD}$ – 0.4 | – | |
| | | $I_{OH}$ = –2.5 mA | 0.85 × $V_{DD}$ | – | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4.0 mA | – | 0.4 | |
| $I_{DDO1}$ | $V_{DD}$ Average Read Current | $V_{IN}$ = $V_{IH}$ / $V_{IL}$, $I_{OUT}$ = 0 mA<br>CYCLE = $t_{RC}$ (min) | – | 30 | mA |
| $I_{DDO2}$ | $V_{DD}$ Average Program Current | $V_{IN}$ = $V_{IH}$ / $V_{IL}$, $I_{OUT}$ = 0 mA | – | 40 | |
| $I_{DDO3}$ | $V_{DD}$ Average Erase Current | $V_{IN}$ = $V_{IH}$ / $V_{IL}$, $I_{OUT}$ = 0 mA | – | 40 | |
| $I_{DDS1}$ | $V_{DD}$ Standby Current (TTL) | $\overline{CE}$ = $\overline{RESET}$ = $V_{IH}$ or $\overline{RESET}$ = $V_{IL}$ | – | 250 | μA |
| $I_{DDS2}$ | $V_{DD}$ Standby Current (CMOS) | $\overline{CE}$ = $\overline{RESET}$ = $V_{DD}$ ± 0.2 V<br>or $\overline{RESET}$ = $V_{SS}$ ± 0.2 V | – | 10 | |
| $I_{ID}$ | High Voltage Input Current | 11.4 V ≦ $V_{ID}$ ≦ 12.6 1) | – | 200 | |
| $V_{LKO}$ | Low $V_{DD}$ Lock-out Voltage | – | – | 2.5 | V |

1) Less than 10 seconds

## AC TEST CONDITIONS

| PARAMETER | CONDITION |
|---|---|
| Input Pulse Level | 2.4 V / 0.4 V |
| Input Pulse Rise and Fall Time (10% to 90%) | 5 ns |
| Timing Measurement Reference Level (Input) | 1.5 V / 1.5 V |
| Timing Measurement Reference Level (Output) | 1.5 V / 1.5 V |
| Output Load | $C_L$ (100 pF) + 1 TTL Gate |

## AC CHARACTERISTICS AND OPERATING CONDITIONS

| SYMBOL | PARAMETER | -85 | | -10 | | -12 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Ta = –40 to 85 °C | | | | | | |
| | | $V_{DD}$ = 3.0 to 3.6 V | | $V_{DD}$ = 2.7 to 3.6 V | | | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{RC}$ | Read Cycle Time | 85 | – | 100 | – | 120 | – | ns |
| $t_{ACC}$ | Address Access Time | – | 85 | – | 100 | – | 120 | ns |
| $t_{CE}$ | $\overline{CE}$ Access Time | – | 85 | – | 100 | – | 120 | ns |
| $t_{OE}$ | $\overline{OE}$ Access Time | – | 35 | – | 40 | – | 50 | ns |
| $t_{CEE}$ | $\overline{CE}$ to Output Low-Z | 0 | – | 0 | – | 0 | – | ns |
| $t_{OEE}$ | $\overline{OE}$ to Output Low-Z | 0 | – | 0 | – | 0 | – | ns |
| $t_{OEH}$ | $\overline{OE}$ Hold Time (Read) | 0 | – | 0 | – | 0 | – | ns |
| $t_{OH}$ | Output Data Hold Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{DF1}$ | $\overline{CE}$ to Output High-Z | – | 30 | – | 30 | – | 30 | ns |
| $t_{DF2}$ | $\overline{OE}$ to Output High-Z | – | 30 | – | 30 | – | 30 | ns |
| $t_{CMD}$ | Command Write Cycle Time | 85 | – | 100 | – | 120 | – | ns |
| $t_{AS}$ | Address Setup Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{AH}$ | Address Hold Time | 45 | – | 50 | – | 50 | – | ns |
| $t_{DS}$ | Data Setup Time | 45 | – | 50 | – | 60 | – | ns |
| $t_{DH}$ | Data Hold Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{WELH}$ | $\overline{WE}$ Low Level Hold Time * | 45 | – | 50 | – | 50 | – | ns |
| $t_{WEHH}$ | $\overline{WE}$ High Level Hold Time * | 20 | – | 20 | – | 20 | – | ns |
| $t_{CES}$ | $\overline{CE}$ Setup Time to $\overline{WE}$ Active * | 0 | – | 0 | – | 0 | – | ns |
| $t_{CEH}$ | $\overline{CE}$ Hold Time from $\overline{WE}$ High Level * | 0 | – | 0 | – | 0 | – | ns |
| $t_{OES}$ | $\overline{OE}$ Setup to $\overline{WE}$ Active | 0 | – | 0 | – | 0 | – | ns |
| $t_{OEHP}$ | $\overline{OE}$ Hold Time (Toggle / Data Polling) | 10 | – | 10 | – | 10 | – | ns |
| $t_{OEHT}$ | $\overline{OE}$ High Level Hold Time (Toggle) | 20 | – | 20 | – | 20 | – | ns |
| $t_{PPW}$ | Auto Program Time | 16 ** | – | 16 ** | – | 16 ** | – | μs |
| $t_{PCEW}$ | Auto Chip Erase Time | 15 ** | – | 15 ** | – | 15 ** | – | s |
| $t_{PBEW}$ | Auto Block Erase Time | 1.5 ** | – | 1.5 ** | – | 1.5 ** | – | s |
| $t_{VDS}$ | $V_{DD}$ Setup Time | 500 | – | 500 | – | 500 | – | μs |
| $t_{BUSY}$ | Program / Erase Valid to RDY / $\overline{BSY}$ Delay | 35 | – | 40 | – | 50 | – | ns |
| $t_{RP}$ | $\overline{RESET}$ Low Level Hold Time | 500 | – | 500 | – | 500 | – | ns |
| $t_{READY}$ | $\overline{RESET}$ Low Level to Read Mode | – | 20 | – | 20 | – | 20 | μs |
| $t_{RB}$ | RDY / $\overline{BSY}$ Recovery Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{RH}$ | $\overline{RESET}$ Recovery Time | 500 | – | 500 | – | 500 | – | ns |
| $t_{CEBTS}$ | $\overline{CE}$ Setup time $\overline{BYTE}$ Transition | 5 | – | 5 | – | 5 | – | ns |
| $t_{BTD}$ | $\overline{BYTE}$ to Output High-Z | – | 30 | – | 30 | – | 30 | ns |
| $t_{VPT}$ | $V_{ID}$ Transition Time | 4 | – | 4 | – | 4 | – | μs |
| $t_{VPS}$ | $V_{ID}$ Setup Time | 4 | – | 4 | – | 4 | – | μs |
| $t_{VPH}$ | $\overline{OE}$ Hold Time (Block Protect) | 8 | – | 8 | – | 8 | – | μs |
| $t_{PPLH}$ | $\overline{WE}$ Low Level Hold Time (Block Protect) | 100 | – | 100 | – | 100 | – | μs |
| $t_{PAS}$ | Protect Address Setup Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{PAH}$ | Protect Address Hold Time | 0 | – | 0 | – | 0 | – | ns |
| $t_{CESP}$ | $\overline{CE}$ Setup Time (Block Protect) | 4 | – | 4 | – | 4 | – | μs |
| $t_{CEHP}$ | $\overline{CE}$ Hold Time (Block Protect) | 8 | – | 8 | – | 8 | – | μs |

* : $\overline{WE}$ Control ** : Typ.

## OPERATING MODES

### READ MODE

When the device is set to Read mode, it acts as an asynchronous ROM with an access time of 85/100/120 ns. The device is set to Read mode at power-on or when an Auto - Program / Erase operation completes. A software or hardware reset is necessary to return the device to Read mode when an Auto Program / Erase operation fails.

### STANDBY MODE

There are two methods of entering Standby mode: the first involves using both $\overline{CE}$ and $\overline{RESET}$ and the second using only $\overline{RESET}$.

The first method involves using $\overline{CE}$ and $\overline{RESET}$ for mode control. If $V_{DD} \pm 0.2$ V (CMOS level) is applied to $\overline{CE}$ and $\overline{RESET}$ when the device is operating in Read mode, the current is reduced below 10 $\mu$A. Similarly, if $V_{IH}$ (TTL level) is applied to $\overline{CE}$ and $\overline{RESET}$, the current is reduced below 250 $\mu$A. When using $\overline{CE}$ for control, make sure that the device is operating in Read mode; otherwise, it is not possible to enter Standby mode.

The second method involves using only $\overline{RESET}$ for mode control. IF $V_{SS} \pm 0.2$ V (CMOS level) is applied to $\overline{RESET}$ when the device is operating in Read mode, the current is reduced below 10 $\mu$A. Similarly, if $V_{IL}$ (TTL level) is applied to $\overline{RESET}$, the current is reduced below 250 $\mu$A. The difference the control method using $\overline{CE}$ described above, is that if $V_{IL}$ is applied to $\overline{RESET}$ when the device is operating in any mode other than Read mode, it enters Standby mode after stopping the operating which is currently being executed. This is a hardware reset and is described later.

In standby mode, DQ is put in high-impedance state.

### COMMAND WRITE

The TC58FVT400/B400 utilizes the JEDEC command control standard for a single power supply $E^2$PROM. A command is executed by inputting an address and data into the Command register. The command is entered by a $\overline{WE}$ Control Write ($\overline{WE}$ pulse with $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$) or a $\overline{CE}$ Control Write ($\overline{CE}$ pulse with $\overline{WE} = V_{IL}$ and $\overline{OE} = V_{IH}$). The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CE}$. The data is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$. I/O0 to 7 are valid for data input and I/O8 to 15 are ignored.

A command is when the Reset command is input. The device then enters Read Mode. When an undefined command is input, the Command register is reset and the device enters Read mode.

### RESET (Software Reset)

The device does not enter Read mode automatically when a command such as Auto Program / Erase or ID Read is not correctly executed (for example, if Program or Erase fails). The Reset or Read Command is necessary to return the device to Read mode. The Reset and Read commands must also be used to reset the Command register.

RESET (Hardware Reset)

A hardware reset is used for aborting Auto mode operations such as Auto Program/Erase and for resetting the operation mode. The device enters Read mode 20 $\mu$s after a 500-ns Low level input pulse to the $\overline{RESET}$ pin. Data may be corrupted if the device is reset during an Auto mode operation.

After a hardware reset the device enters Read mode when $\overline{RESET} = V_{IH}$ and Standby mode when $\overline{RESET} = V_{IL}$. The I/O pins are High-Impedance when $\overline{RESET} = V_{IL}$. The Read operation sequence and input of any command are allowed after the device enters Read mode.

ID READ MODE

The ID Read mode is used to establish the device type. The ID Read mode is set either from the Command mode by inputting a 90H command or from the EPROM mode by applying $V_{ID}$ to the A9 pin.

When A0, A1 and A6 = $V_{IL}$, the data that is read is the manufacturer code (0098H). When A0 = $V_{IH}$ and A1 and A6 = $V_{IL}$, the data that is read is the device code (TC58FVT400 = CDH / TC58FVTB400 = 4CH). The access time for an ID Read is the same as that of a normal Read operation. I/O8 to 15 are in High-Impedance state in Byte mode. A reset command is necessary to return the device to Read mode from command mode. And applying $V_{IH}$ to the A9 pin is necessary to return the device to Read mode from EPROM mode.

AUTO PROGRAM MODE

The TC58FVT400/B400 can be programmed in either byte or word units. The Auto Program mode is set using the Program command. The program address is latched on the falling edge of the $\overline{WE}$ signal and data is latched on the rising edge of the fourth bus cycle. Auto programming starts on the rising edge of the $\overline{WE}$ signal in the fourth bus cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is determined from the Hardware Sequence flag.

Programming of a protected block is ignored. The device enters Read mode 3 $\mu$s after the rising edge of the $\overline{WE}$ signal in the fourth bus cycle.

The device allows the programming of memory cells from 1 to 0. The programming of Memory cells from 0 to 1 will fail. A cell must be erased to turn it from 0 to 1.

If an Auto Program operation fails, the device remains in programming state and does not automatically return to Read mode. The device status can be determined from the setting of the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

If a programming operation fails, please do not try to use the block which contains the address to which data could not be programmed.

Auto Chip Erase Mode

The Auto Chip Erase mode is set using the Chip Erase command. The Auto Chip Erase operation starts on the rising edge of $\overline{WE}$ in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is determined from the Hardware Sequence flag.

Command inputs are ignored during an Auto Chip Erase. The hardware reset allows interruption of an Auto Chip Erase operation. The Auto Chip Erase operation does not complete correctly when interrupted. Hence a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 100 $\mu$s after the rising edge of the $\overline{WE}$ signal in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device remains in, erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

Auto Block / Multi Block Erase Mode

The Auto Block and Multi Block Erase modes are set using the Block Erase command. The block address is latched on the falling edge of the $\overline{WE}$ signal in the sixth bus cycle. The Block Erase starts as soon as the hold time has elapsed after the rising edge of the $\overline{WE}$ signal. All memory cells in the selected block are automatically programmed to 0, erased and verified as erased by the chip. The Multi Block Erase operation allows erasing of multiple blocks. Any additional block addresses or Multi Block Erase commands must be input within the Erase Hold Time - that is, within 50 $\mu$s of any $\overline{WE}$ signal rising edge. The device status can be determined from the setting of the Hardware Sequence flag.

Commands (except Erase Suspend) are ignored during a Block/Multi Block Erase operation. The operation can be aborted by a hardware reset. The Auto Erase operation does not complete correctly when aborted, therefore, a further Erase operation is necessary.

An attempt to erase a protected block is ignored. If all the selected blocks are protected, the Auto Erase operation is not executed and the device returns to Read mode 100 $\mu$s after the rising edge of the $\overline{WE}$ signal in the last bus cycle.

If an Auto Erase operation fails, the device remains in erasing state and does not return to Read mode. The device status is determined from the Hardware Sequence flag. Either a Reset command or a hardware reset is necessary to return the device to Read mode after a failure.

Erase Suspend / Resume Mode

The Erase Suspend mode is used to read data from a block not selected for erasing. The Erase Suspend command is allowed during a Block Erase operation or during the Block Erase Hold Time; it is ignored in other operation modes. A Block Erase operation is also suspended if the Suspend command is input during the Block Erase Hold Time. The device is reset if any command other than Suspend is input. The suspended device recognizes only Read and Resume commands.

The device enters Suspend mode 15 $\mu$s after the Erase Suspend command is input. The device then enters a pseudo-Read Mode. Data can be read out from an unselected block but is invalid if the address is set to a block selected for erasing. The device status can be determined from the Hardware Sequence flag. DQ6 (the toggle bit) stops toggling and RDY/$\overline{BSY}$ outputs 1 once the device is set to pseudo-Read mode. The host processor must track the current device mode since there is no way of telling whether the device is in pseudo-or ordinary Read mode. The device remains in pseudo-Read mode even if a Suspend command is input.

The device restarts the Block Erase operation after receiving a Resume command. The device returns to the status in which the Suspend command was input. The DQ6 output toggles and RDY/$\overline{BSY}$ outputs a 0.

BLOCK PROTECT

The TC58FVT400/B400 has a block protection feature to prevent programing and erasing of protected blocks. Block protection is enabled by either hardware protection (1) or a software command mode (2). The initial device is shipped with all blocks unprotected.

(1) A blocks is protected when: A9 = $\overline{OE}$ = $V_{ID}$, $\overline{CE}$ = $V_{IL}$, A0 / A6 = $V_{IL}$, A1 = $V_{IH}$; the block address is set using A12 to A17. The block protect data is programmed within $t_{PPLH}$ of the $\overline{WE}$ signal going Low.

(2) A block can also be protected using a software command. Block protection is executed by setting the $\overline{WE}$ signal to Low for $t_{PPLH}$ while $\overline{CE}$ = $V_{IL}$. After the command input in the sixth bus cycle A12 to A17 = the block address. Block protection can be verified using the Verify Block Protect command.

TEMPORARY BLOCK UNPROTECTION

The TC58FVT400/B400 has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying $V_{ID}$ to the $\overline{RESET}$ pin. In this state any block can be programmed or erased. The device returns to the previous condition after $V_{ID}$ is removed from the $\overline{RESET}$ pin. That is, previously protected blocks are protected again.

VERIFY BLOCK PROTECT

The Verify Block Protect command is used to check whether a block is protected or unprotected. Verify Block Protect is enabled either through hardware (1) or by a software command (2). In Word mode 0001H is output when the block is protected and 0000H is output when it is unprotected. DQ8 to 15 are High-Impedance in Byte mode.

(1) Verify Block Protection is enabled when: A9 = $V_{ID}$, A0 and A6 = $V_{IL}$ and A1 = $V_{IH}$.
A12 to A17 = the block address.

(2) Verify Block Protection can also be enabled using a software command.

## HARDWARE SEQUENCE FLAG

The TC58FVT400/B400 has a Hardware Sequence flag which allows the device status to be determined during Auto operation. The output data is read out with the same timing as Read mode at $\overline{CE} = \overline{OE} = V_{IL}$. RDY/$\overline{BSY}$ outputs either High or Low.

The device re-enters the Read mode automatically after Auto operation has completed successfully. The device status is read out from the Hardware Sequence flag and the operation result is verified by comparing the read-out data to the original data.

### DQ7 ($\overline{DATA}$ Polling)

The device status can be determined using the data polling function during an Auto Program or Auto Erase operation. $\overline{DATA}$ polling begins on the rising edge of $\overline{WE}$ in the last bus cycle. In an Auto Program operation, DQ7 outputs inverted data during the programming operation and outputs real data after programming has finished. In an Auto Erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto Program operation fails, DQ7 simply outputs the data.

The latched address is reset after an operation has finished. The polling data is asynchronous with the $\overline{OE}$ signal.

### DQ6 (Toggle Bit)

The device status can be determined by the Toggle Bit function during an Auto Program or Auto Erase operation. In an Auto Program operation the Toggle bit begins toggling on the rising edge of $\overline{WE}$ in the last bus cycle. In an Auto Erase operation The Toggle bit begins toggling as soon as the Erase Hold Time has elapsed after the rising edge of the $\overline{WE}$ signal in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each attempt ($\overline{OE}$ access) while $\overline{CE} = V_{IL}$ while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation failed, the DQ6 output toggles.

DQ6 toggles for around 3 $\mu$s when an attempt is made to execute an Auto Program operation on a protected block. It then stops toggling. DQ6 toggles for around 100 $\mu$s when an attempt is made to execute an Auto Erase operation on a protected block. It then stops toggling. After toggling stops the device returns to Read mode.

### DQ5 (Internal Time-out)

DQ5 outputs a 1 when the Internal Timer has timed out during a Program or Erase operation. This indicates that the operation has not completed within the allotted time.

An attempt to program 1 into a cell containing 0 will fail (see Auto Program mode). DQ5 outputs 1 in this case. Either a hardware reset or a software Reset command is required to put the device into Read mode.

DQ3 (Block Erase Timer)

The Block Erase operation starts 50 μs (Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle. DQ3 outputs a 0 during the Block Erase Hold Time and a 1 when the Erase operation starts. Additional Block Erase commands can only be accepted during this Block Erase Hold Time. Each Block Erase command received within this hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

RDY/$\overline{BSY}$ (READY/$\overline{BUSY}$)

TC58FVT400/B400 has a RDY/$\overline{BSY}$ signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto Program or Auto Erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can accept a new command. The RDY/$\overline{BSY}$ signal outputs a 0 when an operation has failed.

The RDY/$\overline{BSY}$ signal outputs a 0 after the rising edge of $\overline{WE}$ in the last command cycle of a Program operation and during the Erase Hold Time after the last command cycle of an Erase operation.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. The RDY/$\overline{BSY}$ signal outputs a 1 during an Erase Suspend operation. The output buffer for the RDY/$\overline{BSY}$ pin is an open drain type circuit, allowing a wired–OR connection. A pull-up resistor needs to be inserted between $V_{DD}$ and the RDY/$\overline{BSY}$ pin.

## DATA PROTECTION

The TC58FVT400/B400 utilizes a JEDEC standard command sequence which protects data against accidental alteration due to noise.

$V_{DD}$ Lock-out Voltage

The device is reset when $V_{DD}$ is less than $V_{LKO}$ to protect memory cell data against $V_{DD}$ noise, and during power-up and power-down. An Auto Program or Erase operation stops when $V_{DD}$ drops below $V_{LKO}$. An Erase Suspend operation is reset and an Erase operation stops if the device is in Suspend mode. An operation will not complete correctly if it is interrupted by $V_{DD}$ Lock-out.

$\overline{WE}$ Glitch Pulses

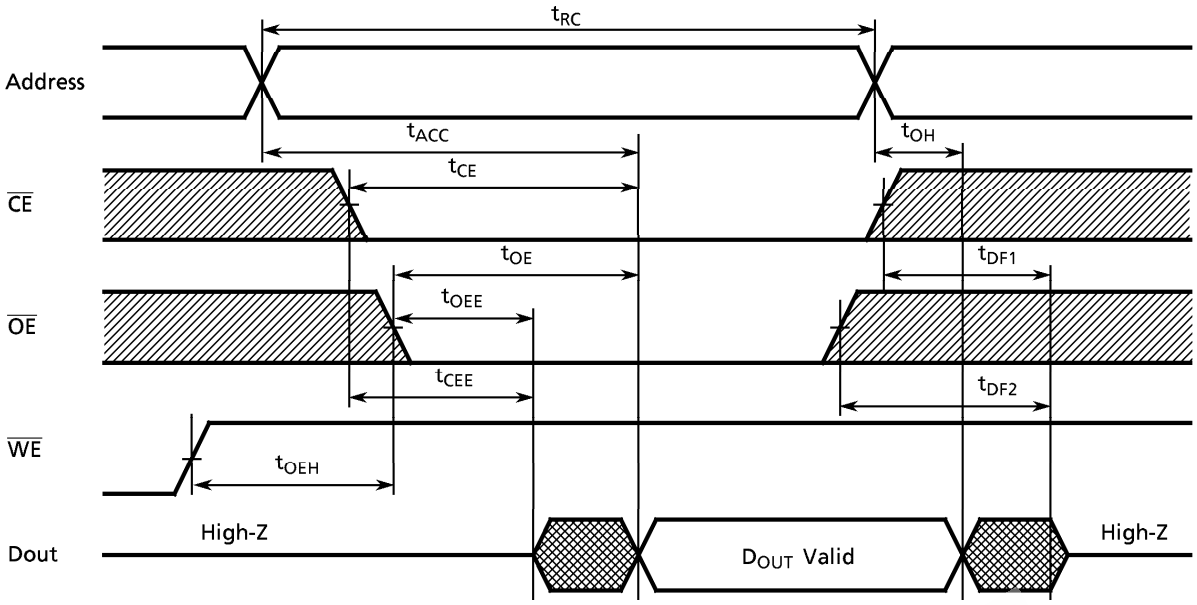
Glitches must be suppressed (to less than 5 ns) in order for operation to proceed smoothly.

Protection at Power-on

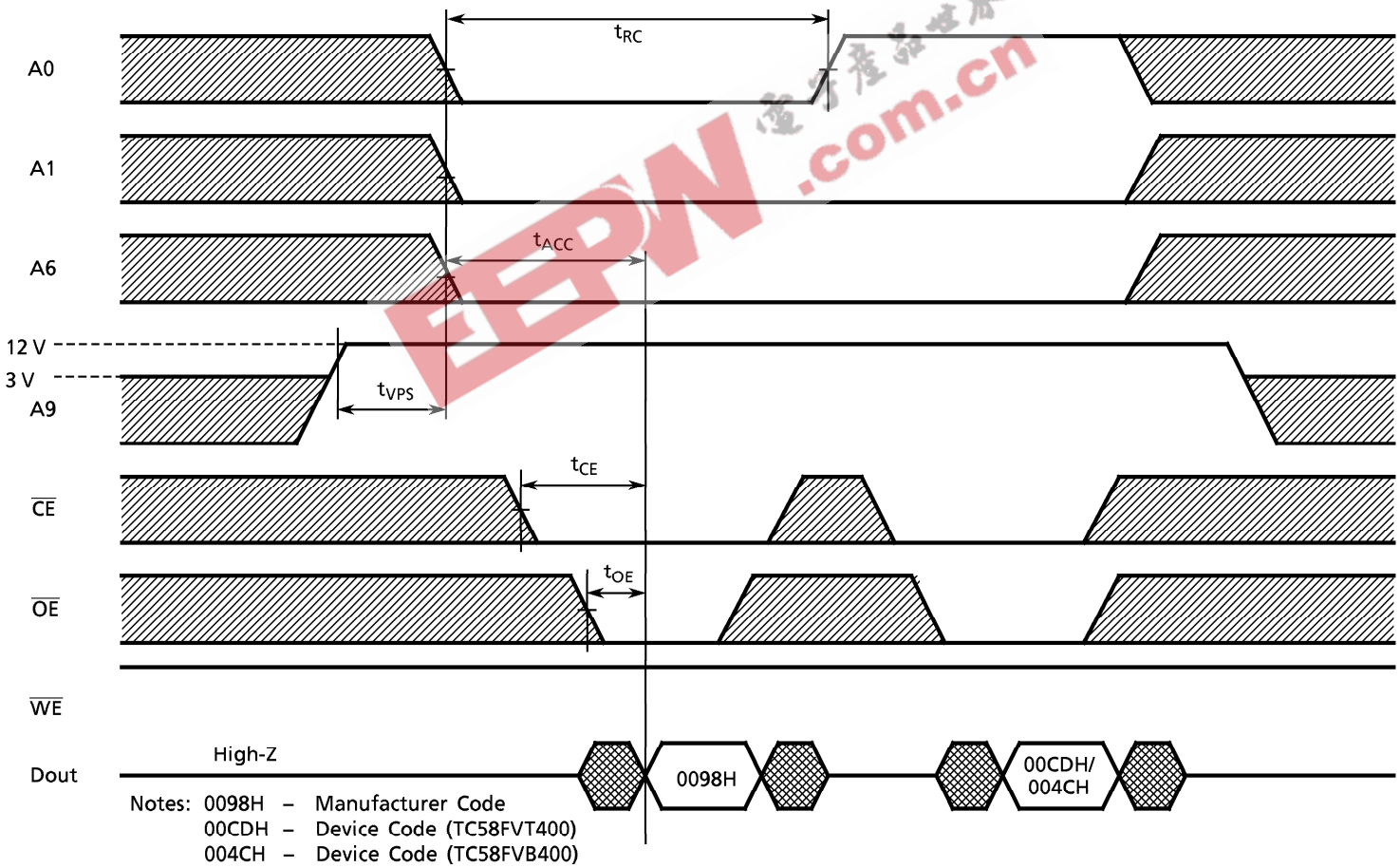
A command is not recognized on the rising edge of $\overline{WE}$ if $V_{DD}$ rises from 0 V to the operating voltage while $\overline{WE} = V_{IL}$, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$. In this case the device is reset and enters Read mode.

## TIMING DIAGRAMS

### Read / ID Read Operation

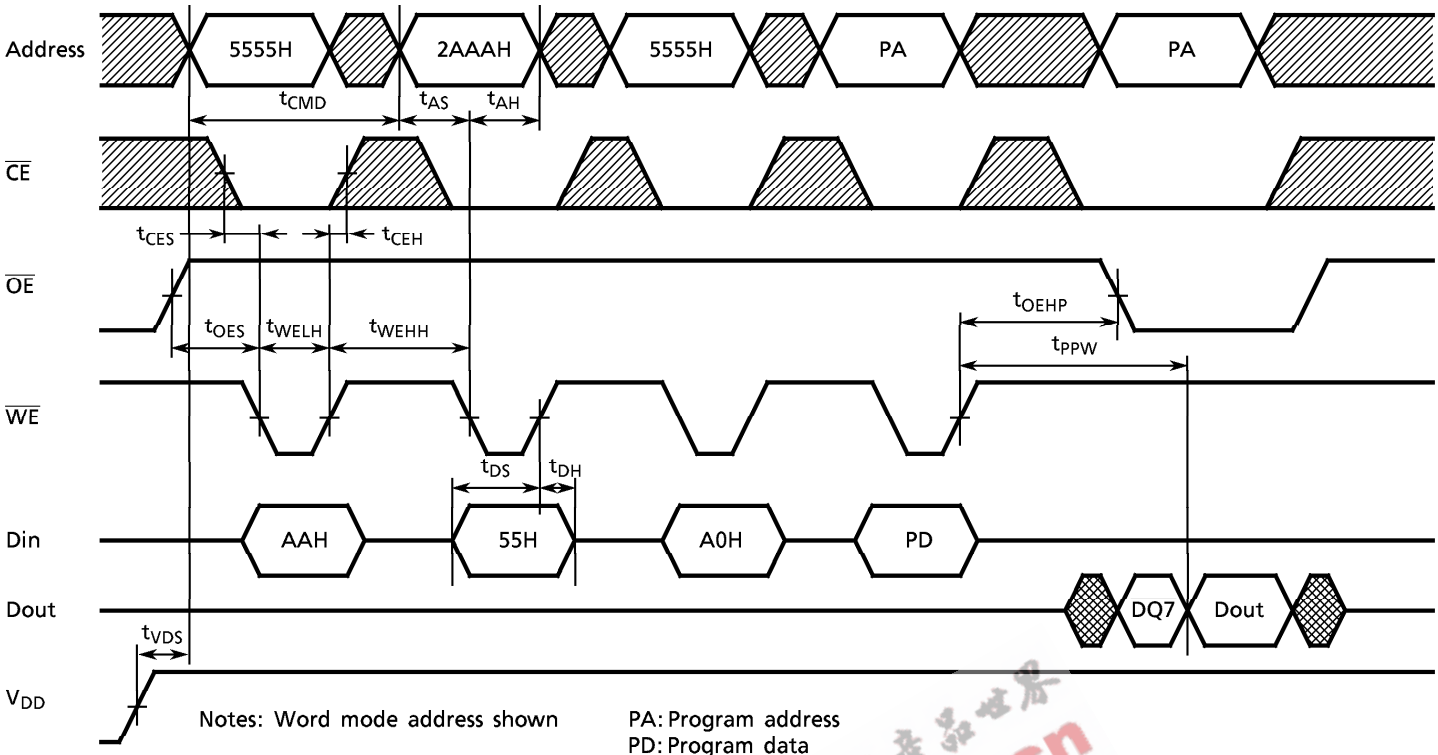



### ID Read Operation (Hardware)




Notes: 0098H – Manufacturer Code
00CDH – Device Code (TC58FVT400)
004CH – Device Code (TC58FVB400)

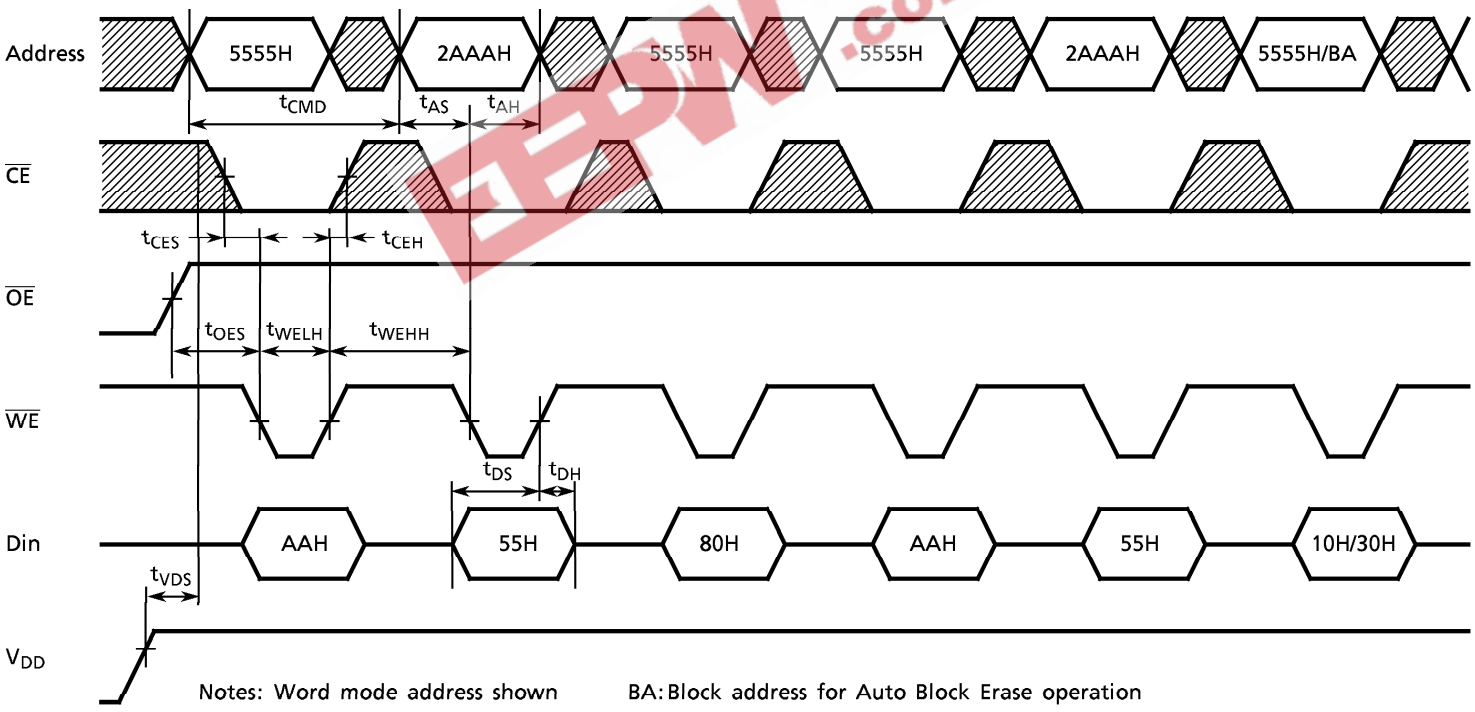
## Auto Program Operation ($\overline{WE}$ Control)




Notes: Word mode address shown

PA: Program address
PD: Program data

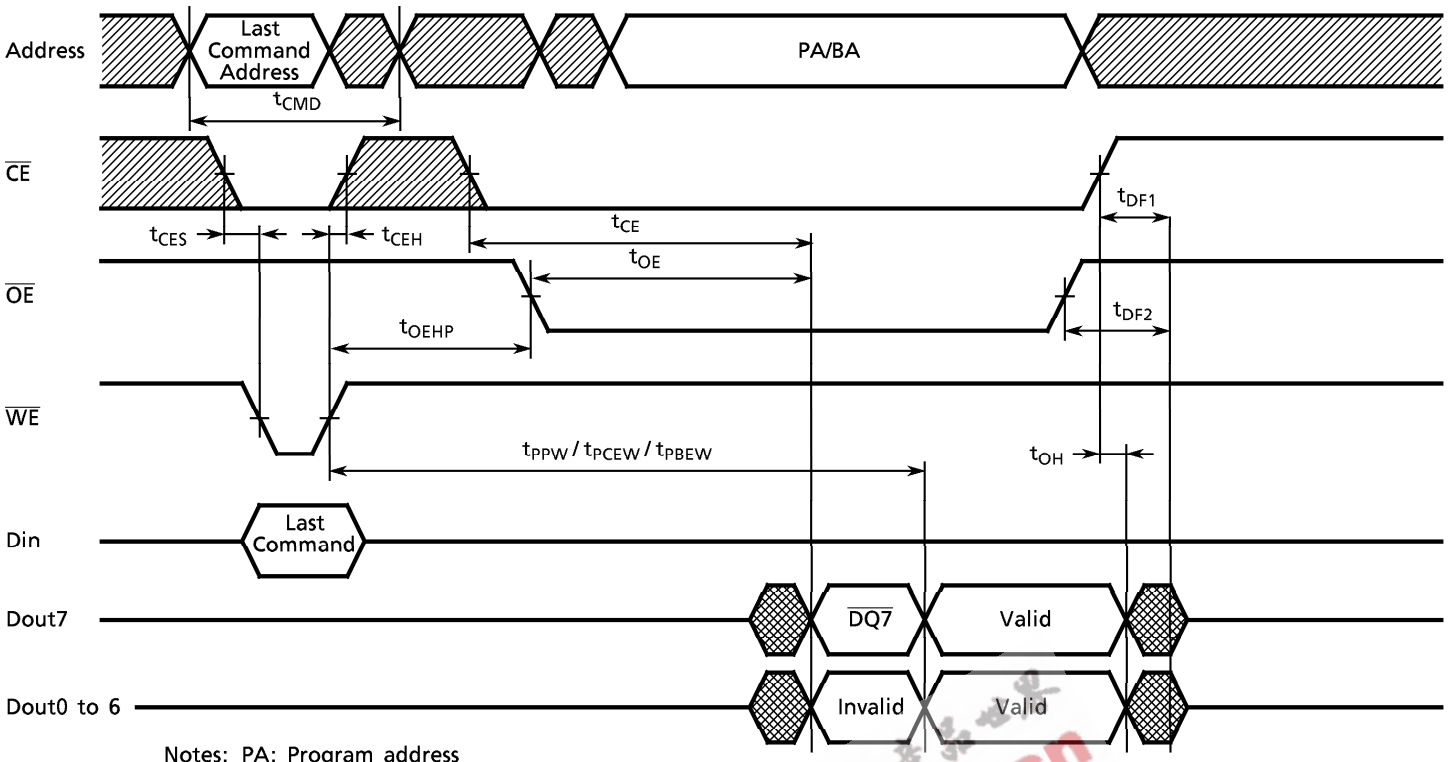
## Auto Chip Erase / Auto Block Erase Operation ($\overline{WE}$ Control)




Notes: Word mode address shown

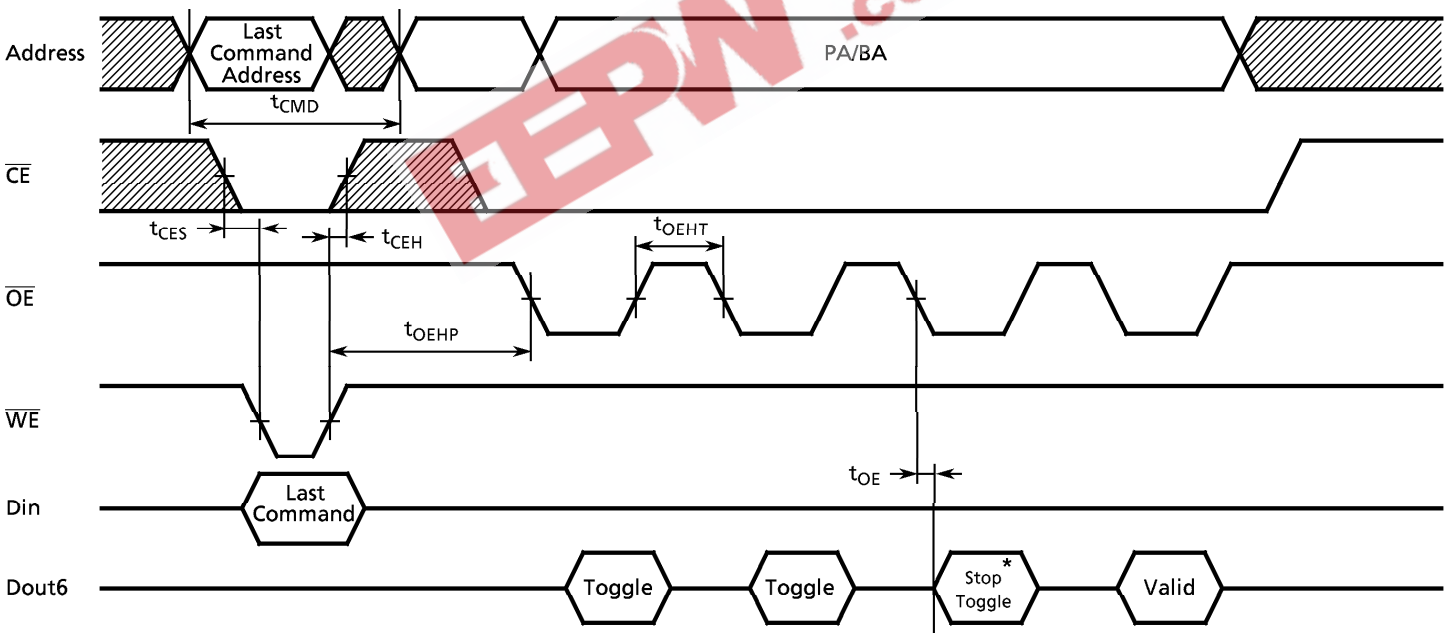
BA: Block address for Auto Block Erase operation

## $\overline{\text{DATA}}$ Polling during Program/Erase Operation




Notes: PA: Program address
BA: Block address

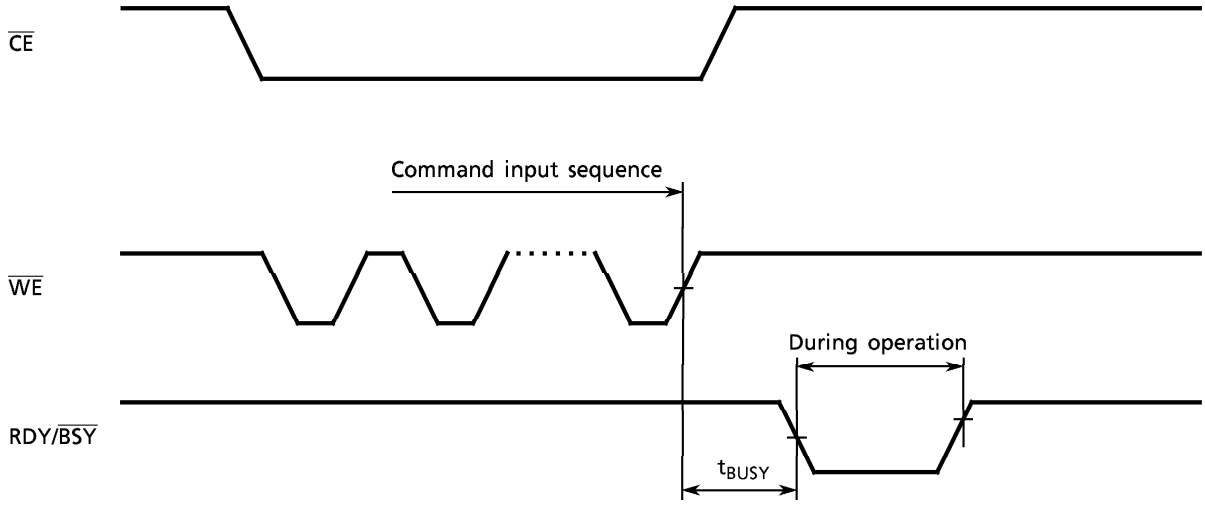
## Toggle Bit during Program/Erase Operation



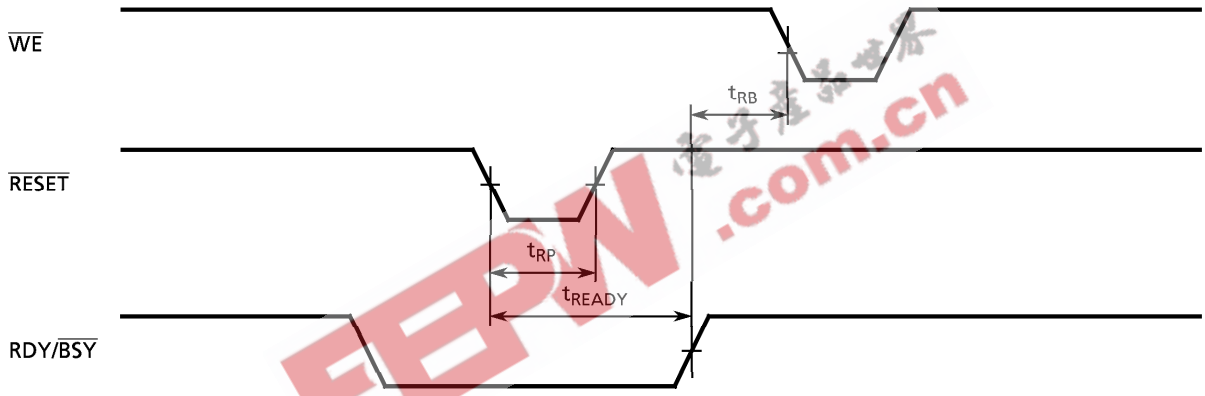

* Dout6 stops toggling when the last command has completed.

Notes: PA: Program address
BA: Block address

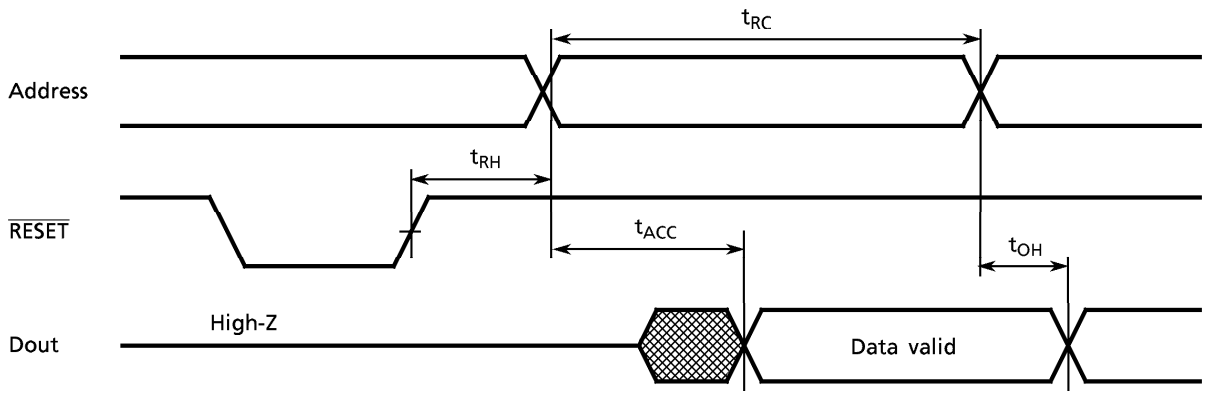
RDY/$\overline{BSY}$ during Auto Program/Erase Operation



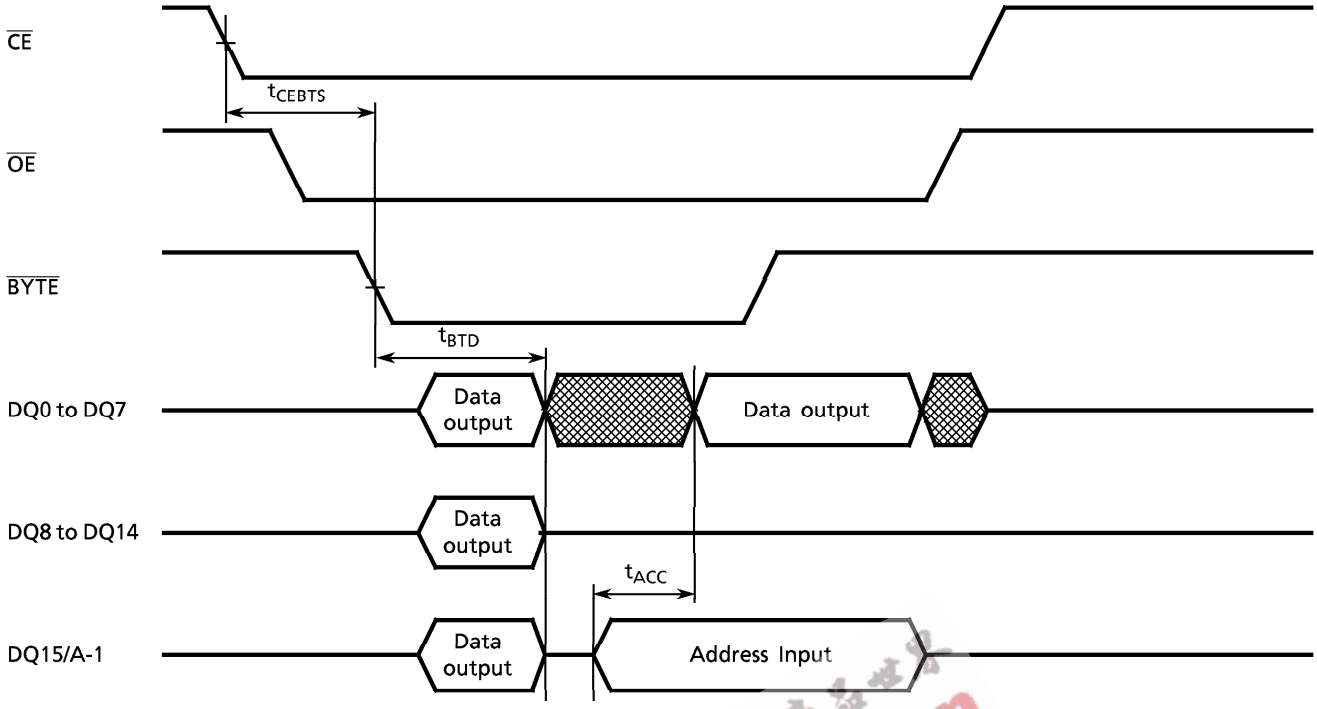

Hardware Reset Operation



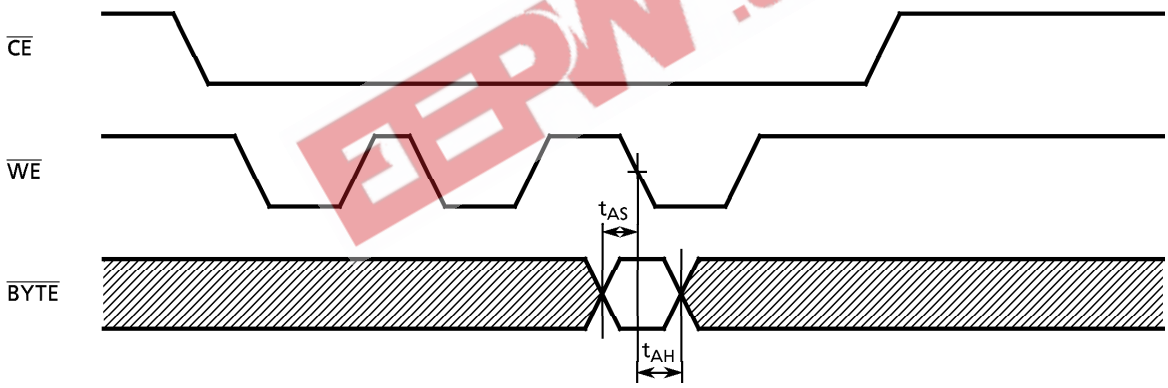

Read after $\overline{RESET}$



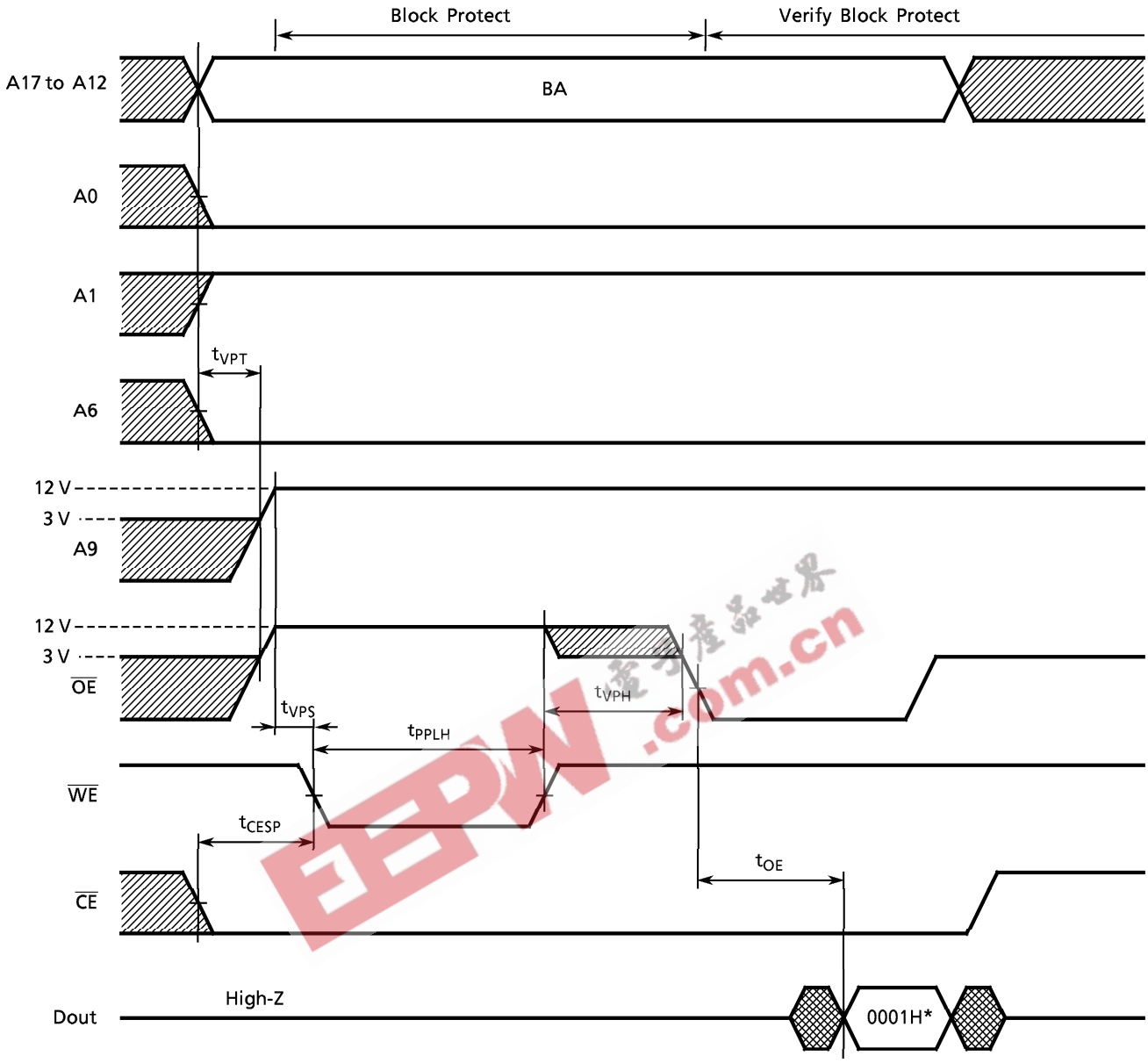
## $\overline{\text{BYTE}}$ during Read Operation




## $\overline{\text{BYTE}}$ during Write Operation



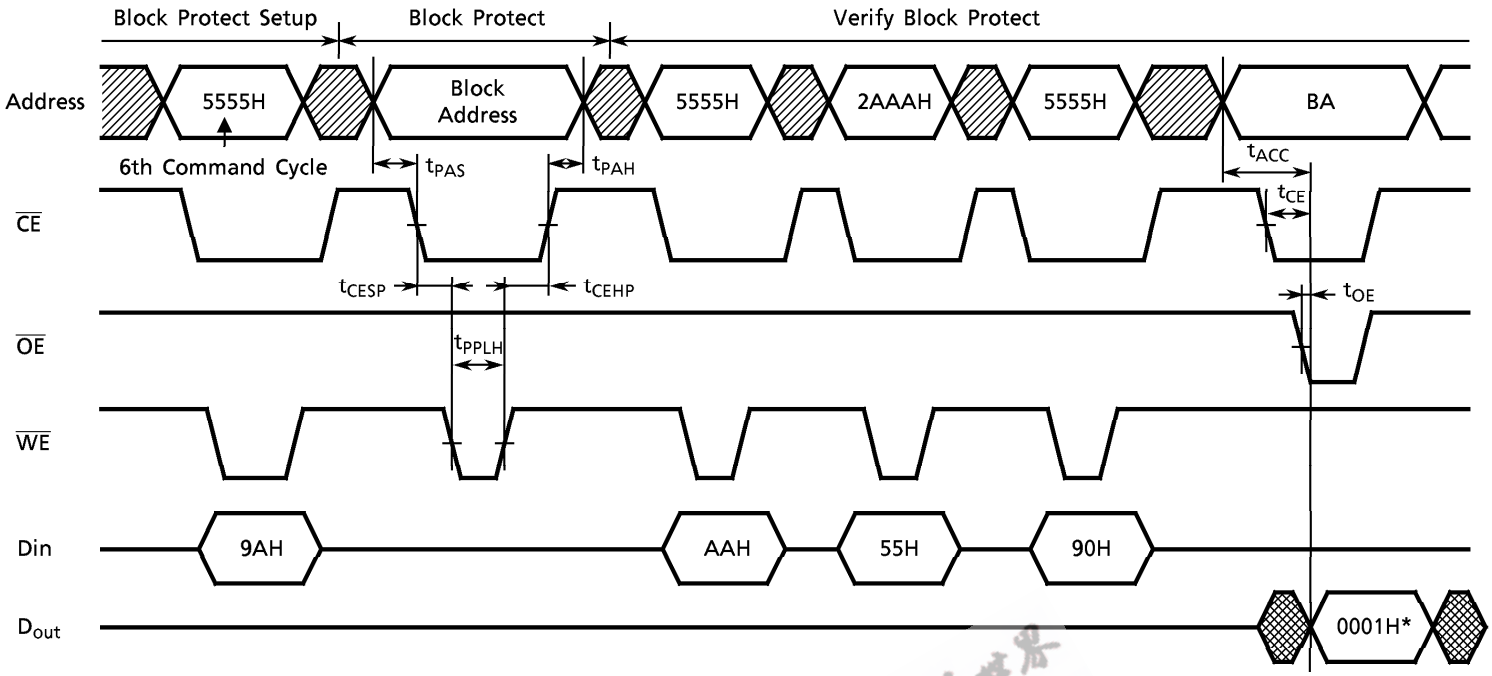
Block Protect Operation (Hardware)




BA: Block address

* : 0001H indicates that block is protected.

Block Protect (Software)

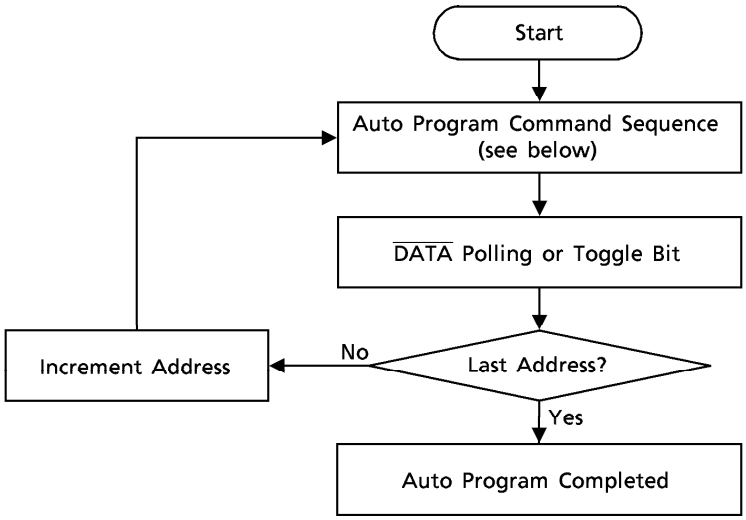



BA : Block address

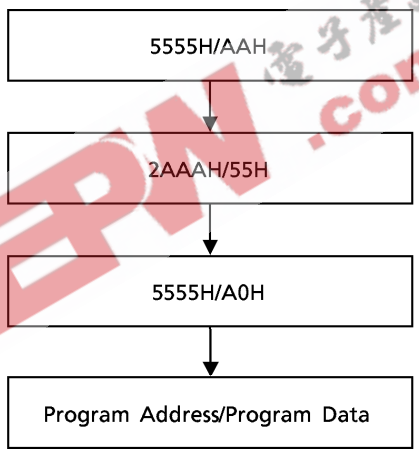
* : 0001H indicates that block is protected.

## FLOWCHARTS

### Auto Program

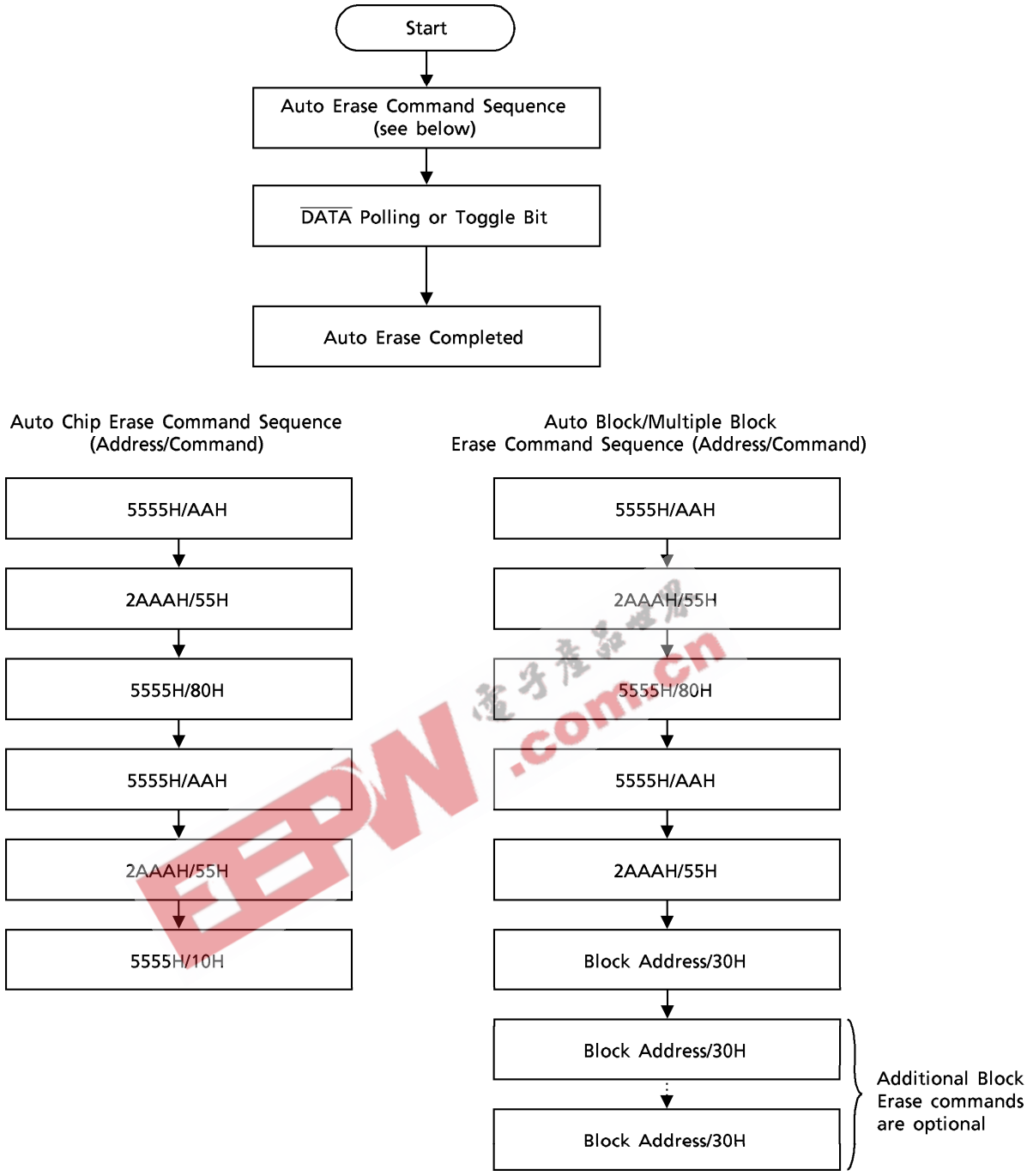



Auto Program Command Sequence (Address/Command)



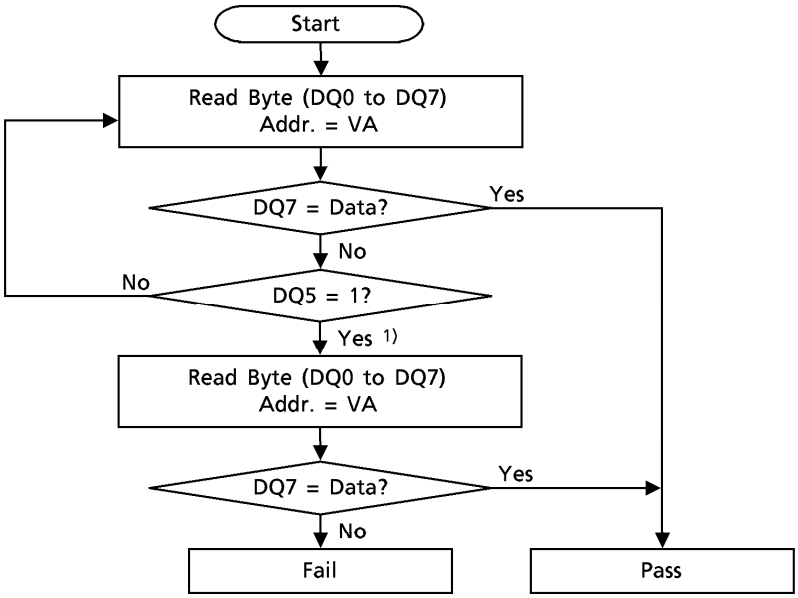

Note: Word mode command sequence is shown.

Auto Erase




Note: Word mode command sequence is shown.

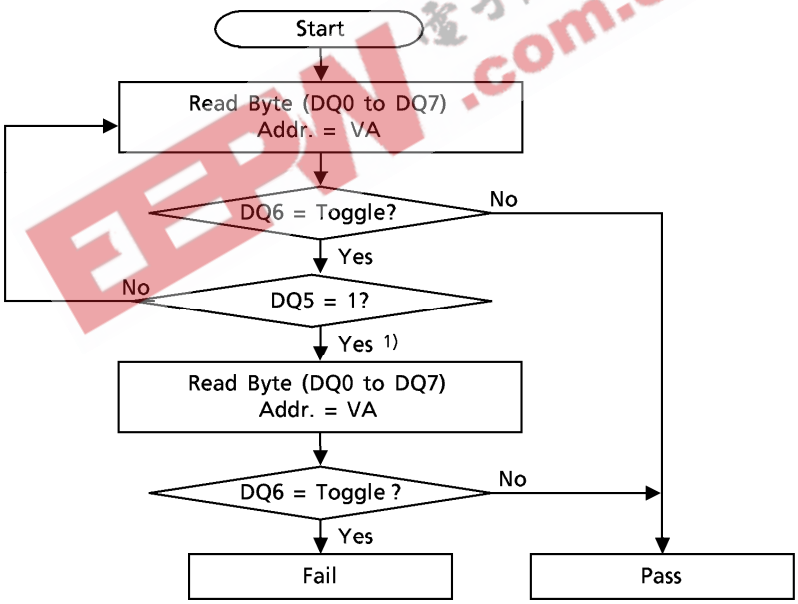
## DQ7 $\overline{\text{DATA}}$ Polling




VA: Byte address for programming.
Any of the addresses within the block being erased during a Block Erase operation.
Don't care during a Chip Erase operation

Note: 1) DQ7 must be rechecked even if DQ5 = 1 because DQ7 may change at the same time as DQ5.

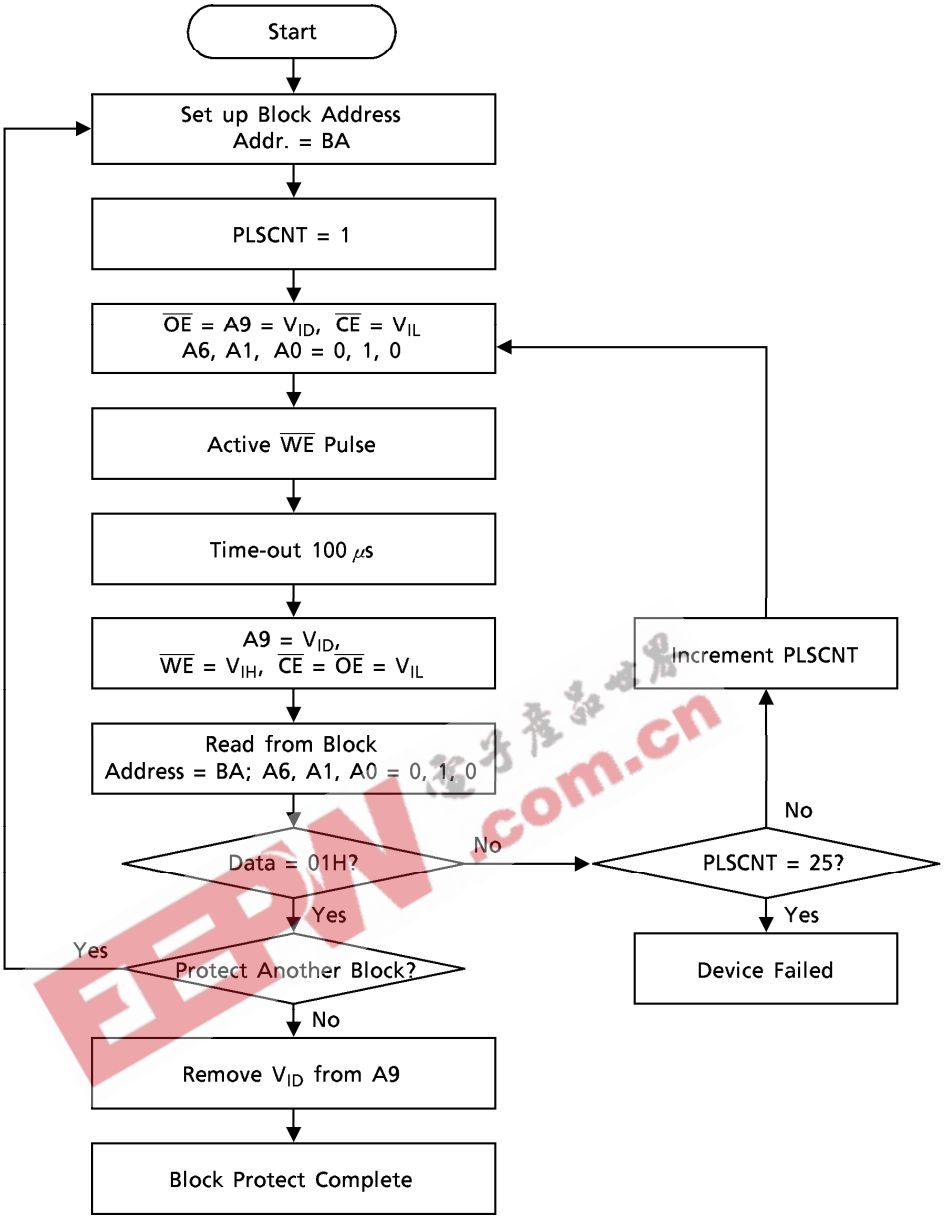
## DQ6 Toggle Bit




VA: Byte address for programming.
Any of the addresses within the block being erased during a Block Erase operation.
Don't care during a Chip Erase operation
Any address not within the current block during an Erase Suspend operation

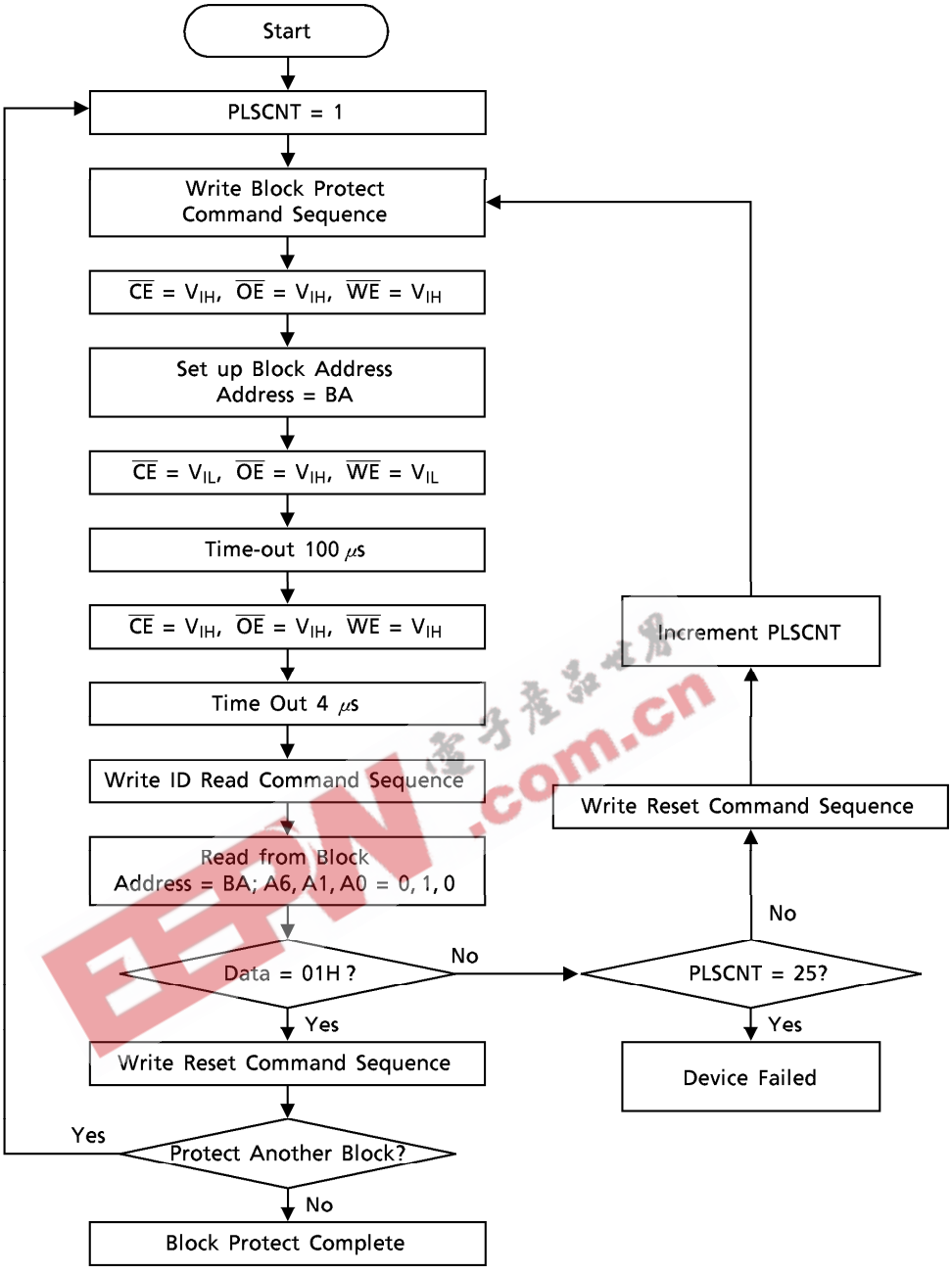
Note: 1) DQ6 must be rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time that DQ5 changes to 1.

Block Protect (Hardware)




BA: Block address

Block Protect (Software)



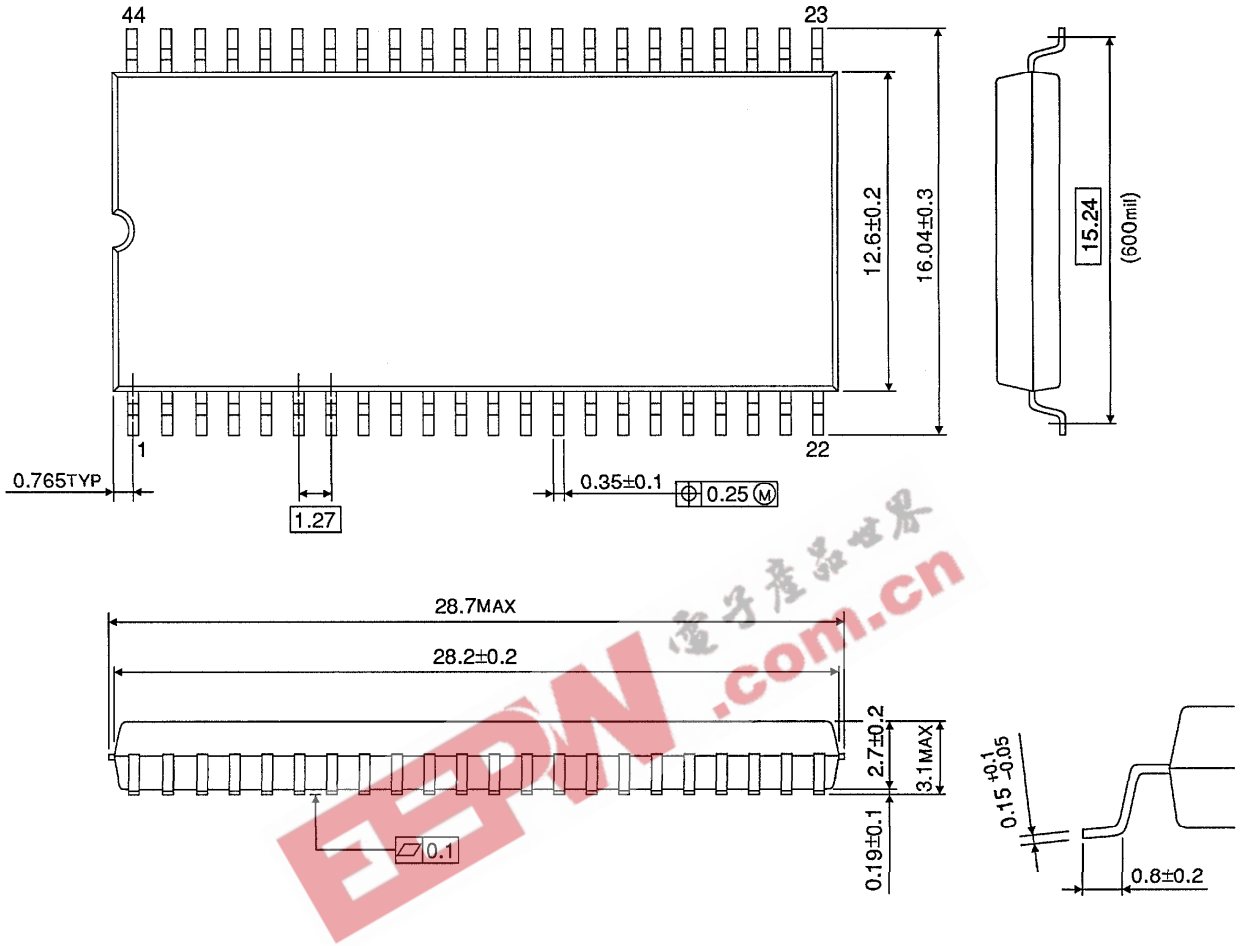

BA: Block Address

## PACKAGE DIMENSIONS

- Plastic SOP

  SOP44－P－600－1.27

Unit: mm



## PACKAGE DIMENSIONS

- Plastic TSOP

TSOP I 48 – P – 1220 – 0.50

Unit: mm