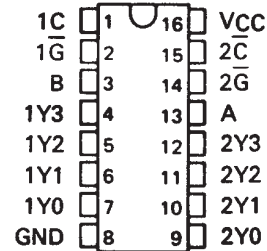


SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

SDLS057 – MARCH 1974 – REVISED MARCH 1988

- **Applications:**
 - Dual 2-to 4-Line Decoder
 - Dual 1-to 4-Line Demultiplexer
 - 3-to 8-Line Decoder
 - 1-to 8-Line Demultiplexer
- **Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words**
- **Input Clamping Diodes Simplify System Design**
- **Choice of Outputs:**
 - Totem Pole ('155, 'LS155A)
 - Open-Collector ('156, 'LS156)

SN54155, SN54156, SN54LS155A,
SN54LS156 . . . J OR W PACKAGE
SN74155, SN74156 . . . N PACKAGE
SN74LS155A, SN74LS156 . . . D OR N PACKAGE
(TOP VIEW)

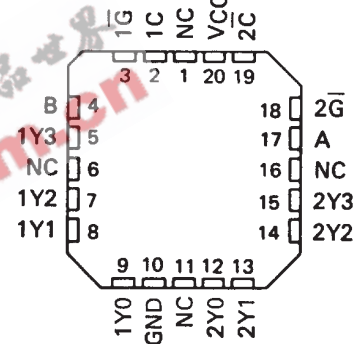


TYPES	TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS	TYPICAL POWER DISSIPATION
'155, '156	21 ns	125 mW
'LS155A	18 ns	31 mW
'LS156	32 ns	31 mW

description

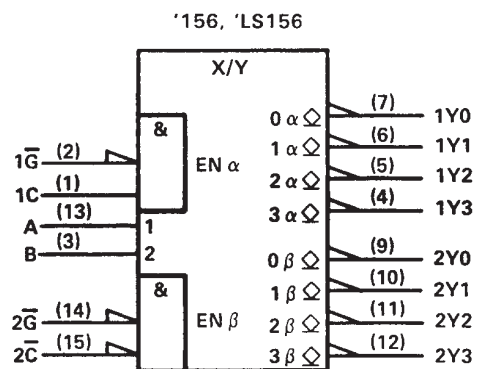
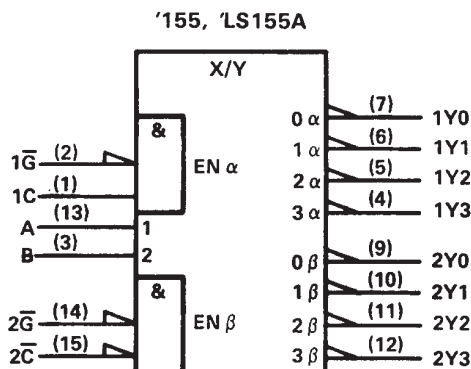
These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

SN54LS155A, SN54LS156 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbols (2-line to 4-line decoder)[†]



[†]These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. For alternative symbols for other applications, see the following page.

Pin numbers shown are for D, J, N, and W packages.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

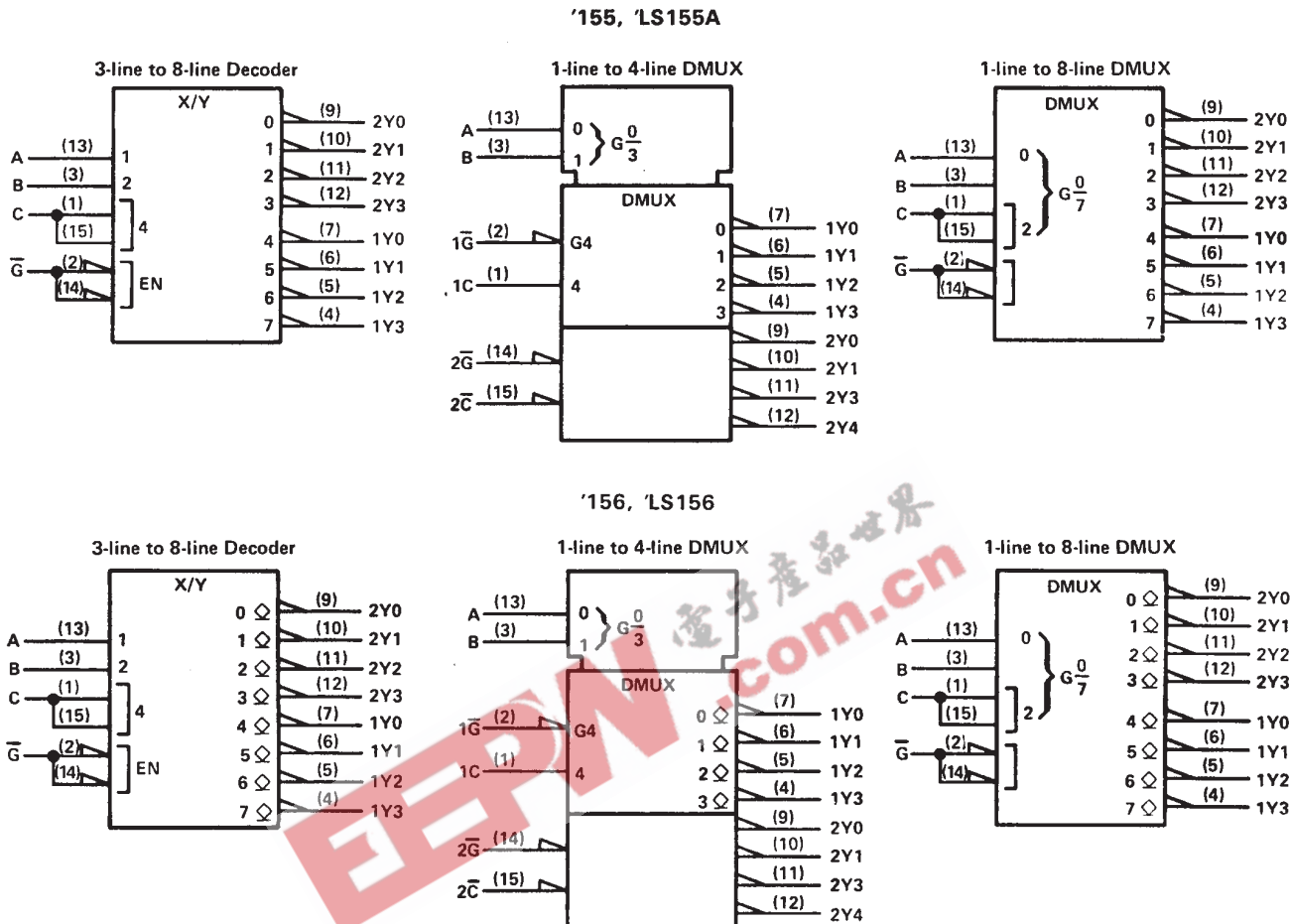
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SN54155, SN54156, SN54LS155A, SN54LS156, SN74155, SN74156, SN74LS155A, SN74LS156 DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

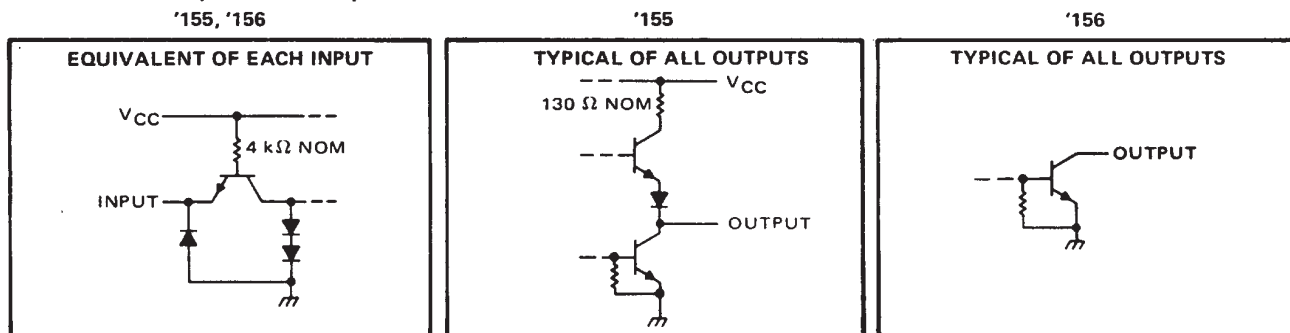
SDLS057 – MARCH 1974 – REVISED MARCH 1988

additional logic symbols (alternatives)[†]



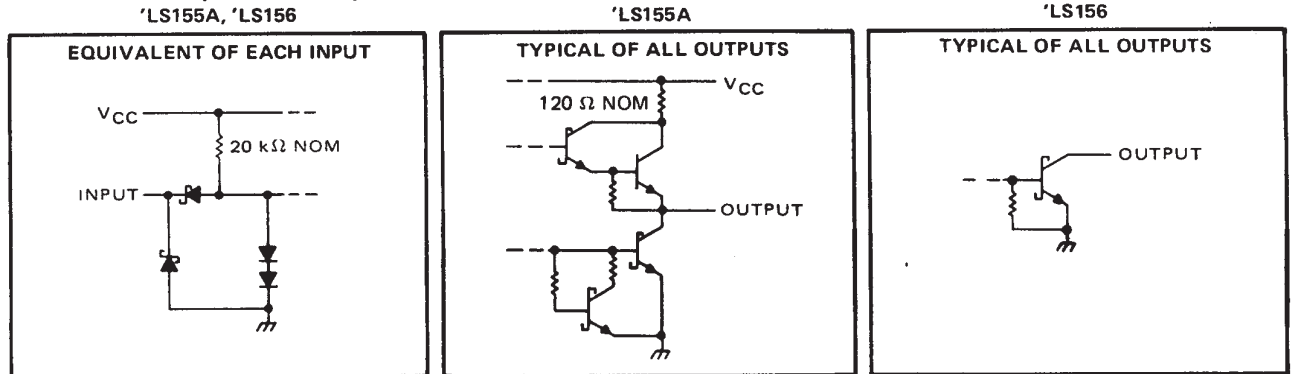
[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

schematics of inputs and outputs

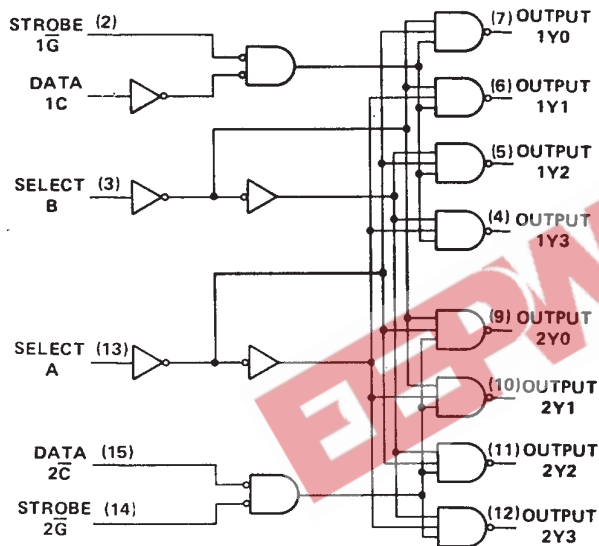


SN54155, SN54156, SN54LS155A, SN54LS156,
SN74155, SN74156, SN74LS155A, SN74LS156
DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS
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schematics of inputs and outputs (continued)



logic diagram (positive logic)



FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

SELECT		STROBE	DATA	OUTPUTS			
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

SELECT		STROBE	DATA	OUTPUTS			
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

SELECT		STROBE OR DATA	OUTPUTS							
C†	B A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X X	H	H	H	H	H	H	H	H	H
L	L L	L	L	H	H	H	H	H	H	H
L	L H	L	H	L	H	H	H	H	H	H
L	H L	L	H	H	L	H	H	H	H	H
L	H H	L	H	H	H	L	H	H	H	H
H	L L	L	H	H	H	H	L	H	H	H
H	L H	L	H	H	H	H	H	L	H	H
H	H L	L	H	H	H	H	H	H	L	H
H	H H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant

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Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage: '155, '156	5.5 V
'LS155A, 'LS156	7 V
Off-state output voltage: '156	5.5 V
'LS156	7 V
Operating free-air temperature range: SN54', SN54LS' Circuits	-55°C to 125°C
SN74', SN74LS' Circuits	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

PARAMETER	TEST CONDITIONS†	SN54155 SN74155		UNIT	
		MIN	TYP‡	MAX	
V _{IH} High-level input voltage		2			V
V _{IL} Low-level input voltage				0.8	V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = -8 mA			-1.5	V
V _{OH} High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OH} = -800 µA	2.4	3.4		V
V _{OL} Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 16 mA		0.2	0.4	V
I _I Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1	mA
I _{IH} High-level input current	V _{CC} = MAX, V _I = 2.4 V			40	µA
I _{IL} Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1.6	mA
I _{OS} Short-circuit output current§	V _{CC} = MAX	SN54155	-20	-55	mA
		SN74155	-18	-57	
I _{CC} Supply current	V _{CC} = MAX, See Note 2	SN54155	25	35	mA
		SN74155	25	40	

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54155 SN74155			UNIT
					MIN	TYP	MAX	
t _{PLH}	A, B, 2C̄, 1Ḡ, or 2Ḡ	Y	2	C _L = 15 pF, R _L = 400 Ω, See Note 3		13	20	ns
t _{PHL}	A, B, 2C̄, 1Ḡ, or 2Ḡ	Y	2			18	27	ns
t _{PLH}	A or B	y	3			21	32	ns
t _{PHL}	A or B	Y	3			21	32	ns
t _{PLH}	1C	Y	3			16	24	ns
t _{PHL}	1C	Y	3			20	30	ns



**TEXAS
INSTRUMENTS**

SN54155A, SN74155A

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54156 SN74156			UNIT
		MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2		V
V_{IL} Low-level input voltage				0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -8 \text{ mA}$			-1.5	V
I_{OH} High-level output current	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$			250	µA
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40	µA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	SN54156		25	35
		SN74156		25	40

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54156 SN74156			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$	Y	2	$C_L = 15 \text{ pF},$ $R_L = 400 \Omega,$ See Note 3		15	23	ns
t_{PHL}	A, B, $2\overline{C}$, $1\overline{G}$, or $2\overline{G}$	Y	2			20	30	ns
t_{PLH}	A or B	Y	3			23	34	ns
t_{PHL}	A or B	Y	3			23	34	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			22	33	ns

§ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54LS155A, SN74LS155A

DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions

	SN54LS155A			SN74LS155A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	–55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS155A			SN74LS155A			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$							V
	$I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	
	$I_{OL} = 8 \text{ mA}$					0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			–0.4			–0.4	mA
I_{OS} Short-circuit output current§	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		6.1	10		6.1	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS155A SN74LS155A			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, $2\bar{C}$, $1\bar{G}$, or $2\bar{G}$	Y	2	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Note 3	10	15		ns
t_{PHL}	A, B, $2\bar{C}$, $1\bar{G}$, or $2\bar{G}$	Y	2		19	30		ns
t_{PLH}	A or B	Y	3		17	26		ns
t_{PHL}	A or B	Y	3		19	30		ns
t_{PLH}	1C	Y	3		18	27		ns
t_{PHL}	1C	Y	3		18	27		ns

¶ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN54LS156A, SN74LS156A DUAL 2-LINE TO 4-LINE DECODERS/DEMULTIPLEXERS

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recommended operating conditions

	SN54LS156			SN74LS156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS156		SN74LS156		UNIT
				MIN	TYP‡	MAX	MIN	
V _{IH}	High-level input voltage			2			2	V
V _{IL}	Low-level input voltage					0.7		0.8
V _{IK}	Input clamp voltage	V _{CC} = MIN, I _I = −18 mA				−1.5		−1.5
I _{OH}	High-level output current	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max, V _{OH} = 5.5 V				100		100
V _{OL}	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = V _{IL} max	I _{OL} = 4 mA	0.25	0.4	0.25	0.4	V
			I _{OL} = 8 mA			0.35	0.5	
I _I	Input current at maximum input voltage	V _{CC} = MAX, V _I = 7 V				0.1		0.1
I _{IH}	High-level input current	V _{CC} = MAX, V _I = 2.7 V				20		20
I _{IL}	Low-level input current	V _{CC} = MAX, V _I = 0.4 V				−0.4		−0.4
I _{CC}	Supply current	V _{CC} = MAX, See Note 2				6.1	10	6.1

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS156 SN74LS156			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C 1G, or 2G	Y	2	$C_L = 15 \text{ pF}$, $R_L = 2 \text{ k}\Omega$, See Note 3	25	40		ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2		34	51		ns
t_{PLH}	A or B	Y	3		31	46		ns
t_{PHL}	A or B	Y	3		34	51		ns
t_{PLH}	1C	Y	3		32	48		ns
t_{PHL}	1C	Y	3		32	48		ns

§ t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9750801Q2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-9750801QEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9750801QEA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9750801QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
5962-9750801QFA	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SN54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS156J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN54LS156J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SN74155N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74155N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74155N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74155N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74156N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74156N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS155AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155AD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ADRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS155AN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS155ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS155ANE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS155ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ANSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS155ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LS155ANSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS156N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS156N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS156N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS156NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS156NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54155J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ54155W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54155W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI
SNJ54LS155AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS155AFK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS155AJ	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS155AW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS155AW	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS156FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS156FK	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI
SNJ54LS156J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS156J	ACTIVE	CDIP	J	16	1	TBD	Call TI	Level-NC-NC-NC
SNJ54LS156W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SNJ54LS156W	ACTIVE	CFP	W	16	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

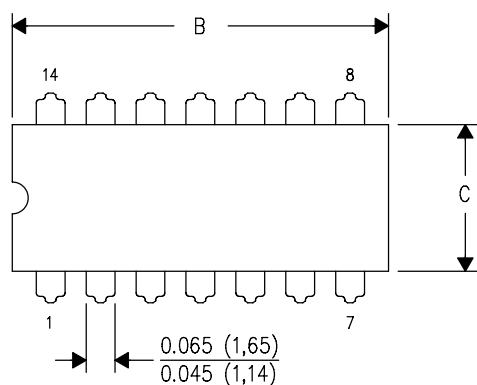
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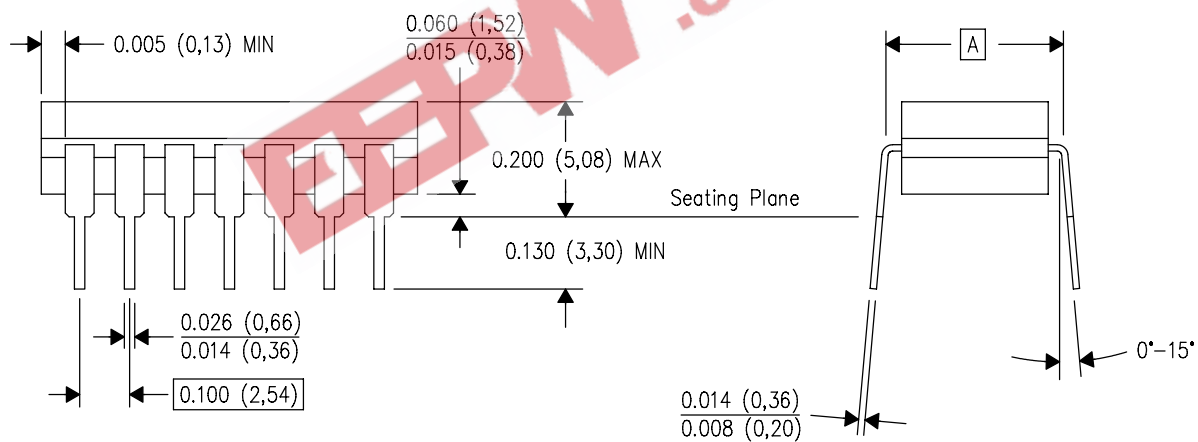
J (R—GDIP—T**) (R—GDIP—T**)

14 LEADS SHOWN

CERAMIC DUAL IN—LINE PACKAGE



PINS **	14	16	18	20
DIM				
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



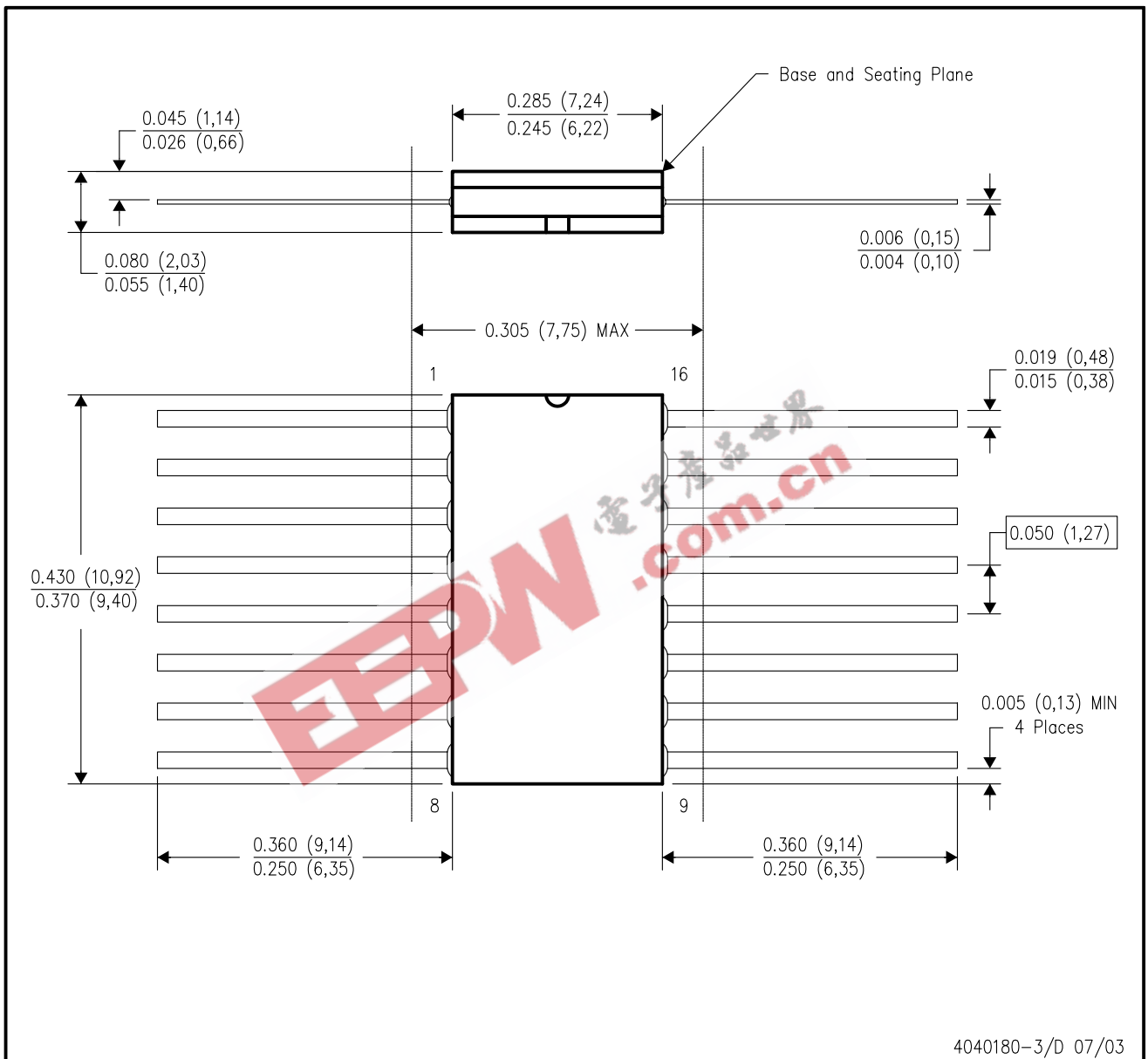
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

MECHANICAL DATA

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only.
 - Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

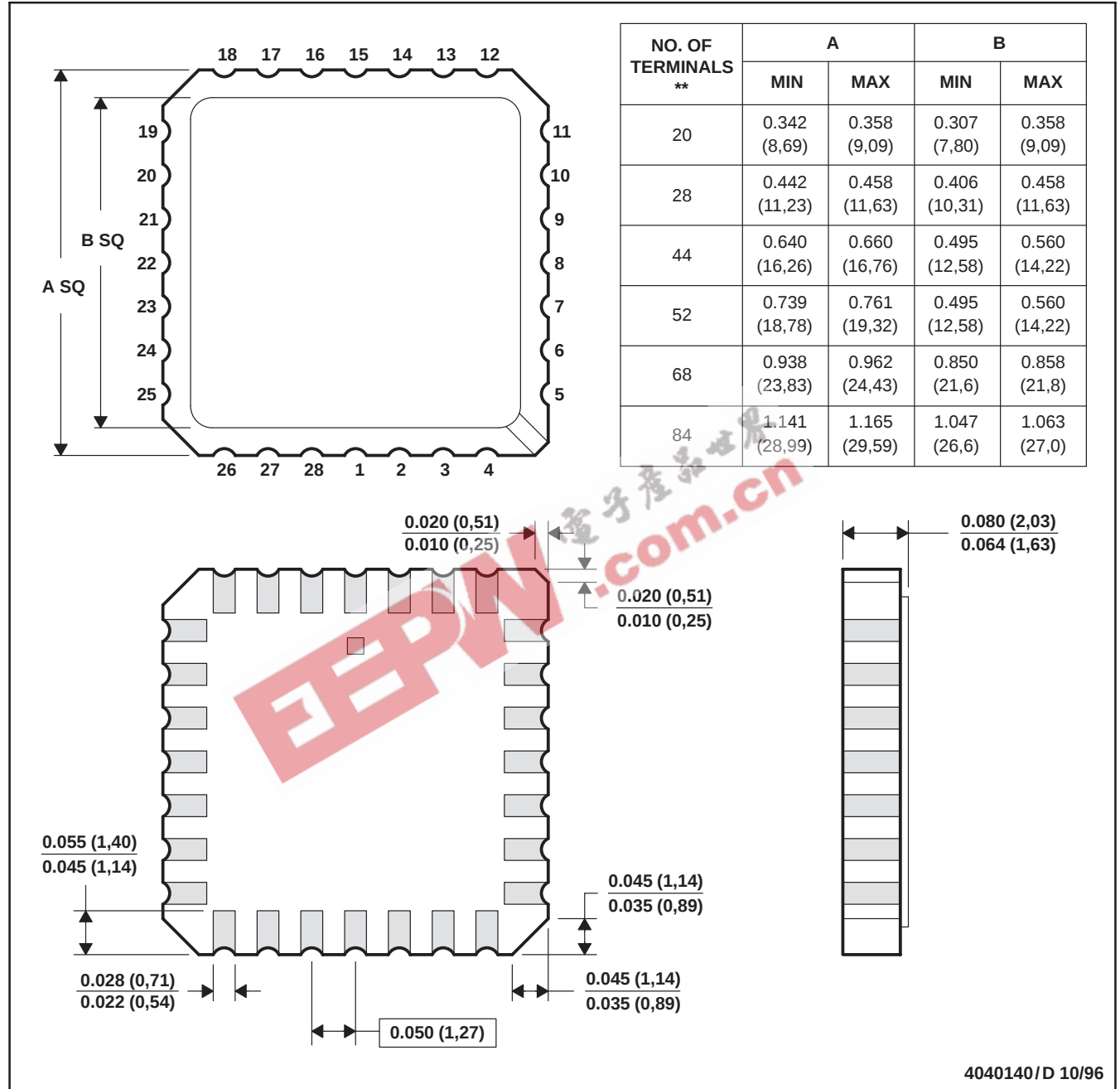
MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



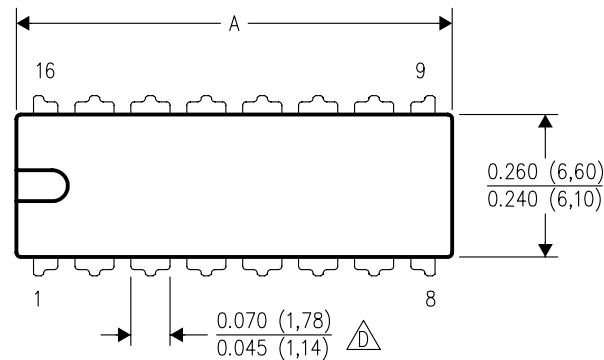
- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals are gold plated.
 - Falls within JEDEC MS-004

MECHANICAL DATA

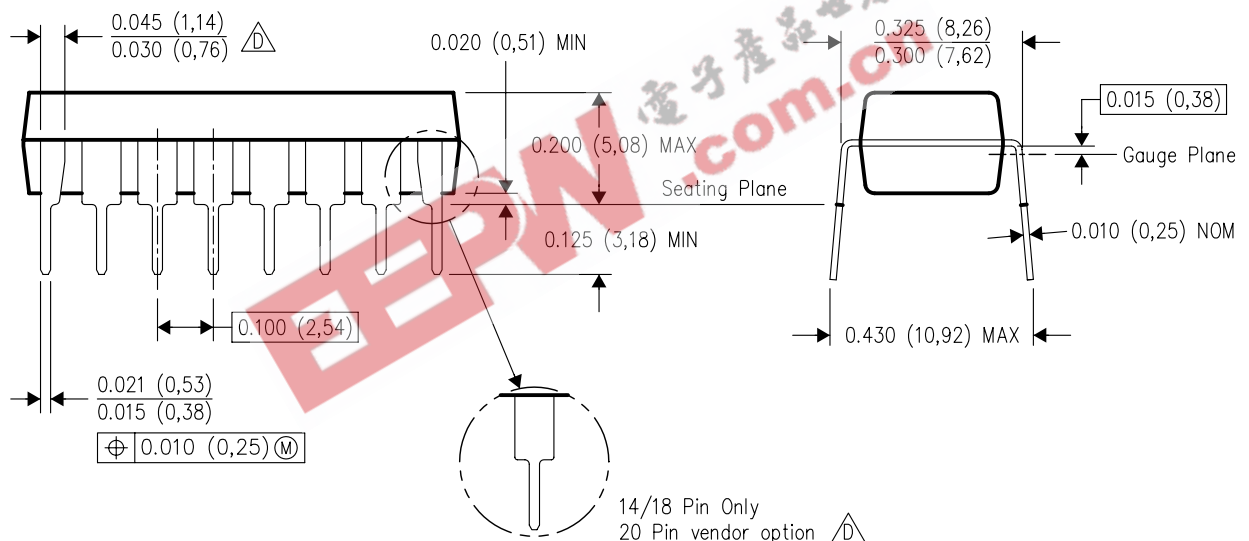
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



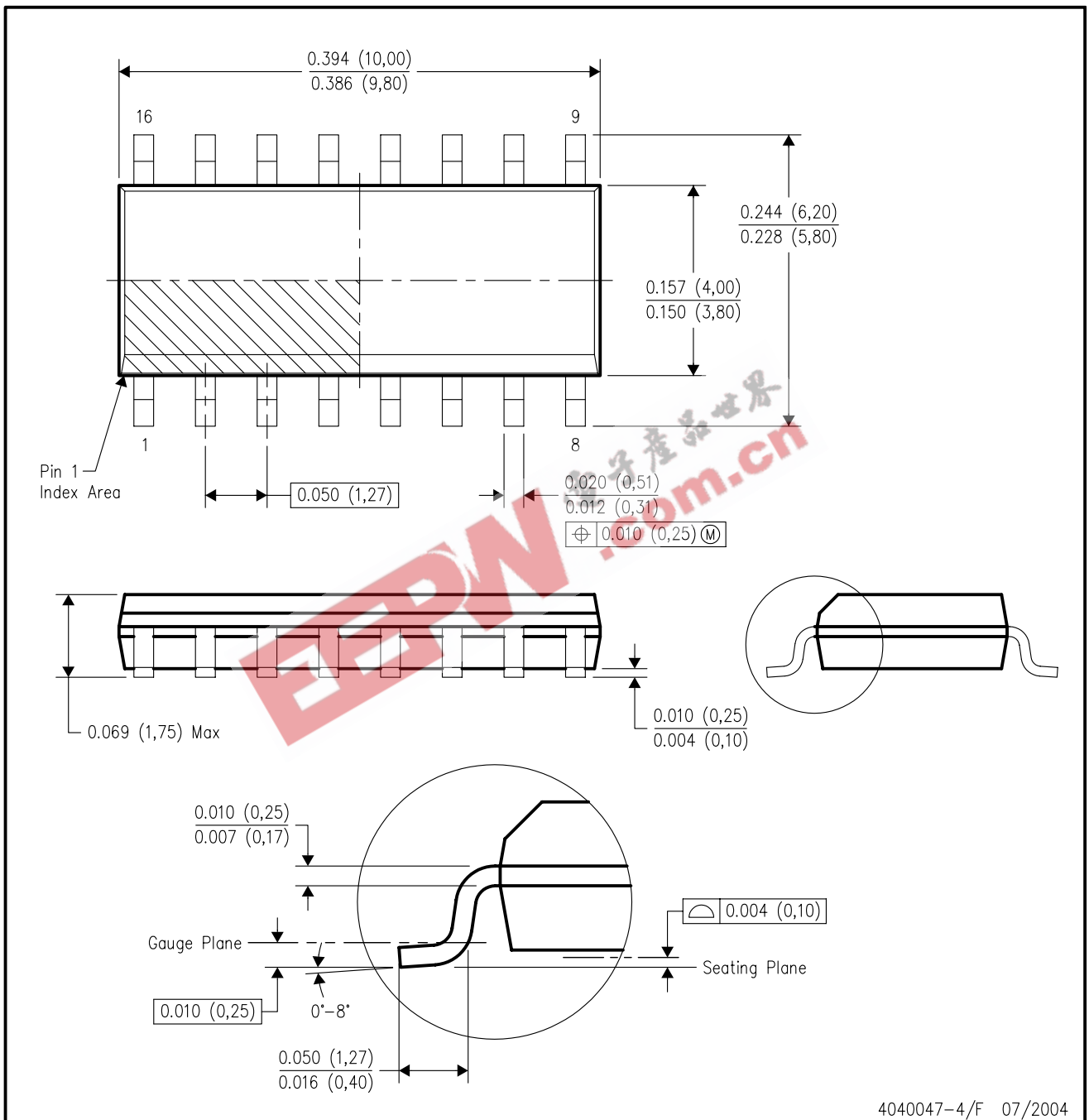
4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE

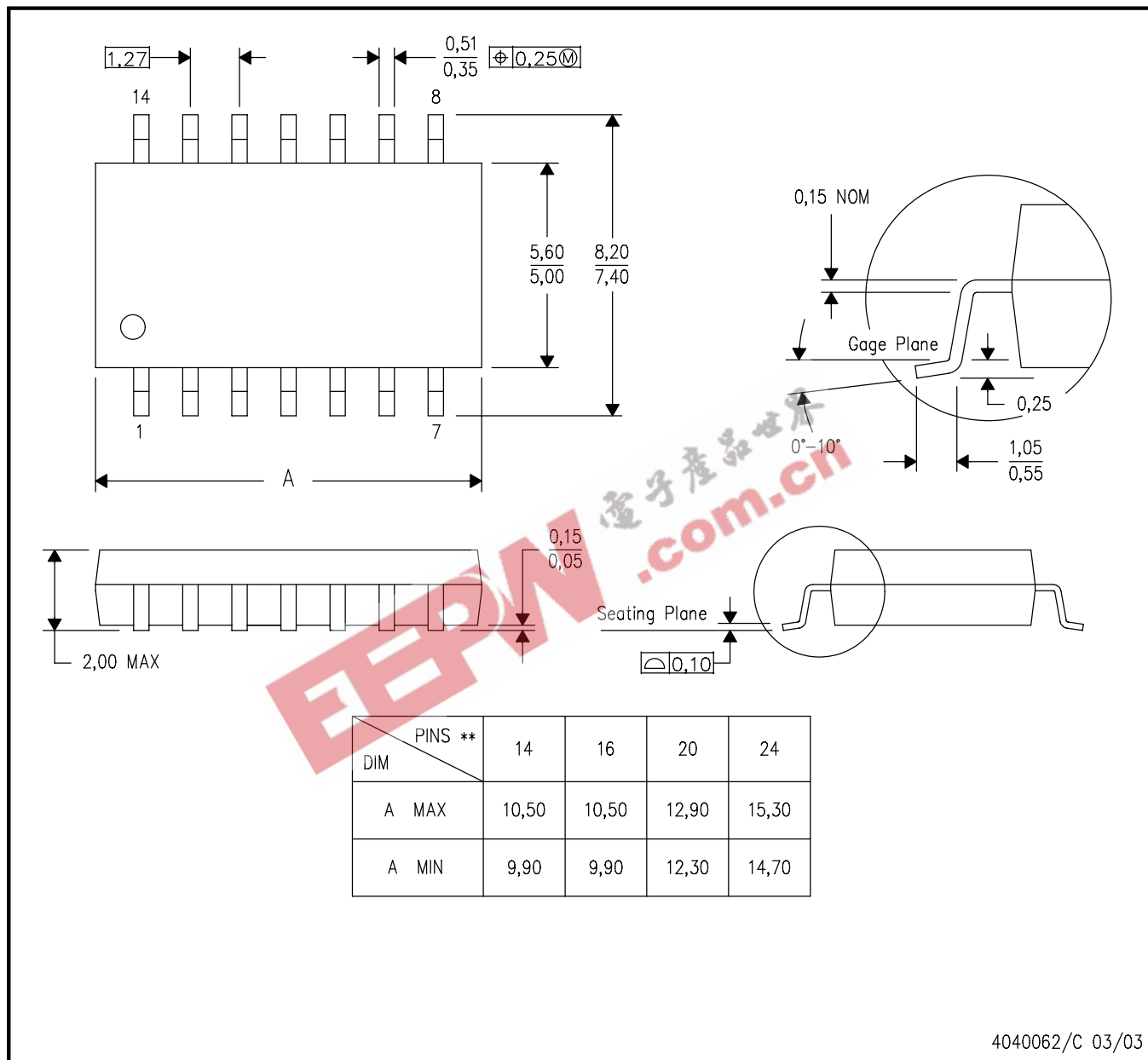


MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265