

## 4-ch MOTOR DRIVER FOR PORTABLE CD PLAYERS

### —YD5901

#### DESCRIPTION

This driver IC contains a 4ch H bridge driver and DC-DC converter control circuit on one chip, and was developed for use in portable CD players. QFP-44 is used for the package, making it ideal for smaller sets.

#### FEATURES

\*Built-in 4ch H Bridge Driver, and PWM Control of Load Drive Voltage is Made Possible by External Components.

\*DC-DC Converter Control Circuit on Chip.

\* With Reset Output Inversion Output Pin.

\*Empty Detection Level Can be Switched Between Rechargeable Battery and Dry Battery.

\*Constant Current Charging; Current Value Can be Varied Using External Resistor.

\*Built-in Power Transistor For Charging.

\*Built-in Independent Thermal Shutdown Circuit.

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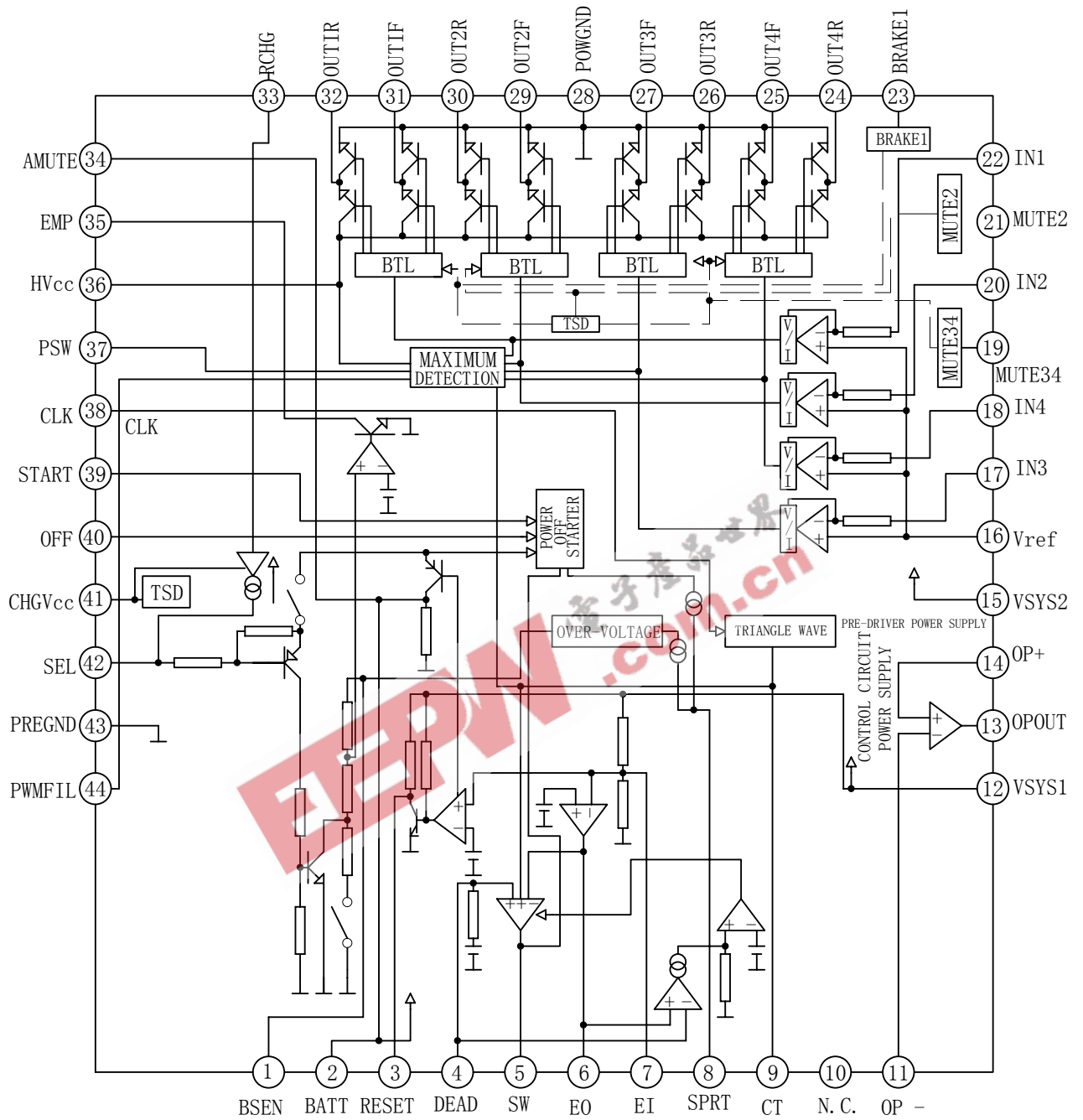
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BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS** (Tamb=25°C)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc*1	13.5	V
Driver Output Current	Io	500	mA
Power Dissipation	Pd	625*2	mW
Operating Temperature	Topr	-30 to +85	°C
Storage Temperature	Tstg	-55 to +150	°C

\*1 Vcc shows input voltage of VSYS1, VSYS3, HVcc, BATT, and CHGVcc.

\*2 Reduced by 5mW for each increase in Tamb of 1°C over 25°C.

**ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, Tamb=25°C, BATT=2.4V,

VSYS1=VSYS2=3.2V, Vref=1.6V, CHGVcc=0V, fCLK=88.2kHz)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Common Section</b>						
BATT Stand-by Current	I <sub>ST</sub>	BATT=9.0V, VSYS1=VSYS2=Vref=0V		0	3	μA
BATT Supply Current (No Load)	I <sub>BAT</sub>	HVcc=0.45V, MUTE34=3.2V		2.5	4.0	mA
VSYS1 Supply Current (No Load)	I <sub>YSY1</sub>	HVcc=0.45V, MUTE34=3.2, EI=0V		4.7	6.4	mA
VSYS2 Supply Current (No Load)	I <sub>YSY2</sub>	HVcc=0.45V, MUTE34=3.2V		4.1	5.5	mA
CHGVcc Supply Current (No Load)	I <sub>CGVCC</sub>	CHGVcc=4.5V, R <sub>OUT</sub> =OPEN		0.65	2.00	mA
<b>H-Bridge Driver Part</b>						
Voltage Gain ch1, ch3, ch4	G <sub>VC134</sub>		12	14	16	dB
Voltage Gain ch2	G <sub>VC2</sub>		21.5	23.5	24.5	dB
Gain Error By Polarity	ΔG <sub>VC</sub>		-2	0	2	dB
Input Pin Resistance ch1, ch3, ch4	R <sub>IN134</sub>	IN=1.7V and 1.8V	9	11	13	kΩ
Input Pin Resistance ch2	R <sub>IN2</sub>	IN=1.7V and 1.8V	6	7.5	9	kΩ
Maximum Output Voltage	V <sub>OUT</sub>	RL=8Ω, HVcc=BATT=4.0V, IN=0-3.2V	1.9	2.1		V
Saturation Voltage (Lower)	V <sub>satL</sub>	I <sub>O</sub> =-300mA, IN=0 和 3.2V		240	400	mV

Saturation Voltage (Upper)	V <sub>satU</sub>	I <sub>O</sub> =-300mA, I <sub>N</sub> =0 和 3.2V		240	400	mV
Input Offset Voltage	V <sub>OI</sub>		-8	0	8	mV
Output Offset Voltage ch1, ch3, ch4	V <sub>OO134</sub>	V <sub>ref</sub> =I <sub>N</sub> =1.6V	-50	0	50	mV
Output Offset Voltage ch2	V <sub>OO2</sub>	V <sub>ref</sub> =I <sub>N</sub> =1.6V	-130	0	130	mV
Dead Zone	V <sub>DB</sub>		-10	0	10	mV
BRAKE1 ON Threshold Voltage	V <sub>BRON</sub>	I <sub>N1</sub> =1.8V	2.0			V
BRAKE1 OFF Threshold Voltage	V <sub>BROFF</sub>	I <sub>N1</sub> =1.8V			0.8	V
MUTE2 ON Threshold Voltage	V <sub>M2ON</sub>	I <sub>N2</sub> =1.8V	2.0			V
<b>H-Bridge Driver Part</b>						
MUTE2 OFF Threshold Voltage	V <sub>M2OFF</sub>	I <sub>N2</sub> =1.8V			0.8	V
MUTE34 ON Threshold Voltage	V <sub>M34ON</sub>	I <sub>N3</sub> =I <sub>N4</sub> =1.8V			0.8	V
MUTE34 OFF Threshold Voltage	V <sub>M34OFF</sub>	I <sub>N3</sub> =I <sub>N4</sub> =1.8V	2.0			V
V <sub>ref</sub> ON Threshold Voltage	V <sub>refON</sub>	I <sub>N1</sub> =I <sub>N2</sub> =I <sub>N3</sub> =I <sub>N4</sub> =1.8V	1.2			V
V <sub>ref</sub> OFF Threshold Voltage	V <sub>refOFF</sub>	I <sub>N1</sub> =I <sub>N2</sub> =I <sub>N3</sub> =I <sub>N4</sub> =1.8V			0.8	V
BRAKE1 Brake Current	I <sub>BRAKE1</sub>	Current difference between BRAKE pin "H" time and "L" time.	4	7	10	mA
<b>PWM Power Supply Driving</b>						
PSW Sink Current	I <sub>PSW</sub>	I <sub>N1</sub> =2.1V	10	13	17	mA
HV <sub>cc</sub> Level Shift Voltage	V <sub>SHIF</sub>	I <sub>N1</sub> =1.8V, HV <sub>cc</sub> -OUT1F	0.35	0.45	0.55	V
HV <sub>cc</sub> Leak Current	I <sub>HLK</sub>	HV <sub>cc</sub> =9.0V, V <sub>SYS1</sub> =V <sub>SYS2</sub> =BATT =0V		0	5	μA
PWM Amp Transfer Gain		HV <sub>cc</sub> =1.8V, HV <sub>cc</sub> =1.2~1.4V	1/60	1/50	1/40	1/kΩ
<b>DC-DC Converter</b>						
<b>Error Amp</b>						
V <sub>SYS1</sub> Threshold Voltage	V <sub>SITH</sub>		3.05	3.20	3.35	V

EO Pin Output Voltage “H”	$V_{EOH}$	EI=0.7V, $I_o=-100\ \mu A$	1.4	1.6		V
EO Pin Output Voltage “L”	$V_{EOL}$	EI=1.3V, $I_o=100\ \mu A$			0.3	V
<b>Short Circuit Protection</b>						
SPRT Pin Voltage	$V_{SPR}$	EI=1.3V		0	0.1	V
EO=H SPRT Pin Current1	$I_{SPR1}$	EI=0.7V	6	10	16	$\mu A$
OFF=L SPRT Pin Current2	$I_{SPR2}$	EI=1.3V, OFF=0V	12	20	32	$\mu A$
SPRT Pin Current3 Over-Voltage	$I_{SPR3}$	EI=1.3V, BATT=9.5V	12	20	32	$\mu A$
SPRT Pin Impedance	$R_{SPR}$		175	220	265	k $\Omega$
SPRT Pin Threshold Voltage	$V_{SPTH}$	EI=0.7V, $C_T=0V$	1.10	1.20	1.30	V
Over-Voltage Protection Detect	$V_{HVPR}$	BSEN Pin Voltage	8.0	8.4	9.0	V
<b>Transistor Driving</b>						
SW Pin Output Voltage1 “H”	$V_{SW1H}$	BATT= $C_T=1.5V$ , $S1=VSYS2=0V$ , $I_o=-2mA$ Starting Time	0.78	0.98	1.13	V
SW Pin Output Voltage 2 “H”	$V_{SW2H}$	$C_T=0V$ , $I_o=-10mA$ , EI=0.7V, SPRT=0V	1.00	1.50		V
SW Pin Output Voltage 2 “L”	$V_{SW2L}$	$C_T=20V$ , $I_o=-10mA$		0.30	0.45	V
SW Pin Oscillating Frequency1	$f_{sw1}$	$C_T=470pF$ , $VSYS1=YSYS2=0V$ Starting time	65	80	95	kHz
SW Pin Oscillating Frequency 2	$f_{sw2}$	$C_T=470pF$ , CLK=0V	60	70	82	kHz
SW Pin Oscillating Frequency 3	$f_{sw3}$	$C_T=470pF$		88.2		kHz
SW Pin Minimum Pulse Width	$T_{SWMIN}$	$C_T=470pF$ , EO=0.5V→0.7V Sweep	0.01		0.60	ms
Pulse Duty Start	$D_{SW1}$	$C_T=470pF$ , $VSYS1=VSYS2=0V$	40	50	60	%
Max. Pulse Duty At Self-Running	$D_{SW2}$	$C_T=470pF$ , EI=0.7V, CLK=0V	70	80	90	%
Max. Pulse Duty At CLK Synchronization	$D_{SW3}$	$C_T=470pF$ , EI=0.7V	65	75	85	%

<b>Interface</b>						
OFF Pin Threshold Voltage	$V_{OFFH}$	EI=1.3V			VSYS1 -2.0	V
OFF Pin Bias Current	$I_{OFF}$	OFF=0V	75	95	115	$\mu$ A
START Pin ON Threshold Voltage	$V_{STATH1}$	VSYS1=VSYS2=0V, $C_T=2.0V$			BATT- 1.0	V
START Pin OFF Threshold Voltage	$V_{STATH2}$	VSYS1=VSYS2=0V, $C_T=2.0V$	BATT- 0.3			V
START Pin Bias Current	$I_{START}$	START=0V	10	20	30	$\mu$ A
CLK Pin Threshold Voltage "H"	$V_{CLKTHH}$		2.0			V
CLK Pin Threshold Voltage "L"	$V_{CLKTHL}$				0.8	V
CLK Pin Bias Current	$I_{CLK}$	CLK=3.2V			10	$\mu$ A
<b>Dead Time</b>						
DEAD Pin Impedance	$R_{DEAD}$		52	65	78	k $\Omega$
DEAD Pin Output Voltage	$V_{DEAD}$		0.78	0.88	0.98	V
<b>Starter Circuit</b>						
Starter Switching Voltage	$V_{STNM}$	VSYS1=VSYS2=0V → 3.2V, START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	$V_{SNHS}$	START=0V	130	200	300	mV
Discharge Release	$V_{DIS}$		1.63	1.83	2.03	V
<b>Empty Detection</b>						
EMP Detection Voltage1	$V_{EMPT1}$	VSEL=0V	2.1	2.2	2.3	V
EMP Detection Voltage2	$V_{EMPT2}$	ISEL=-2 $\mu$ A	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	$V_{EMHS1}$	VSEL=0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	$V_{EMHS2}$	ISEL=-2 $\mu$ A	25	50	100	mV
EMP Pin Output Voltage	$V_{EMP}$	$I_O=1mA, BSEN=1V$			0.5	V
EMP Pin Output Leak Current	$I_{EMPL}$	BSEN=2.4V			1.0	$\mu$ A
BSEN Pin Input Resistance	$R_{BSEN}$	VSEL=0V	17	23	27	k $\Omega$

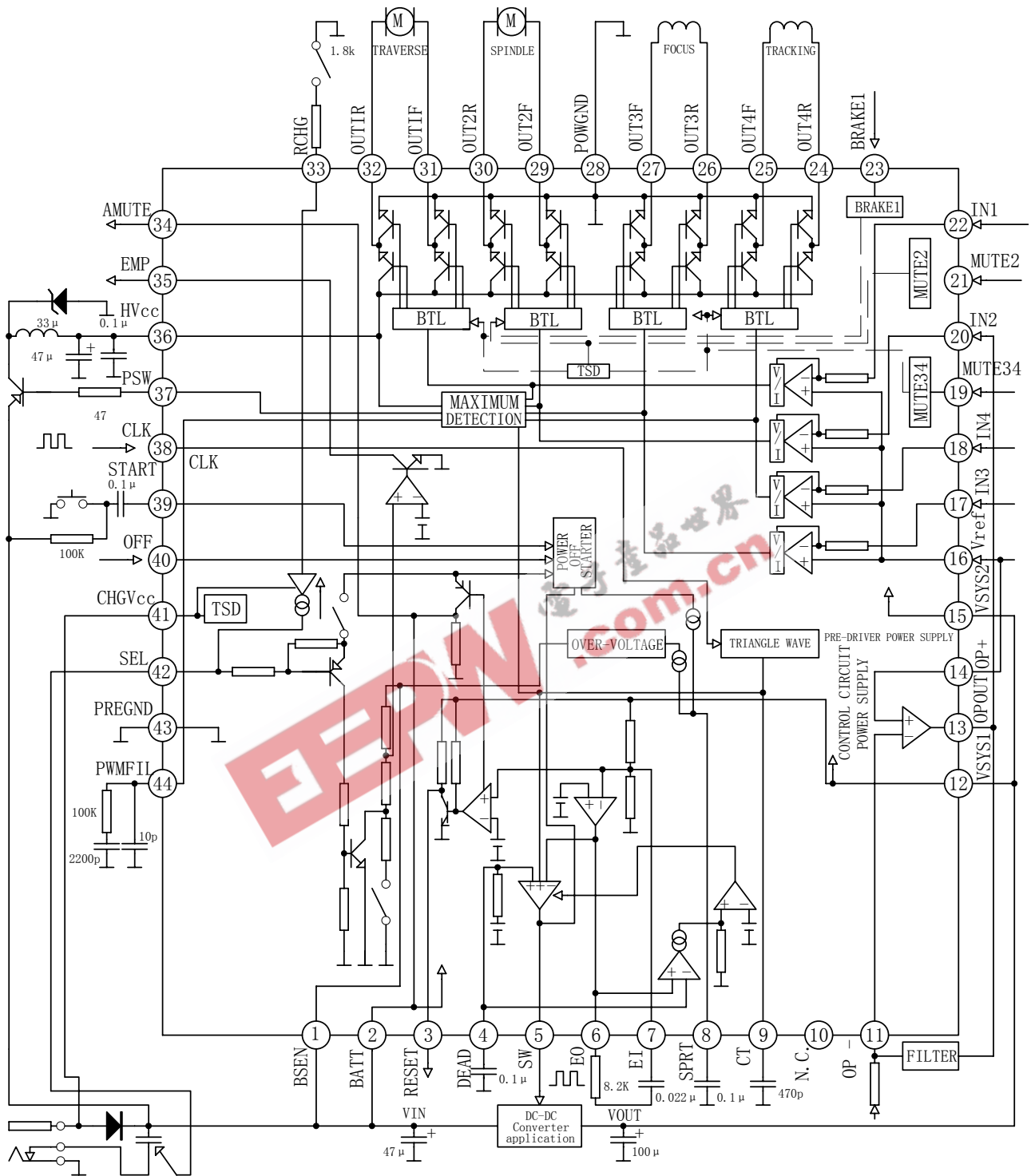
BSEN Pin Leak Current	$I_{BSENL}$	VSYS1=VSYS2=0V, BSEN=4.5V			1.0	mA
SEL Pin Detection Voltage	$V_{SELTH}$	VSELTH=BATT-SEL, BSEN=2.0V	1.5			V
SEL Pin Detection Current	$I_{SELT}$		-2			$\mu A$
<b>Reset Circuit</b>						
VSYS1RESET Threshold Voltage Ratio	$H_{SRT}$	Comparison with error amplifier threshold voltage	85	90	95	%
RESET Detection Hysteresis Width	$V_{RSTHS}$		25	50	100	mV
RESET Pin Output Voltage	$V_{RST}$	$I_o=1mA,$ VSYS1=VSYS2=2.8V			0.5	V
RESET Pin PULL UP Resistance	$R_{RST}$		72	90	108	k $\Omega$
AMUTE Pin Output Voltage1	$V_{AMT1}$	$I_o=-1mA,$ VSYS1=VSYS2=2.8V	BATT-0.4		BATT	V
AMUTE Pin Output Voltage2	$V_{AMT2}$	$I_o=-1mA, START=0V,$ VSYS1=VSYS2=0V	BATT-0.4		BATT	V
AMUTE Pin PULL DOWN Resistance	$R_{AMT}$		77	95	113	k $\Omega$
<b>Op Amp</b>						
Input Bias Current	$I_{BIAS}$	OP+=1.6V			300	nA
Input Offset Voltage	$V_{OIOP}$		-5.5	0	5.5	mV
High Level Offset Voltage	$V_{OHOP}$	RL=OPEN	2.8			V
Low Level Offset Voltage	$V_{OLOP}$	RL=OPEN			0.2	V
Output Drive Current (Source)	$I_{SOU}$	50 $\Omega$ GND		-6.5	-3.0	mA
Output Drive Current (Sink)	$I_{SIN}$	50 $\Omega$ GND	0.4	0.7		mA
Open Loop Voltage Gain	GVO	$V_{IN}=-7.5dBV, f=1kHz$		70		dB
Slew Rate	SR			0.5		V/ $\mu s$
<b>Battery Charging Circuit</b>						
RCHG Pin Bias Voltage	$V_{RCHG}$	CHGVcc=4.5V, RCHG=1.8k $\Omega$	0.71	0.81	0.91	V
RCHG Pin Output Resistance	$R_{RCHG}$	CHGVcc=4.5V, RCHG=0.5V 和 0.6V	0.75	0.95	1.2	k $\Omega$

SEL Pin Leak Current 1	$I_{\text{SELLK1}}$	CHGV <sub>cc</sub> =4.5V, RCHG=OPEN, BATT=4.5V			1.0	mA
SEL Pin Leak Current 2	$I_{\text{SELLK2}}$	CHGV <sub>cc</sub> =0.6V, RCHG=1.8k $\Omega$ , BATT=4.5V			1.0	$\mu$ A
SEL Pin Saturation Voltage	$V_{\text{SELCG}}$	CHGV <sub>cc</sub> =4.5V, $I_0=300\text{mA}$ , RCHG=0 $\Omega$		0.45	1.00	V

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APPLICATION CIRCUIT



OUTLINE DRAWING

