

SDLS120 – MARCH 1974 – REVISED MARCH 1988

(TOP VIEW)

1Q̄	1	16	1Q
1D	2	15	2Q
2D	3	14	2Q̄
3C, 4C	4	13	1C, 2C
VCC	5	12	GND
3D	6	11	3Q̄
4D	7	10	3Q
4Q̄	8	9	4Q

Q_n = the level of Q before the high-to-low transition of G

(TOP VIEW)

1D	1	14	1Q
2D	2	13	2Q
3C, 4C	3	12	1C, 2C
VCC	4	11	GND
3D	5	10	NC
4D	6	9	3Q
NC	7	8	4Q

logic symbols†

Supply voltage, V _{CC} (See Note 1)	7 V
Input voltage: '75, '77	5.5 V
'LS75, 'LS77	7 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54'	– 55°C to 125°C
SN74'	0° C to 70°C
Storage temperature range	– 65°C to 150°C

1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor and is not applicable to the 'LS75 and 'LS77.

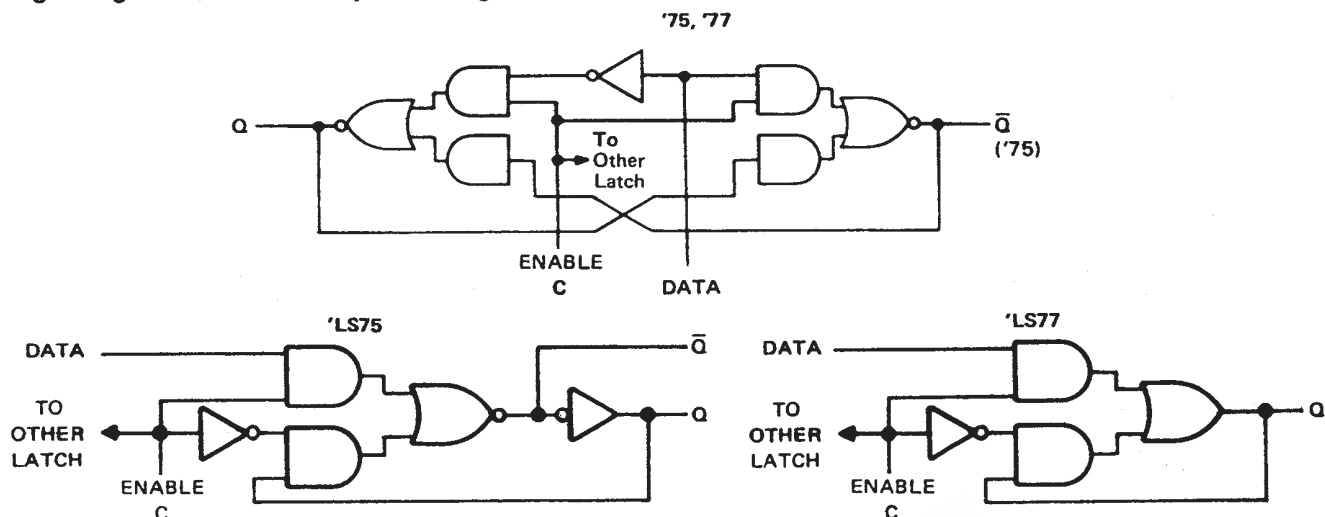


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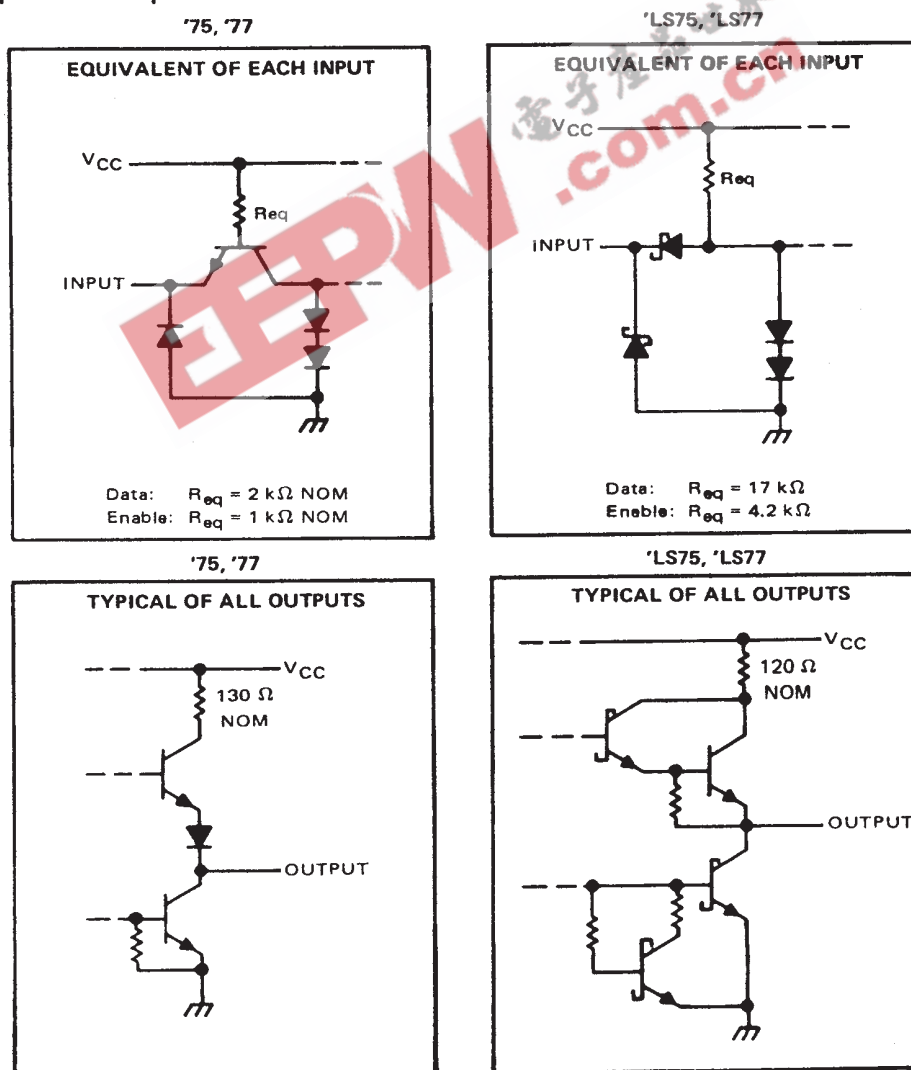
SN5475, SN5477, SN54LS75, SN54LS77 SN7475, SN74LS75 4-BIT BISTABLE LATCHES

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logic diagrams (each latch) (positive logic)



schematics of inputs and outputs



SN5475, SN5477, SN54LS75, SN54LS77
SN7475, SN74LS75
4-BIT BISTABLE LATCHES

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recommended operating conditions

	SN5475, SN5477			SN7475			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μ A
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{su}	20			20			ns
Hold time, t_h	5			5			ns
Operating free-air temperature, T_A	–55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	MIN	TYP [‡]	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			–1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -400 \mu\text{A}$	2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1	mA
I_{IH}	High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			80	μ A
					160	
I_{IL}	Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			–3.2	mA
					–6.4	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	SN54'	–20	–57	mA
			SN74'	–18	–57	
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3	SN54'	32	46	mA
			SN74'	32	53	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	$C_L = 15\text{ pF},$ $R_L = 400\ \Omega,$ See Figure 1	16	30	ns	
t_{PHL}				14	25		
$t_{PLH}^{\dagger\dagger}$	D	$\overline{Q}$		24	40	ns	
$t_{PHL}^{\dagger\dagger}$				7	15		
t_{PLH}	C	Q		16	30	ns	
t_{PHL}				7	15		
$t_{PLH}^{\dagger\dagger}$	C	$\overline{Q}$		16	30	ns	
$t_{PHL}^{\dagger\dagger}$				7	15		

$t_{PLH} \equiv$ propagation delay time, low-to-high-level output

$t_{PHL} \equiv$ propagation delay time, high-to-low-level output

^{††} These parameters are not applicable for the SN5477.

SN5475, SN5477, SN54LS75, SN54LS77
SN7475, SN74LS75
4-BIT BISTABLE LATCHES

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recommended operating conditions

	SN54LS75 SN54LS77			SN74LS75			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			–400			–400	μA
Low-level output current, I_{OL}			4			8	mA
Width of enabling pulse, t_W	20			20			ns
Setup time, t_{SU}	20			20			ns
Hold time, t_H	5			5			ns
Operating free-air temperature, T_A	–55		125	0		70	$^{\circ}C$

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS75 SN54LS77			SN74LS75			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			–1.5			–1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu A$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL} \text{ max}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$				0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$	D input		0.1			0.1	mA
		C input		0.4			0.4	
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$	D input		20			20	μA
		C input		80			80	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$	D input		–0.4			–0.4	mA
		C input		–1.6			–1.6	
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	–20		–100	–20		–100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 2	'LS75		6.3	12	6.3	12	mA
		'LS77		6.9	13			

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}C$

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS75		'LS77			UNIT
				MIN	MAX	MIN	TYP	MAX	
tPLH	D	Q	CL = 15 pF, RL = 2 kΩ, See Figure 1	15	27	11	19	ns	
tPHL				9	17	9	17		
tPLH	D	Q̄		12	20			ns	
tPHL				7	15				
tPLH	C	Q		15	27	10	18	ns	
tPHL				14	25	10	18		
tPLH	C	Q̄		16	30			ns	
tPHL				7	15				

¶ t_{PLH} = propagation delay time, low-to-high-level output

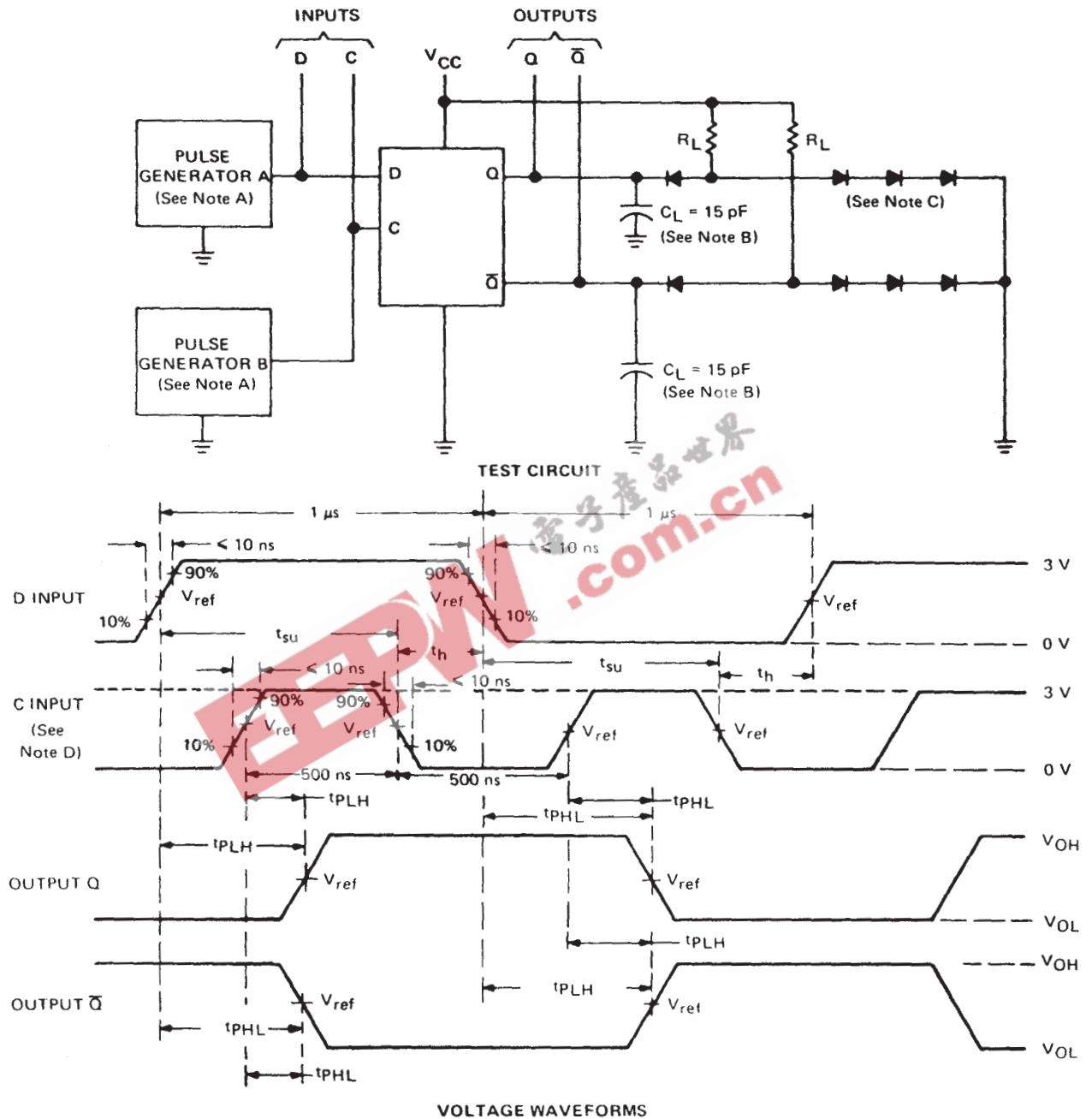
t_{PHL} = propagation delay time, high-to-low-level output

SN5475, SN5477, SN54LS75, SN54LS77
SN7475, SN74LS75
4-BIT BISTABLE LATCHES

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switching characteristics†

PARAMETER MEASUREMENT INFORMATION



† Complementary Q outputs are on the '75 and 'LS75 only.

- NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50 \Omega$; for pulse generator A, $PRR \leq 500 \text{ kHz}$; for pulse generator B, $PRR \leq 1 \text{ MHz}$. Positions of D and C input pulses are varied with respect to each other to verify setup times.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.
- D. When measuring propagation delay times from the D input, the corresponding C input must be held high.
- E. For '75 and '77, $V_{ref} = 1.5 \text{ V}$; for 'LS75 and 'LS77, $V_{ref} = 1.3 \text{ V}$.

FIGURE 1

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