Winbond Electronics Corp.

150MHZ 4-DIMM CLOCK

1.0 GENERAL DESCRIPTION

The W83195R-08 is a Clock Synthesizer which provides all clocks required for high-speed RISC or CISC microprocessor such as Intel Pentium II. W83195R-08 provides sixteen CPU/PCI frequencies which are externally selectable with smooth transitions. W83195R-08 also provides 17 SDRAM clocks controlled by the none-delay buffer_in pin.

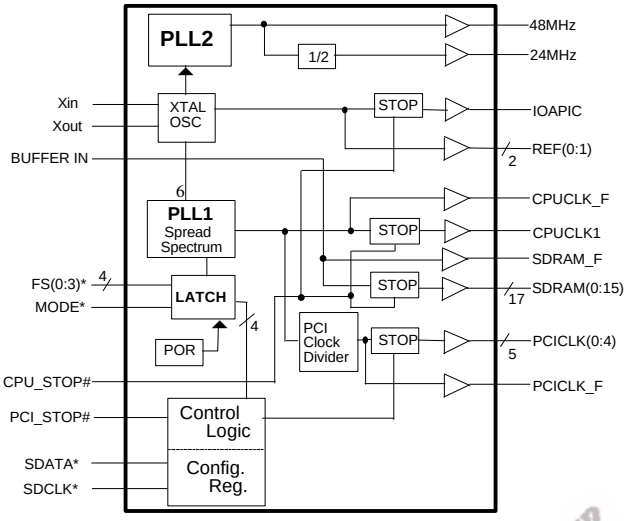
The W83195R-08 accepts a 14.318 MHz reference crystal as its input and runs on a 3.3V supply. Spread spectrum built in at ¡Ó0.5% or ¡Ó0.25% to reduce EMI. Programmable stopping individual clock outputs and frequency selection through I^2C interface. The device meets the Pentium power-up stabilization, which requires CPU and PCI clocks be stable within 2 ms after power-up. Using dual function pin for the slots(ISA, PCI, CPU, DIMM) is not recommend. The add on cards may have a pull up or pull down.

High drive seven PCI and SDRAM CLOCK outputs typically provide greater than 1 V /ns slew rate into 30 pF loads. Two CPU CLOCK outputs typically provide better than 1 V /ns slew rate into 20 pF loads, when maintaining 50¡Ó 5% duty cycle. The fixed frequency outputs, such as REF, 24MHz and 48 MHz provide better than 0.5V /ns slew rate.

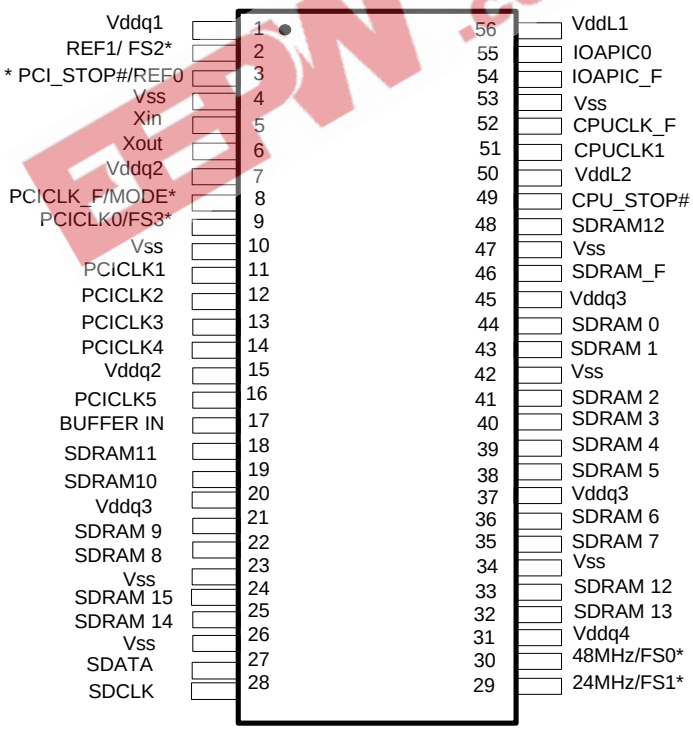
2.0 PRODUCT FEATURES

- Supports Pentium™ II CPU with I^2C.
- 3 CPU clocks (one free-running CPU clock)
- 17 SDRAM clocks for 4 DIMs
- 7 PCI synchronous clocks
- Two IOAPIC clocks for multiprocessor support
- Optional single or mixed supply:
  (Vddq1=Vddq2 = Vddq3 = Vddq4 = VddL1 =VddL2= 3.3V) or (Vddq1= Vddq2 = Vddq3=Vddq4 = 3.3V, VddL1 = VdqL2 = 2.5V)
- < 250ps skew among CPU and SDRAM clocks
- < 250ps skew among PCI clocks
- < 5ns propagation delay SDRAM from buffer input
- Skew from CPU(earlier) to PCI clock -1 to 4ns, center 2.6ns.
- Smooth frequency switch with selections from 50 MHz to 133 MHz CPU
- I^2C 2-Wire serial interface and I^2C read back
- ¡Ó0.25% or ¡Ó0.5% center type spread spectrum function to reduce EMI
- Programmable registers to enable/stop each output and select modes (mode as Tri-state or Normal)
- MODE pin for power Management
- One 48 MHz for USB & one 24 MHz for super I/O
- 56-pin SSOP package

3.0 BLOCK DIAGRAM



4.0 PIN CONFIGURATION



5.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Active Low

* - Internal 250kΩ pull-up

5.1 Crystal I/O

SYMBOL	PIN	I/O	FUNCTION
Xin	5	IN	Crystal input with internal loading capacitors and feedback resistors.
Xout	6	OUT	Crystal output at 14.318MHz nominally.

5.2 CPU, SDRAM, PCI, IOAPIC Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CPUCLK_F	52	OUT	Free running CPU clock. Not affected by CPU_STOP#
CPUCLK1	51	OUT	Low skew (< 250ps) clock outputs for host frequencies such as CPU, Chipset and Cache. Powered by VddL2. Low if CPU_STOP# is low.
CPU_STOP#	47	IN	This asynchronous input halts CPUCLK1,IOAPIC & SDRAM(0:12) at logic "0" level when driven low.
IOAPIC0	55	OUT	High drive buffered output of the crystal, and is powered by VddL1.
IOAPIC_F	54	OUT	Free running IOAPIC clock, and not affected by CPU_STOP#
SDRAM [0:15]	18,19,21,22,24 ,25,32,33,35, 36,38,39,40,41 ,43,44	OUT	SDRAM clock outputs. Fanout buffer outputs from BUFFER IN pin.(Controlled by chipset)
PCICLK_F/ *MODE	8	I/O	Free running PCI clock during normal operation. Latched Input. Mode=1, Pin 2 is REF0; Mode=0, Pin2 is PCI_STOP#
PCICLK0/*FS3	9	I/O	Low skew (< 250ps) PCI clock outputs. Latched input for FS3 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
PCICLK [1:5]	11,12,13,14,16	OUT	Low skew (< 250ps) PCI clock outputs. Synchronous to CPU clocks with 1-48ns skew(CPU early).
BUFFER IN	17	IN	Inputs to fanout for SDRAM outputs.
SDRAM_F	46	O	Free running SDRAM clock, and not affected by CPU_STOP#

5.3 I²C Control Interface

SYMBOL	PIN	I/O	FUNCTION
*SDATA	27	I/O	Serial data of I²C 2-wire control interface with internal pull-up resistor.
*SDCLK	28	IN	Serial clock of I²C 2-wire control interface with internal pull-up resistor.

5.4 Fixed Frequency Outputs

SYMBOL	PIN	I/O	FUNCTION
REF0 / PCI_STOP#	3	I/O	14.318MHz reference clock. This REF output is the stronger buffer for ISA bus loads. Halt PCICLK(0:4) clocks at logic 0 level, when input low (In mobile mode. MODE=0)
REF1 / *FS2	2	I/O	14.318MHz reference clock. Latched input for FS2 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
24MHz / *FS0	30	I/O	24MHz output clock. Latched input for FS1 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.
48MHz / *FS1	29	I/O	48MHz output for USB during normal operation. Latched input for FS0 at initial power up for H/W selecting the output frequency of CPU, SDRAM and PCI clocks.

5.5 Power Pins

SYMBOL	PIN	FUNCTION
Vddq1	1	Power supply for Ref [0:1] crystal and core logic.
VddL1	56	Power supply for IOAPIC output, either 2.5V or 3.3V.
VddL2	50	Power supply for CPUCLK_F & CPUCLK[1:2], either 2.5V or 3.3V.
Vddq2	7,15	Power supply for PCICLK_F, PCICLK[0:5], 3.3V.
Vddq3	20,37,45	Power supply for SDRAM_F & SDRAM[0:15], and CPU PLL core, nominal 3.3V.
Vddq4	31	Power for 24 & 48MHz output buffers and fixed PLL core.
Vss	4,10,23,26,34,42,48, 53	Circuit Ground.

6.0 FREQUENCY SELECTION

FS3=0			CPU,SDRAM (MHz)	PCI (MHz)	REF,IOAPIC
FS2	FS1	FS0			(MHz)
0	0	0	124	41.33(CPU/3)	14.318
0	0	1	75	37.5(CPU/2)	14.318
0	1	0	83.3	41.65(CPU/2)	14.318
0	1	1	66.8	33.4(CPU/2)	14.318
1	0	0	103	34.3(CPU/3)	14.318
1	0	1	112	37.33(CPU/3)	14.318
1	1	0	133	44.33(CPU/3)	14.318
1	1	1	100.3	33.3(CPU/3)	14.318
FS3=1			CPU,SDRAM (MHz)	PCI (MHz)	REF,IOAPIC
FS2	FS1	FS0			(MHz)
0	0	0	120	40.00(CPU/3)	14.318
0	0	1	115	38.33(CPU/3)	14.318
0	1	0	110	36.67(CPU/3)	14.318
0	1	1	105	35.00(CPU/3)	14.318
1	0	0	140	35.00(CPU/4)	14.318
1	0	1	150	37.50(CPU/4)	14.318
1	1	0	124	31.00(CPU/4)	14.318
1	1	1	133	33.25(CPU/4)	14.318

7.0 MODE PIN -POWER MANAGEMENT INPUT CONTROL

MODE, Pin8 (Latched Input)	PIN 3
0	PCI_STOP# (Input)
1	REF0 (Output)

8.0 FUNTION DESCRIPTION

8.1 POWER MANAGEMENT FUNCTIONS

All clocks can be individually enabled or disabled via the 2-wire control interface. On power up, external circuitry should allow 3 ms for the VCO's to stabilize prior to enabling clock outputs to assure correct pulse widths. When MODE=0, pins 3 and 47 are inputs (PCI_STOP#), (CPU_STOP#), when MODE=1, these functions are not available. A particular clock can be enabled as both the 2-wire serial control interface and one of these pins indicate that it should be enable.

The W83195R-08 may be disabled in the low state according to the following table in order to reduce power consumption. All clocks are stopped in the low state, but maintain a valid high period on transitions from running to stop. The CPU and PCI clocks transform between running and stop by waiting for one positive edge on PCICLK_F followed by negative edge on the clock of interest, after which high levels of the output are either enabled or disabled.

CPU_STOP#	PCI_STOP#	CPUCLK[1:2] IOAPIC0 & SDRAM [0:15]	PCI	OTHER CLKs	XTAL & VCOs
0	0	LOW	LOW	RUNNING	RUNNING
0	1	LOW	RUNNING	RUNNING	RUNNING
1	0	RUNNING	LOW	RUNNING	RUNNING
1	1	RUNNING	RUNNING	RUNNING	RUNNING

8.2 2-WIRE I^{2}C CONTROL INTERFACE

The clock generator is a slave I^{2}C component which can be read back the data stored in the latches for verification. All proceeding bytes must be sent to change one of the control bytes. The 2-wire control interface allows each clock output individually enabled or disabled. On power up, the W83195R-08 initializes with default register settings. Use of the 2-wire control interface is then optional.

The SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high during normal data transfer. There are only two exceptions. One is a high-to-low transition on SDATA while SDCLK is high used to indicate the beginning of a data transfer cycle. The other is a low-to-high transition on SDATA while SDCLK is high used to indicate the end of a data transfer cycle. Data is always sent as complete 8-bit bytes followed by an acknowledge generated.

Byte writing starts with a start condition followed by 7-bit slave address and a write command bit [1101 0010], command code checking [0000 0000], and byte count checking. After successful reception of each byte, an acknowledge (low) on the SDATA wire will be generated by the clock chip. Controller can start to write to internal I^{2}C registers after the string of data. The sequence order is as follows:

Bytes sequence order for I^2C controller :

Clock Address A(6:0) & R/W	Ack	8 bits dummy Command code	Ack	8 bits dummy Byte count	Ack	Byte0,1,2... until Stop

Set R/W to 1 when read back the data sequence is as follows [1101 0011] :

Clock Address A(6:0) & R/W	Ack	Byte 0	Ack	Byte 1	Ack	Byte2, 3, 4... until Stop

8.3 SERIAL CONTROL REGISTERS

The Pin column lists the affected pin number and the PowerUp column gives the default state at true power up. "Command Code" byte and "Byte Count" byte must be sent following the acknowledge of the Address Byte. Although the data (bits) in these two bytes are considered "don't care", they must be sent and will be acknowledge. After that, the sequence described below (Register 0, Register 1, Register 2, ...) will be valid and acknowledged.

8.3.1 Register 0: CPU Frequency Select Register (default = 0)

Bit	@PowerUp	Pin	Description
7	0	-	0 = ¡Ó0.25% Spread Spectrum Modulation 1 = ¡Ó0.5% Spread Spectrum Modulation
6	0	-	SSEL2 (for frequency table selection by software via I^2C)
5	0	-	SSEL1 (for frequency table selection by software via I^2C)
4	0	-	SSEL0 (for frequency table selection by software via I^2C)
3	0	-	0 = Selection by hardware 1 = Selection by software I^2C - Bit 6:4, 2
2	0	-	SSEL3 (for frequency table selection by software via I^2C)
1	0	-	0 = Normal 1 = Spread Spectrum enabled
0	0	-	0 = Running 1 = Tristate all outputs

Note : The frequency table selected by software via I^2C is the same as the hardware setting frequency table.

8.3.2 Register 1 : CPU , 48/24 MHz Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	46	SDRAM16 (Active / Inactive)
2	1	49	CPUCLK2 (Active / Inactive)
1	1	51	CPUCLK1 (Active / Inactive)
0	1	52	CPUCLK_F (Active / Inactive)

8.3.3 Register 2: PCI Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	8	PCICLK_F (Active / Inactive)
5	1	16	PCICLK5 (Active / Inactive)
4	1	14	PCICLK4 (Active / Inactive)
3	1	13	PCICLK3 (Active / Inactive)
2	1	12	PCICLK2 (Active / Inactive)
1	1	11	PCICLk1 (Active / Inactive)
0	1	9	PCICLK0 (Active / Inactive)

8.3.4 Register 3: SDRAM Clock Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	30	48MHz (Active / Inactive)
4	1	29	24MHz (Active / Inactive)
3	1	33,32,25,24	SDRAM(12:15) (Active / Inactive)
2	1	22,21,19,18	SDRAM(8:11) (Active / Inactive)
1	1	39,38,36,35	SDRAM(4:7) (Active / Inactive)
0	1	44,43,41,40	SDRAM(0:3) (Active / Inactive)

8.3.5 Register 4: Reserved Register (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	X	-	Latched FS0#
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	x	-	Latched FS1#
2	1	-	Reserved
1	x	-	Latched FS3#
0	1	-	Reserved

8.3.6 Register 5: Peripheral Control (1 = enable, 0 = Stopped)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	X	-	Latched FS2#
5	1	-	Reserved
4	1	54	IOAPIC _F(Active / Inactive)
3	1	55	IOAPIC0 (Active / Inactive)
2	1	-	Reserved
1	1	2	REF1 (Active / Inactive)
0	1	3	REF0 (Active / Inactive)

9.0 SPECIFICATIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in this table may cause permanent damage to the device. Precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. Subjection to maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level (Ground or Vdd).

Symbol	Parameter	Rating
Vdd , V_{IN}	Voltage on any pin with respect to GND	- 0.5 V to + 7.0 V
T_{STG}	Storage Temperature	- 65°C to + 150°C
T_B	Ambient Temperature	- 55°C to + 125°C
T_A	Operating Temperature	0°C to + 70°C

9.2 AC CHARACTERISTICS

Vddq4 = Vddq3 = Vddq2 = Vddq1=3.3V – 5 %, VddL1=VddL2 = 2.375V~2.9V , T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Output Duty Cycle		45	50	55	%	Measured at 1.5V
CPU/SDRAM to PCI Offset	t_{OFF}	1		4	ns	15 pF Load Measured at 1.5V
Skew (CPU-CPU), (PCI-PCI), (SDRAM-SDRAM)	t_{SKEW}			250	ps	15 pF Load Measured at 1.5V
CPU/SDRAM Cycle to Cycle Jitter	t_{CCJ}			¡Ó250	ps	
CPU/SDRAM Absolute Jitter	t_{JA}			500	ps	
Jitter Spectrum 20 dB Bandwidth from Center	BW_J			500	KHz	
Output Rise (0.4V ~ 2.0V) & Fall (2.0V ~0.4V) Time	t_{TLH} t_{THL}	0.4		1.6	ns	15 pF Load on CPU and PCI outputs
Overshoot/Undershoot Beyond Power Rails	V_{over}	0.7		1.5	V	22 Ω at source of 8 inch PCB run to 15 pF load
Ring Back Exclusion	V_{RBE}	0.7		2.1	V	Ring Back must not enter this range.

9.3 DC CHARACTERISTICS

Vddq4 = Vddq3 = Vddq2 = Vddq1=3.3V – 5 %, VddL1=VddL2 = 2.375V~2.9V , T_A = 0°C to +70°C						
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input Low Voltage	V_{IL}			0.8	V_{dc}	
Input High Voltage	V_{IH}	2.0			V_{dc}	
Input Low Current	I_{IL}			-66	µA	
Input High Current	I_{IH}			5	µA	
Output Low Voltage I_{OL} = 4 mA	V_{OL}			0.4	V_{dc}	All outputs
Output High Voltage I_{OH} = 4mA	V_{OH}	2.4			V_{dc}	All outputs using 3.3V power
Tri-State leakage Current	Ioz			10	µA	
Dynamic Supply Current for Vdd + Vddq3	I_{dd3}				mA	CPU = 66.6 MHz PCI = 33.3 Mhz with load
Dynamic Supply Current for Vddq2 + Vddq2b	I_{dd2}				mA	Same as above
CPU Stop Current for Vdd + Vddq3	I_{CPUS3}				mA	Same as above
CPU Stop Current for Vddq2 + Vddq2b	I_{CPUS2}				mA	Same as above
PCI Stop Current for Vdd + Vddq3	I_{PD3}				mA	

9.4 BUFFER CHARACTERISTICS

9.4.1 TYPE 1 BUFFER FOR CPU CLOCK

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-27			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-27	mA	Vout = 2.0V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.2 V
Pull-Down Current Max	$I_{OL(max)}$			27	mA	Vout = 0.3 V
Rise/Fall Time Min Between 0.4 V and 2.0 V	$T_{RF(min)}$	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.4 V and 2.0 V	$T_{RF(max)}$			1.6	ns	20pF Load

9.4.2 TYPE 2 BUFFER FOR IOAPIC

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$				mA	Vout = 1.4 V
Pull-Up Current Max	$I_{OH(max)}$			-29	mA	Vout = 2.7 V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.0 V
Pull-Down Current Max	$I_{OL(max)}$			28	mA	Vout = 0.2 V
Rise/Fall Time Min Between 0.7 V and 1.7 V	$T_{RF(min)}$	0.4			ns	10pF Load
Rise/Fall Time Max Between 0.7 V and 1.7 V	$T_{RF(max)}$			1.8	ns	20pF Load

9.4.3 TYPE 3 BUFFER FOR REF1, 24MHZ, 48MHZ

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-29			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-23	mA	Vout = 3.135V
Pull-Down Current Min	$I_{OL(min)}$	29			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$				mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	1.0			ns	10pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			4.0	ns	20pF Load

9.4.4 TYPE 4 BUFFER FOR SDRAM (0:15)

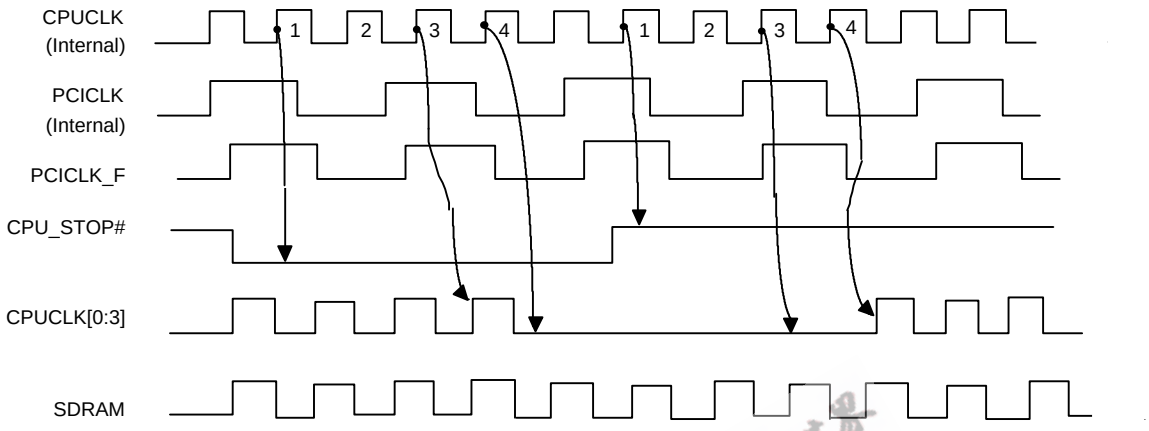
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$				mA	Vout = 1.65 V
Pull-Up Current Max	$I_{OH(max)}$			-46	mA	Vout = 3.135 V
Pull-Down Current Min	$I_{OL(min)}$				mA	Vout = 1.65 V
Pull-Down Current Max	$I_{OL(max)}$			53	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	20pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			1.3	ns	30pF Load

9.4.5 TYPE 5 BUFFER FOR PCICLK(0:5,F)

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Pull-Up Current Min	$I_{OH(min)}$	-33			mA	Vout = 1.0 V
Pull-Up Current Max	$I_{OH(max)}$			-33	mA	Vout = 3.135 V
Pull-Down Current Min	$I_{OL(min)}$	30			mA	Vout = 1.95 V
Pull-Down Current Max	$I_{OL(max)}$			38	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.8 V and 2.0 V	$T_{RF(min)}$	0.5			ns	15pF Load
Rise/Fall Time Max Between 0.8 V and 2.0 V	$T_{RF(max)}$			2.0	ns	30pF Load

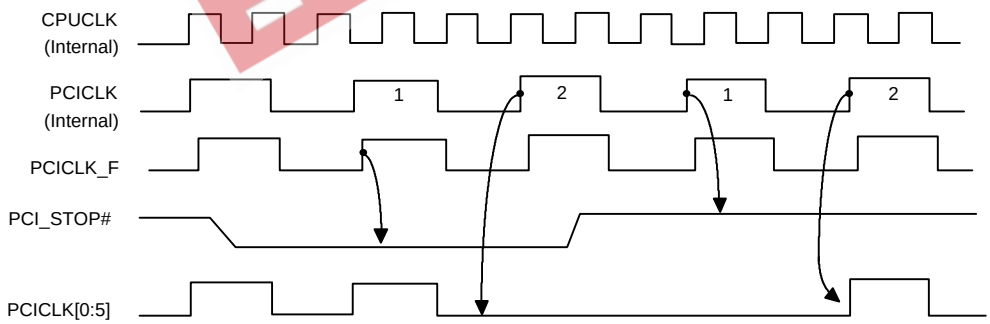
10.0 POWER MANAGEMENT TIMING

10.1 CPU_STOP# Timing Diagram



For synchronous Chipset, CPU_STOP# pin is an asynchronous " active low " input pin used to stop the CPU clocks for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the CPU clocks are stopped. The CPU clocks will always be stopped in a low state and resume output with full pulse width. In this case, CPU "clocks on latency" is less than 4 CPU clocks and "clocks off latency" is less then 4 CPU clocks.

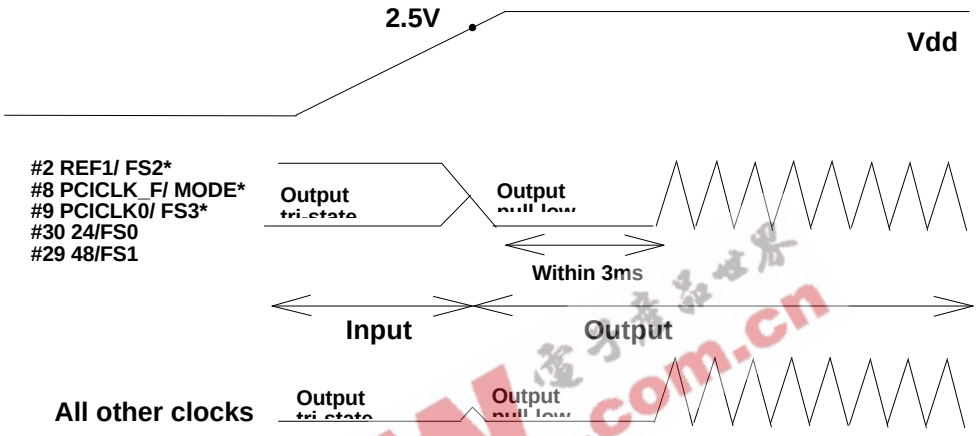
10.2 PCI_STOP# Timing Diagram



For synchronous Chipset, PCI_STOP# pin is an asynchronous "active low" input pin used to stop the PCICLK [0:5] for low power operation. This pin is asserted synchronously by the external control logic at the rising edge of free running PCI clock(PCICLK_F). All other clocks will continue to run while the PCI clocks are stopped. The PCI clocks will always be stopped in a low state and resume output with full pulse width. In this case, PCI "clocks on latency" is less than 2 PCI clocks and "clocks off latency" is less then 2 PCI clocks.

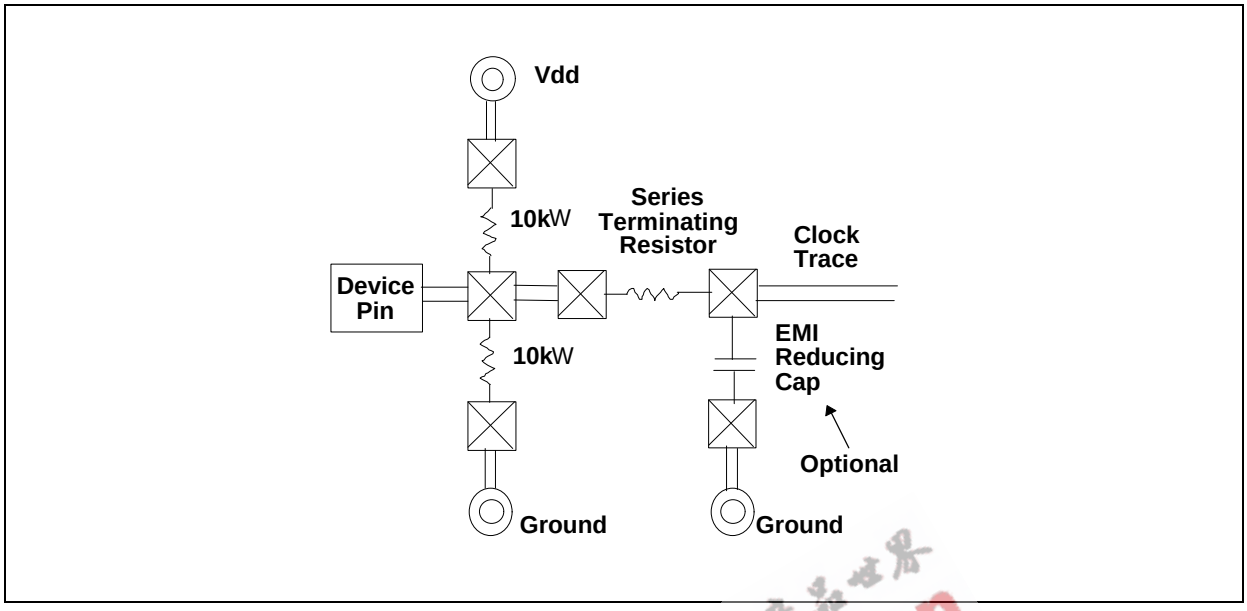
11.0 OPERATION OF DUAL FUCTION PINS

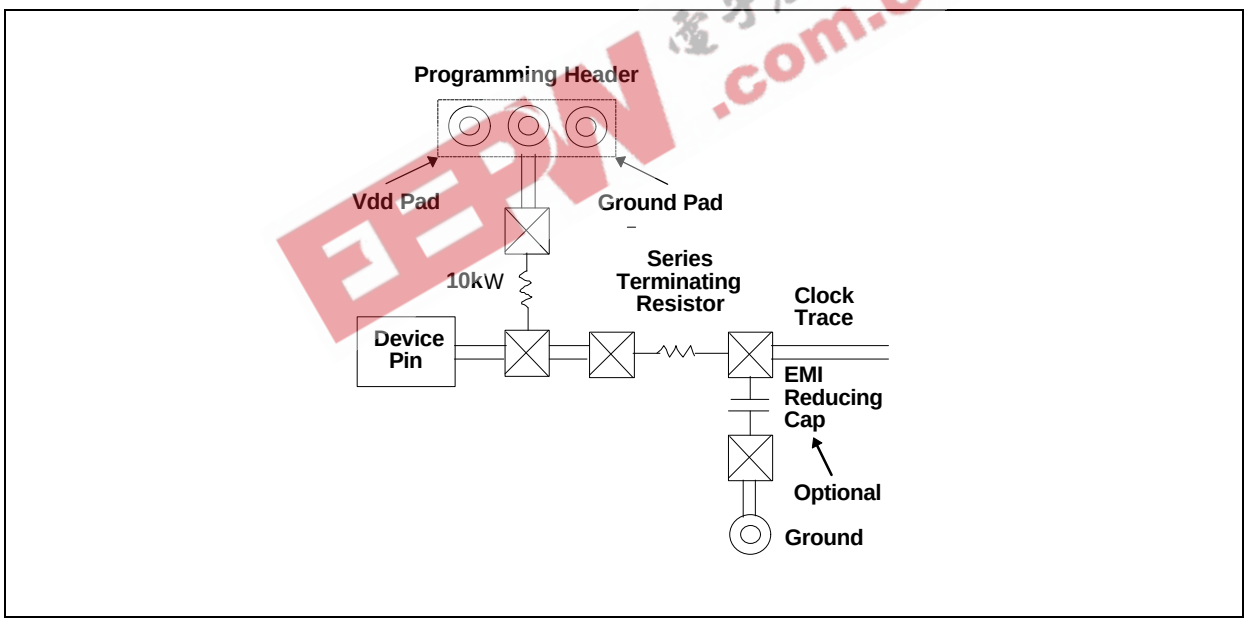
Pins 2,8, 9, 29,30 are dual function pins and are used for selecting different functions in this device (see Pin description). During power up, these pins are in input mode (see Fig1), therefore, and are considered input select pins. When Vdd reaches 2.5V, the logic level that is present on these pins is latched into their appropriate internal registers. Once the correct information is properly latched, these pins will change into output pins and will be pulled low by default. At the end of the power up timer (within 3 ms) outputs starts to toggle at the specified frequency.



Each of these pins has a large pull-up resistor (250 kΩ @3.3V) inside. The default state will be logic 1, but the internal pull-up resistor may be too large when long traces or heavy load appear on these dual function pins. Under these conditions, an external 10 kΩ resistor is recommended to be connected to Vdd if logic 1 is expected. Otherwise, there should be direct connection to ground if a logic 0 is desired. The 10 kΩ resistor should be placed before the serious terminating resistor. Note that these logic will only be latched at initial power on.

If optional EMI reducing capacitor are needed, they should be placed as close to the series terminating resistor as possible and after the series terminating resistor. These capacitors have typical values ranging from 4.7pF to 22pF.

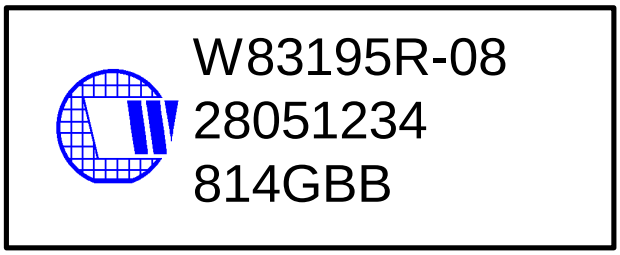

Vdd
10kW
Series Terminating Resistor
Clock Trace
Device Pin
10kW
EMI Reducing Cap
Optional
Ground
Ground


Programming Header
Vdd Pad
Ground Pad
10kW
Series Terminating Resistor
Clock Trace
Device Pin
EMI Reducing Cap
Optional
Ground

13.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83195R-08	56 PIN SSOP	Commercial, 0°C to +70°C

14.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83195R-08

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

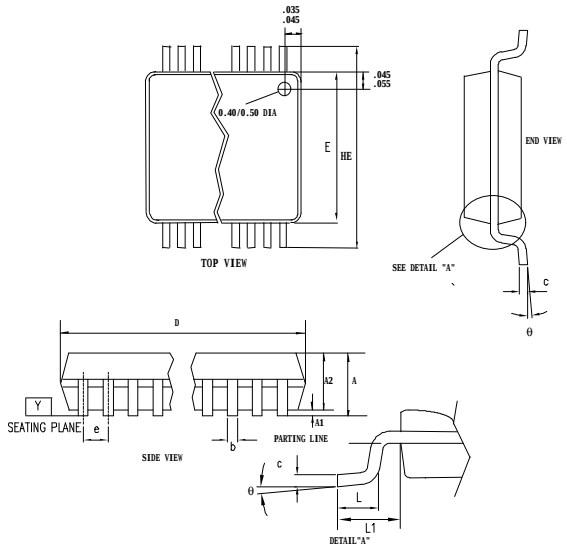
3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

G: assembly house ID; A means ASE, S means SPIL, G means GR

BB: IC revision

15.0 PACKAGE DRAWING AND DIMENSIONS



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	2.41	2.57	2.79	0.095	0.101	0.110
A1	0.20	0.30	0.41	0.008	0.012	0.016
A2	2.24	2.29	2.34	0.088	0.090	0.092
b	0.20	0.25	0.34	0.008	0.010	0.0135
c	0.13	—	0.25	0.005	—	0.010
D	18.2	18.42	18.54	0.720	0.725	0.730
H_E	10.16	10.31	10.41	0.400	0.406	0.410
E	7.42	7.52	7.59	0.292	0.296	0.299
e	0.51	0.64	0.76	0.020	0.025	0.030
L	0.61	0.81	1.02	0.024	0.032	0.040
L1	—	1.40	—	—	0.055	—
Y	—	—	0.08	—	—	0.003
q	0	—	8	0	—	8

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