WM8775

24-bit, 96kHz ADC with 4 Channel I/P Multiplexer

DESCRIPTION

The WM8775 is a high performance, stereo audio ADC with a 4 channel input mixer. The WM8775 is ideal for digitising multiple analogue sources for surround sound processing applications for home hi-fi, automotive and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used with a four stereo channel input selector. Each channel has programmable gain control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

The audio data interface supports I^2S, left justified, right justified and DSP digital audio formats.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including channel selection, volume controls, mutes, de-emphasis and power management facilities.

The device is available in a 28-lead SSOP package. The WM8775 is software compatible with the WM8776.

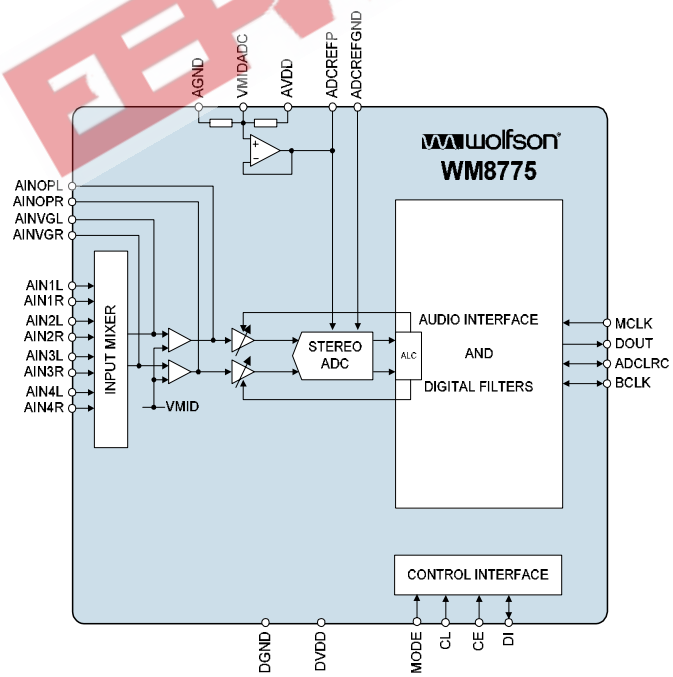
FEATURES

- Audio Performance
  - 102dB SNR ('A' weighted @ 48kHz)
  - -90dB THD
- ADC Sampling Frequency: 32kHz – 96kHz
- Four stereo ADC inputs with analogue gain adjust from +24dB to –21dB in 0.5dB steps
- Digital gain adjust from -21.5dB to -103dB.
- Programmable Automatic Level Control (ALC) or Limiter on ADC input
- 3-Wire SPI Compatible or 2-wire Serial Control Interface
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- Automotive Audio

BLOCK DIAGRAM



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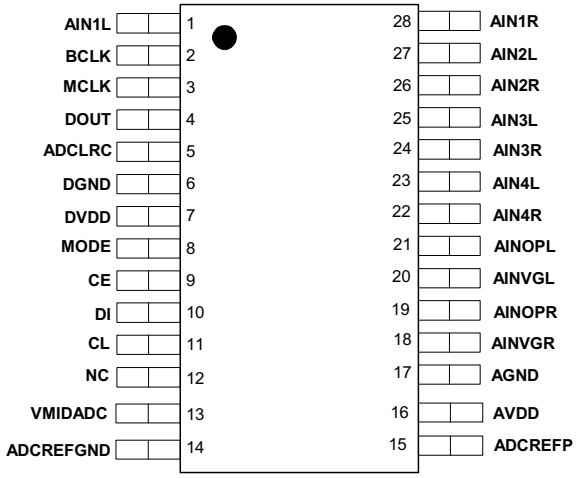
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8775SEDS	-25 to +85°C	28-lead SSOP (Pb-free)	MSL1	260°C
WM8775SEDS/R	-25 to +85°C	28-lead SSOP (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AIN1L	Analogue Input	Channel 1 left input multiplexor virtual ground
2	BCLK	Digital input/output	ADC audio interface bit clock
3	MCLK	Digital input	Master ADC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
4	DOUT	Digital output	ADC data output
5	ADCLRC	Digital input/output	ADC left/right word clock
6	DGND	Supply	Digital negative supply
7	DVDD	Supply	Digital positive supply
8	MODE	Digital Input	Serial Interface Mode select
9	CE	Digital Input	Serial Interface Latch signal
10	DI	Digital input/output	Serial interface data
11	CL	Digital input	Serial interface clock
12		NC	No connection
13	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
14	ADCREFGND	Supply	ADC negative supply and substrate connection
15	ADCREFP	Analogue Output	ADC positive reference decoupling pin; 10uF external decoupling
16	AVDD	Supply	Analogue positive supply
17	AGND	Supply	Analogue negative supply and substrate connection
18	AINVGR	Analogue Input	Right channel multiplexor virtual ground
19	AINOPR	Analogue Output	Right channel multiplexor output
20	AINVGL	Analogue Input	Left channel multiplexor virtual ground
21	AINOPL	Analogue Output	Left channel multiplexor output
22	AIN4R	Analogue Input	Channel 4 right input multiplexor virtual ground
23	AIN4L	Analogue Input	Channel 4 left input multiplexor virtual ground
24	AIN3R	Analogue Input	Channel 3 right input multiplexor virtual ground
25	AIN3L	Analogue Input	Channel 3 left input multiplexor virtual ground
26	AIN2R	Analogue Input	Channel 2 right input multiplexor virtual ground
27	AIN2L	Analogue Input	Channel 2 left input multiplexor virtual ground
28	AIN1R	Analogue Input	Channel 1 right input multiplexor virtual ground

Note : Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (MCLK, ADCLRC, BCLK, DI, CL, CE and MODE)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD		2.7		5.5	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: Digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}=1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		Vrms
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 48kHz	97	102		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 96kHz 64xOSR		99		dB
Dynamic Range (note 2)		A-weighted, -60dB full scale input		102		dB
Total Harmonic Distortion (THD)		1 kHz, 0dBFs		-92		dB
		1kHz, -1dBFs		-95	-85	dB
ADC Channel Separation		1kHz Input		90		dB
Programmable Gain Step Size			0.25	0.5	0.75	dB
Programmable Gain Range (Analogue)		1kHz Input	-21		+24	dB
Programmable Gain Range (Digital)		1kHz Input	-82		+0	dB
Analogue Mute Attenuation (Note 5)		1kHz Input, 0dB gain		76		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Supply Current						
Analogue supply current		AVDD = 5V		48		mA
Digital supply current		DVDD = 3.3V		4.5		mA

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
4. All performance measurement done using certain timing conditions (please refer to section 'Digital Audio Interface').
5. A full digital MUTE can be achieved if the ADC gain (LAG/RAG) is set to minimum.

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

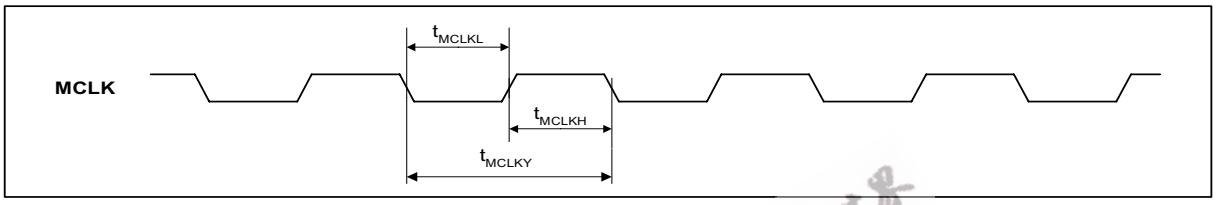


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK System clock pulse width high	t_{MCLKH}		11			ns
MCLK System clock pulse width low	t_{MCLKL}		11			ns
MCLK System clock cycle time	t_{MCLKY}		28		1000	ns
MCLK Duty cycle			40:60		60:40	
Power-saving mode activated		After MCLK stopped	2		10	µs
Normal mode resumed		After MCLK re-started	0.5		1	MCLK cycle

Table 1 Master Clock Timing Requirements

Note:

If MCLK period is longer than maximum specified above, power-saving mode is entered. In this power-saving mode, all registers will retain their values and can be accessed in the normal manner through the control interface.

DIGITAL AUDIO INTERFACE – MASTER MODE

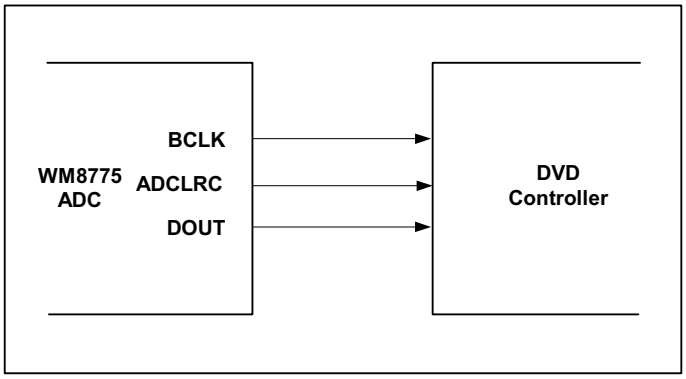


Figure 2 Audio Interface - Master Mode

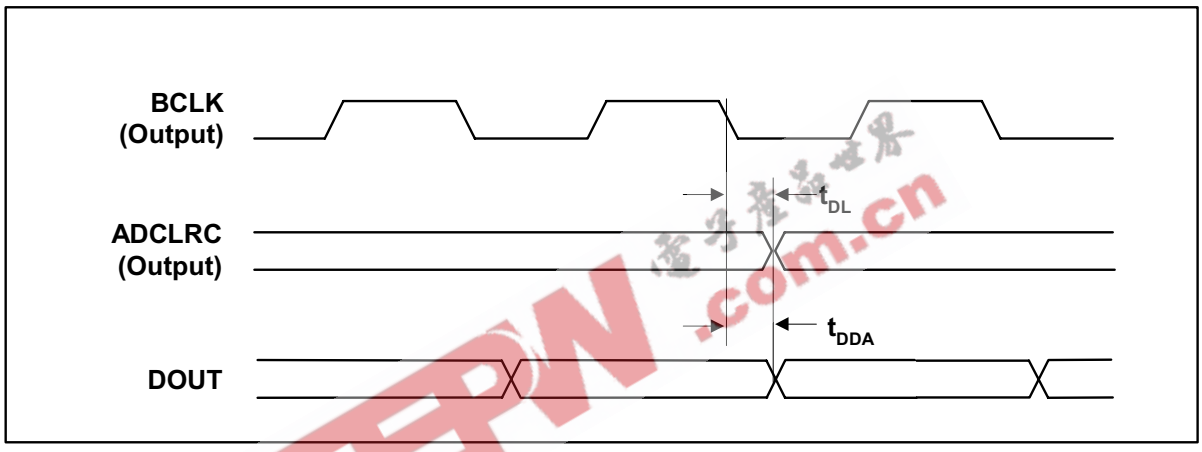


Figure 3 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND=0V, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCLRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
DOUT propagation delay from BCLK falling edge	t_{DDA}		0		10	ns

Table 2 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

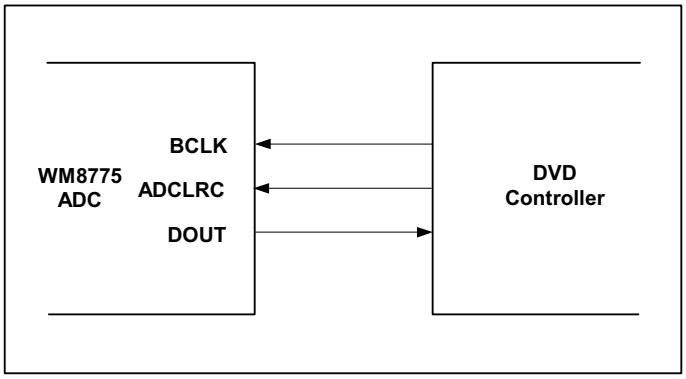


Figure 4 Audio Interface – Slave Mode

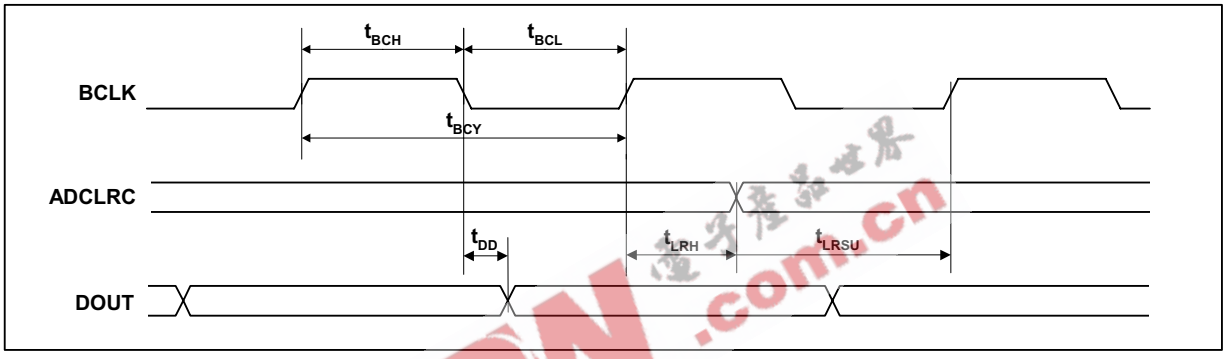


Figure 5 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
ADCLRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
ADCLRC hold time from BCLK rising edge	t_{LRH}		10			ns
DOUT propagation delay from BCLK falling edge	t_{DD}		0		10	ns

Table 3 Digital Audio Data Timing – Slave Mode

Note:

ADCLRC should be synchronous with MCLK, although the WM8775 interface is tolerant of phase variations or jitter on these signals.

3-WIRE MPU INTERFACE TIMING

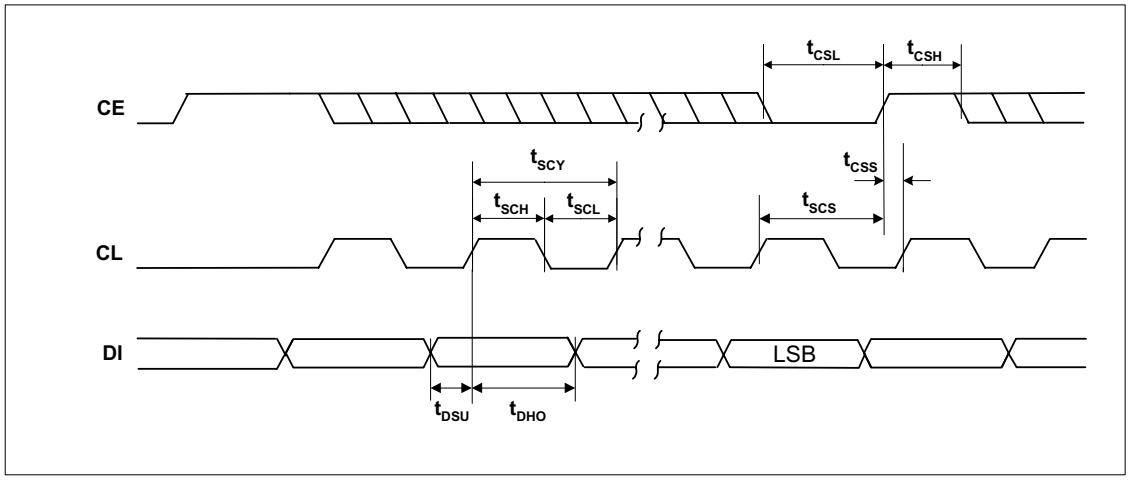


Figure 6 SPI Compatible Control Interface Input Timing (MODE=1)

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CL rising edge to CE rising edge	t_{SCS}	60			ns
CL pulse cycle time	t_{SCY}	80			ns
CL pulse width low	t_{SCL}	30			ns
CL pulse width high	t_{SCH}	30			ns
DI to CL set-up time	t_{DSU}	20			ns
CL to DI hold time	t_{DHO}	20			ns
CE pulse width low	t_{CSL}	20			ns
CE pulse width high	t_{CSH}	20			ns
CE rising to CL rising	t_{CSS}	20			ns

Table 4 3-Wire SPI Compatible Control Interface Input Timing Information

2-WIRE MPU INTERFACE TIMING

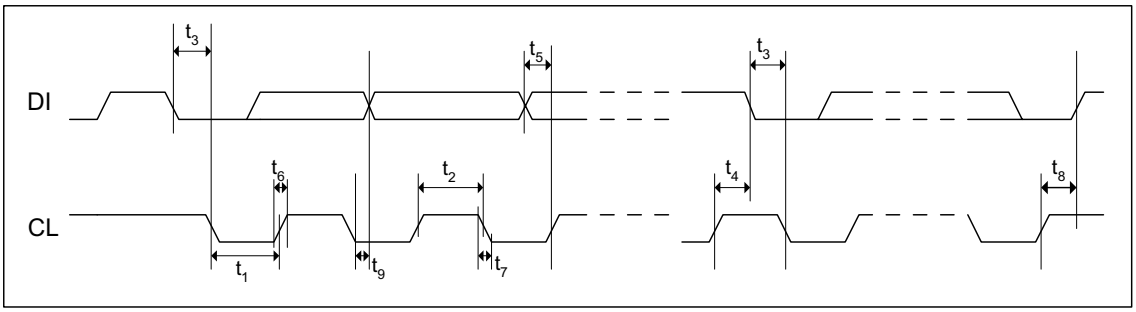


Figure 7 Control Interface Timing – 2-Wire Serial Control Mode (MODE=0)

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
CL Frequency		0		526	kHz
CL Low Pulse-Width	t_1	1.3			us
CL High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
DI, CL Rise Time	t_6			300	ns
DI, CL Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

Table 5 2-Wire Control Interface Timing Information

INTERNAL POWER ON RESET CIRCUIT

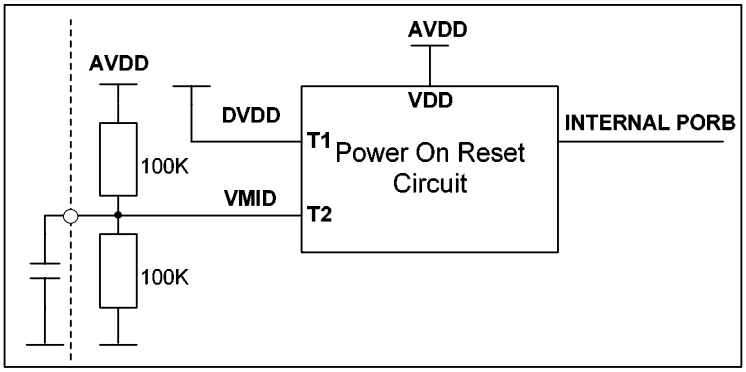


Figure 8 Internal Power on Reset Circuit Schematic

The WM8775 includes an internal Power on Reset Circuit which is used reset the digital logic into a default state after power up.

Figure 8 shows a schematic of the internal POR circuit. The POR circuit is powered from AVDD. The circuit monitors DVDD and VMID and asserts PORB low if DVDD or VMID are below the minimum threshold Vpor_off.

On power up, the POR circuit requires AVDD to be present to operate. PORB is asserted low until AVDD and DVDD and VMID are established. When AVDD, DVDD, and VMID have been established, PORB is released high, all registers are in their default state and writes to the digital interface may take place.

On power down, PORB is asserted low whenever DVDD or VMID drop below the minimum threshold Vpor_off.

If AVDD is removed at any time, the internal Power on Reset circuit is powered down and PORB will follow AVDD.

In most applications the time required for the device to release PORB high will be determined by the charge time of the VMID node.

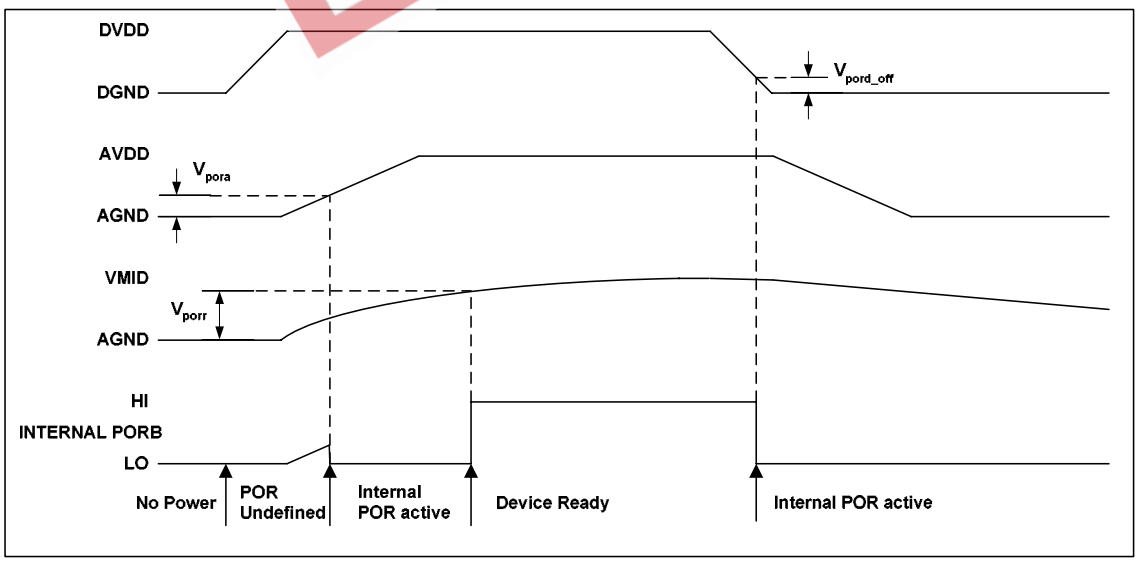


Figure 9 Typical Power up Sequence where DVDD is Powered before AVDD

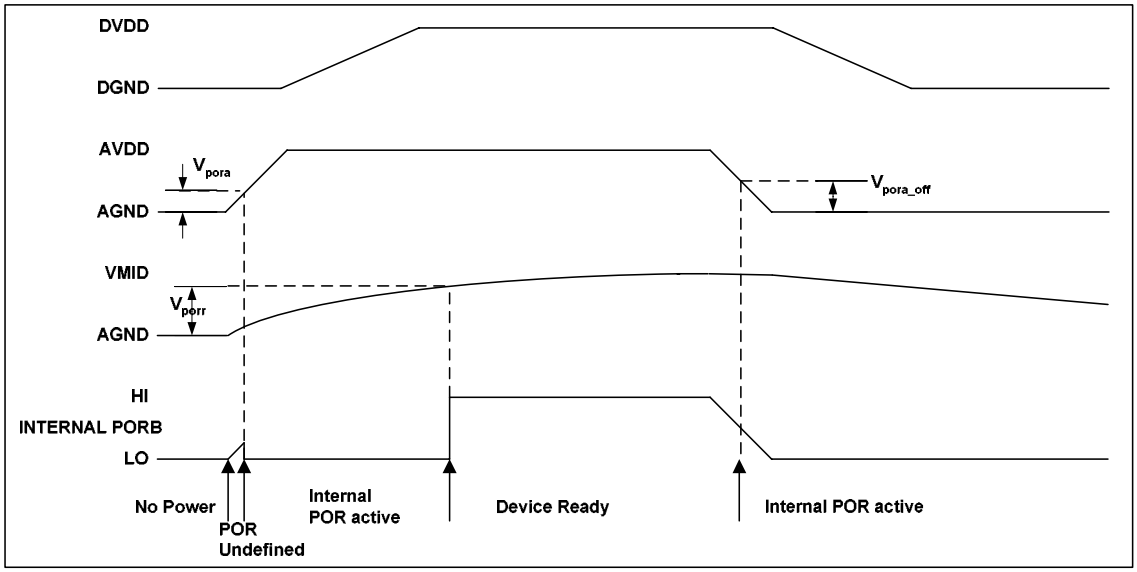


Figure 10 Typical Power up Sequence where AVDD is Powered before DVDD

Typical POR Operation (typical values, not tested)

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.5	0.7	1.0	V
V_{porr}	0.5	0.7	1.1	V
V_{pora_off}	1.0	1.4	2.0	V
V_{pord_off}	0.6	0.8	1.0	V

In a real application the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. Using the POR circuit to monitor VMID ensures a reasonable delay between applying power to the device and Device Ready.

Figure 9 and Figure 10 show typical power up scenarios in a real system. Both AVDD and DVDD must be established and VMID must have reached the threshold Vporr before the device is ready and can be written to. Any writes to the device before Device Ready will be ignored.

Figure 9 shows DVDD powering up before AVDD. Figure 10 shows AVDD powering up before DVDD. In both cases, the time from applying power to Device Ready is dominated by the charge time of VMID.

A 10uF cap is recommended for decoupling on VMID. The charge time for VMID will dominate the time required for the device to become ready after power is applied. The time required for VMID to reach the threshold is a function of the VMID resistor string and the decoupling capacitor. The Resistor string has an typical equivalent resistance of 50kΩ (+/-20%). Assuming a 10uF capacitor, the time required for VMID to reach threshold of 1V is approx 110ms.

DEVICE DESCRIPTION

INTRODUCTION

WM8775 is a stereo audio ADC, with a flexible four input multiplexor. It is available in a single package and controlled by either a 3-wire or a 2-wire interface.

The input multiplexor to the ADC is configured to allow large signal levels to be input to the ADC, using external resistors to reduce the amplitude of larger signals to within the normal operating range of the ADC. The ADC has an analogue input PGA and a digital gain control, accessed by one register write. The input PGA allows input signals to be gained up to +24dB and attenuated down to -21dB in 0.5dB steps. The digital gain control allows attenuation from -21.5dB to -103dB in 0.5dB steps. This allows the user maximum flexibility in the use of the ADC.

The Audio Interface may be configured to operate in either master or slave mode. In Slave mode ADCLRC and BCLK are all inputs. In Master mode ADCLRC and BCLK are outputs. The audio data interface supports right, left and I^2S interface formats along with a highly flexible DSP serial port interface. Operation using system clock of 256fs, 384fs, 512fs or 768fs is provided. In Slave mode selection between clock rates is automatically controlled. In master mode the master clock to sample rate ratio is set by control bit ADCRATE. Master clock sample rates (fs) from less than 32kHz up to 96kHz are allowed, provided the appropriate system clock is input.

Control of internal functionality of the device is by 3-wire SPI compatible or 2-wire serial control interface. Either interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC.

The master clock for WM8775 supports ADC audio sampling rates from 256fs to 768fs, where fs is the audio sampling frequency (ADCLRC) typically 32kHz, 44.1kHz, 48kHz or 96kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode, the WM8775 has a master detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks). If there is a greater than 32 clocks error the interface is disabled and maintains the output level at the last sample. The master clock must be synchronised with ADCLRC, although the WM8775 is tolerant of phase variations or jitter on this clock. Table 6 shows the typical master clock frequency inputs for the WM8775.

The signal processing for the WM8775 typically operates at an oversampling rate of 128fs. For ADC operation at 96kHz, it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs.

SAMPLING RATE (ADCLRC)	System Clock Frequency (MHz)			
	256fs	384fs	512fs	768fs
32kHz	8.192	12.288	16.384	24.576
44.1kHz	11.2896	16.9340	22.5792	33.8688
48kHz	12.288	18.432	24.576	36.864
96kHz	24.576	36.864	Unavailable	Unavailable

Table 6 System Clock Frequencies Versus Sampling Rate

In Master mode BCLK and ADCLRC are generated by the WM8775. The frequency of ADCLRC is set by setting the required ratio of MCLK to ADCLRC using the ADCRATE control bit (Table 7).

ADCRATE[2:0]	MCLK:ADCLRC RATIO
010	256fs
011	384fs
100	512fs
101	768fs

Table 7 Master Mode MCLK:ADCLRC Ratio Select

Table 8 shows the settings for ADCRATE for common sample rates and MCLK frequencies.

SAMPLING RATE (ADCLRC)	System Clock Frequency (MHz)			
	256fs	384fs	512fs	768fs
	ADCRATE =010	ADCRATE =011	ADCRATE =100	ADCRATE =101
32kHz	8.192	12.288	16.384	24.576
44.1kHz	11.2896	16.9340	22.5792	33.8688
48kHz	12.288	18.432	24.576	36.864
96kHz	24.576	36.864	Unavailable	Unavailable

Table 8 Master Mode ADCLRC Frequency Selection

BCLK is also generated by the WM8775. The frequency of BCLK depends on the mode of operation. If using 256, 384, 512 or 768fs (ADCRATE=010, 011,100 or 101) BCLK = MCLK/4. However if DSP mode is selected as the audio interface mode then BCLK=MCLK.

POWERDOWN MODES

The WM8775 has powerdown control bits allowing specific parts of the WM8775 to be powered off when not being used. The 4-channel input source selector and input buffer may be powered down using control bit AINPD. When AINPD is set all inputs to the source selector (AIN1I/R to AIN4L/R) are switched to a buffered VMIDADC. Control bit ADCPD powers off the ADC and also the ADC input PGAs. Setting AINPD and ADCPD will powerdown everything except the references VMIDADC and ADCREFP. These may be powered down by setting PDWN. Setting PDWN will override all other powerdown control bits. It is recommended that the 4-channel input mux and buffer AINPD and ADCPD are powered down before setting PDWN. The default is for all powerdown bits to be 0 i.e. enabled.

DIGITAL AUDIO INTERFACE

MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the MS control bit. In both Master and Slave modes ADCDAT is always an output. The default is Slave mode.

In Slave mode (MS=0) ADCLRC and BCLK are inputs to the WM8775 (Figure 11). ADCLRC is sampled by the WM8775 on the rising edge of BCLK. ADC data is output on DOUT and changes on the falling edge of BCLK. By setting control bit BCLKINV the polarity of BCLK may be reversed so that ADCLRC is sampled on the falling edge of BCLK and DOUT changes on the rising edge of BCLK.

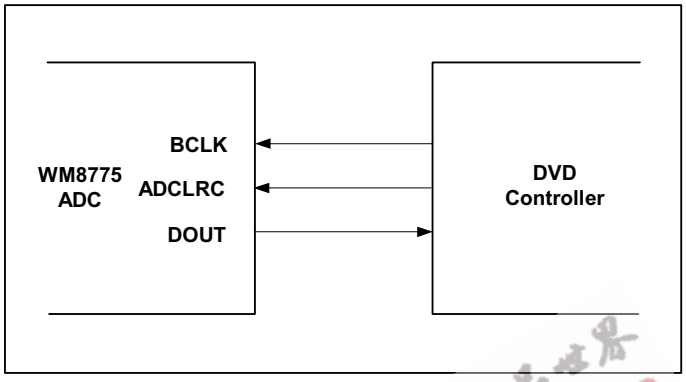


Figure 11 Slave Mode

In Master mode (MS=1) ADCLRC and BCLK are outputs from the WM8775 (Figure 12). ADCLRC and BITCLK are generated by the WM8775. ADCDAT is output on DOUT and changes on the falling edge of BCLK. By setting control bit BCLKINV, the polarity of BCLK may be reversed so that DOUT changes on the rising edge of BCLK.

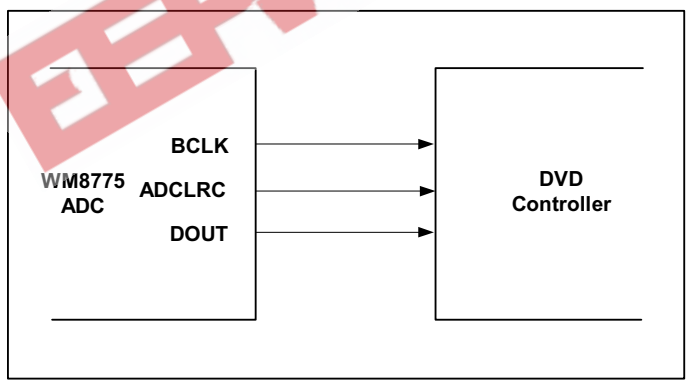


Figure 12 Master Mode

AUDIO INTERFACE FORMATS

Audio data output from the ADC filters, via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP Mode A
- DSP Mode B

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and I^2S modes, the digital audio interface outputs ADC data on DOUT. Audio Data for each stereo channel is time multiplexed with ADCLRC indicating whether the left or right channel is present. ADCLRC is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I^2S modes, the minimum number of BCLKs per ADCLRC period is 2 times the selected word length. ADCLRC must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on ADCLRC is acceptable provided the above requirements are met.

In DSP Mode A or B, the ADC data may also be output, with ADCLRC used as a frame sync to identify the MSB of the first word. The minimum number of BCLKs per ADCLRC period is 2 times the selected word length

LEFT JUSTIFIED MODE

In left justified mode, the MSB of the ADC data is output on DOUT and changes on the same falling edge of BCLK as ADCLRC and may be sampled on the rising edge of BCLK. ADCLRC is high during the left samples and low during the right samples (Figure 13).

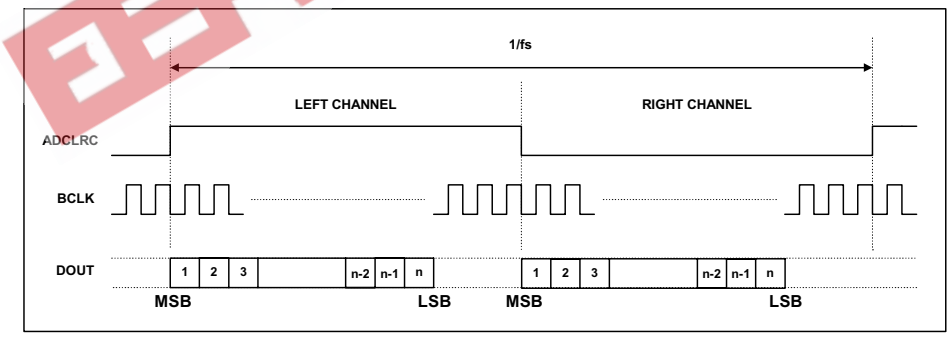


Figure 13 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB of the ADC data is output on DOUT and changes on the falling edge of BCLK preceding a ADCLRC transition and may be sampled on the rising edge of BCLK. ADCLRC is high during the left samples and low during the right samples (Figure 14).

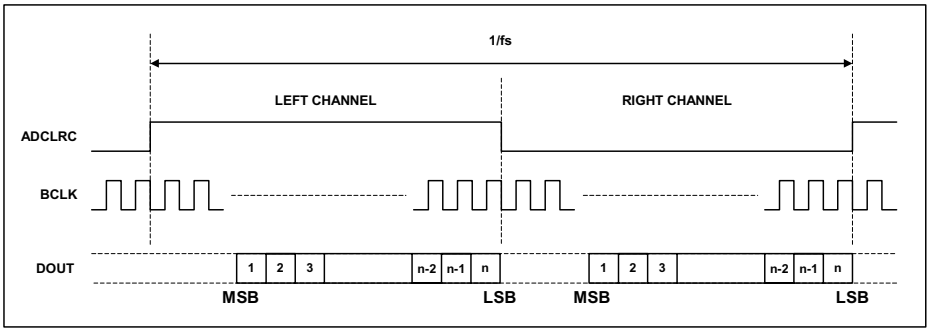


Figure 14 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB of the ADC data is output on DOUT and changes on the first falling edge of BCLK following an ADCLRC transition and may be sampled on the rising edge of BCLK. ADCLRC is low during the left samples and high during the right samples.

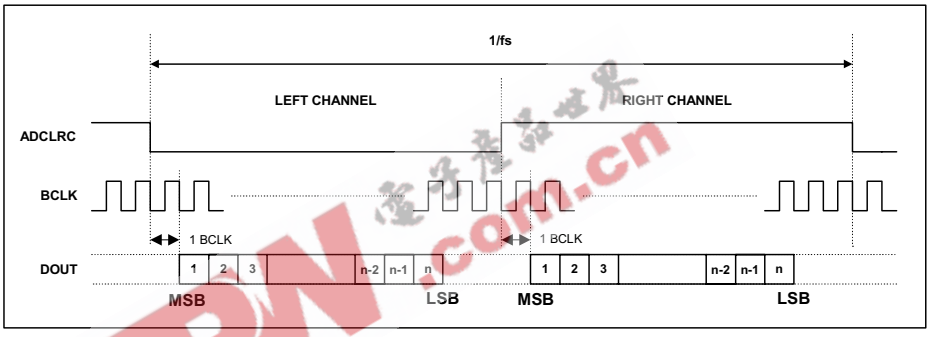


Figure 15 I²S Mode Timing Diagram

DSP MODE

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 16 and Figure 17. In device slave mode, Figure 18 and Figure 19, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

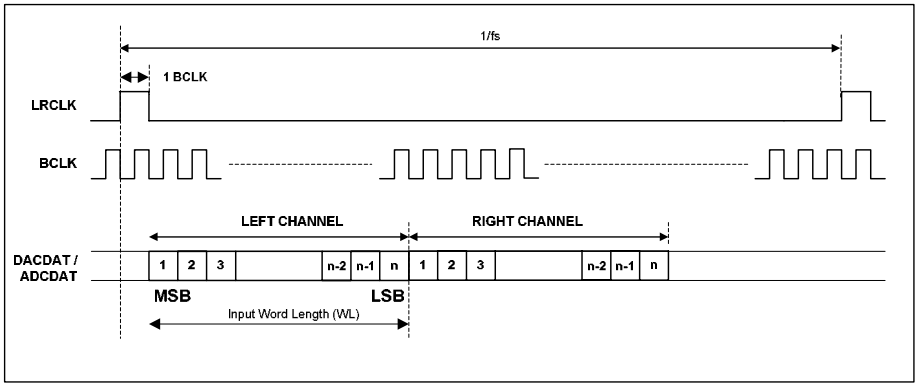


Figure 16 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

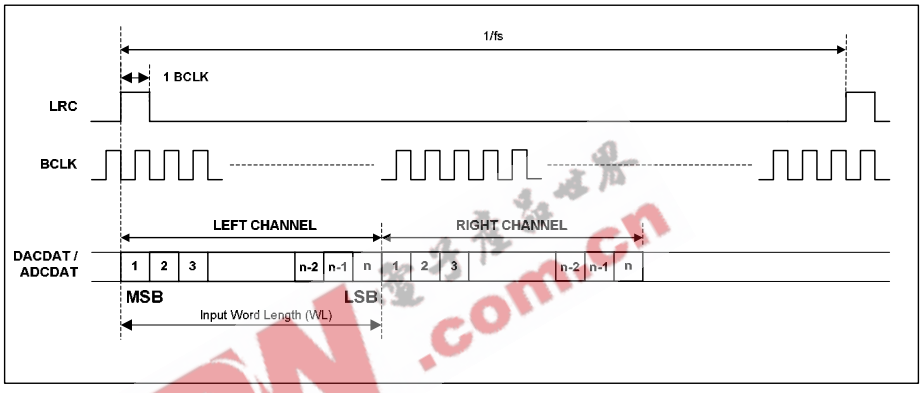


Figure 17 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

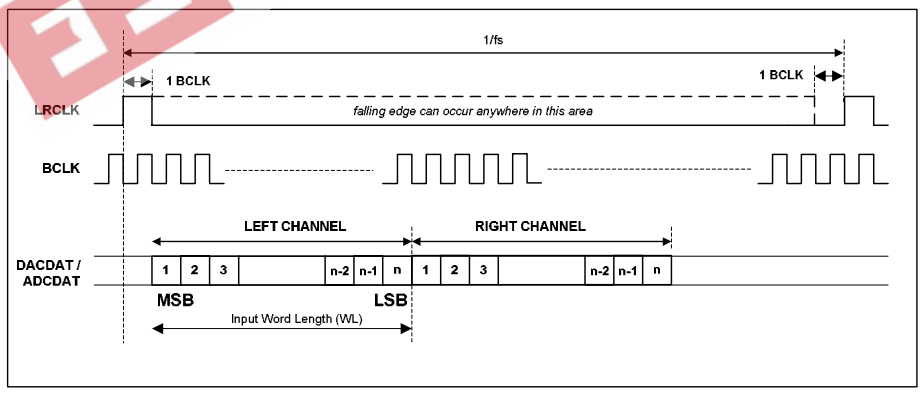


Figure 18 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

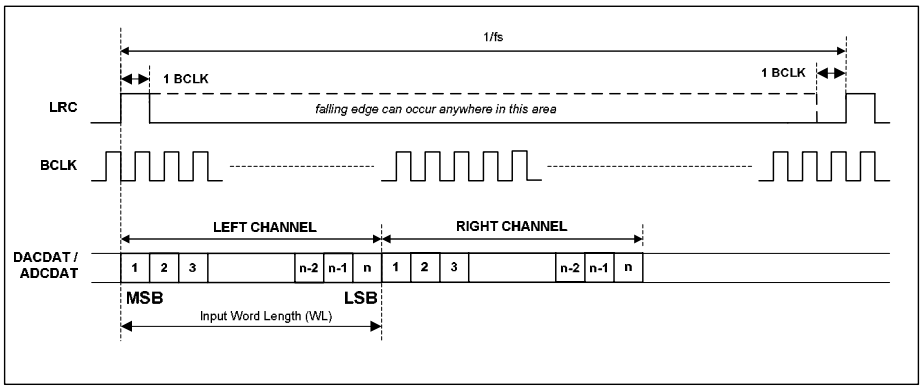


Figure 19 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

CONTROL INTERFACE OPERATION

The WM8775 is controlled using a 3-wire serial interface in a SPI compatible configuration or a 2-wire serial interface mode. The interface type is selected by the MODE pin as shown in Table 9.

MODE	Control Mode
0	2 wire interface
1	3 wire interface

Table 9 Control Interface Selection via MODE pin

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

DI is used for the program data, CL is used to clock in the program data and CE is used to latch the program data. DI is sampled on the rising edge of CL. The 3-wire interface protocol is shown in Figure 20.

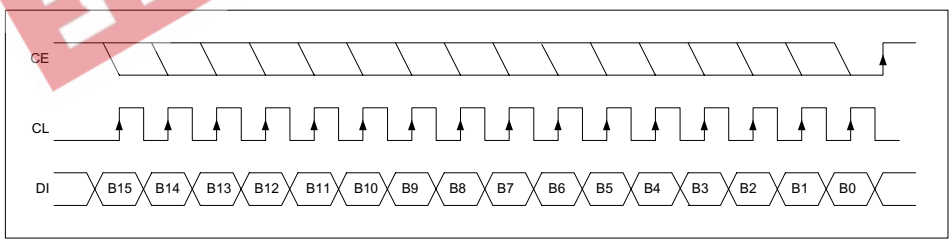


Figure 20 3-Wire SPI Compatible Interface

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CE is edge sensitive – the data is latched on the rising edge of CE.

2-WIRE SERIAL CONTROL MODE

The WM8775 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8775).

The WM8775 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on DI while CL remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on DI (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8775 and the R/W bit is '0', indicating a write, then the WM8775 responds by pulling DI low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8775 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8775 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8775 register address plus the first bit of register data). The WM8775 then acknowledges the first data byte by pulling DI low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8775 acknowledges again by pulling DI low.

The transfer of data is complete when there is a low to high transition on DI while CL is high. After receiving a complete address and data sequence the WM8775 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. DI changes while CL is high), the device jumps to the idle condition.

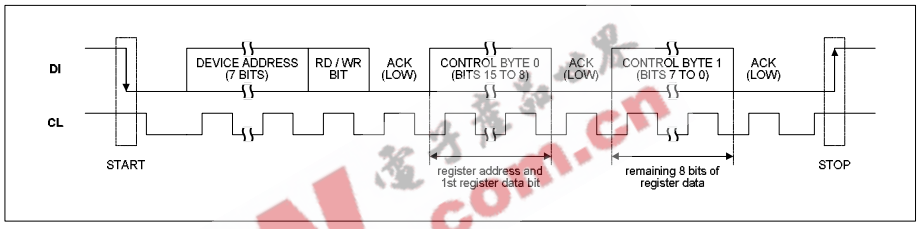


Figure 21 2-Wire Serial Interface

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

The WM8775 has two possible device addresses, which can be selected using the CE pin.

CE STATE	DEVICE ADDRESS
Low	0011010 (0 x 34h)
High	0011011 (0 x 36h)

Table 10 2-Wire MPU Interface Address Selection

CONTROL INTERFACE REGISTERS

DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the FMT[1:0] register bits:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11(0Bh) 0001011 ADC Interface Control	1:0	ADCFMT [1:0]	10	Interface format Select 00 : right justified mode 01: left justified mode 10: I^2S mode 11: DSP mode A or B

In left justified, right justified or I2S modes, the LRP register bit controls the polarity of ADCLRC. If this bit is set high, the expected polarity of ADCLRC will be the opposite of that shown Figure 13, 10 and 11. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the LRP register bit is used to select between modes A and B.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11(0Bh) 0001011 Interface Control	2	ADCLRP	0	In left/right/ I^2S modes: ADCLRC Polarity (normal) 0 : normal ADCLRC polarity 1: inverted ADCLRC polarity In DSP mode: 0 : DSP mode A 1: DSP mode B

By default, ADCLRC is sampled on the rising edge of BCLK and should ideally change on the falling edge. Data sources that change ADCLRC on the rising edge of BCLK can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCLK to the inverse of that shown in Figures 12, 13, 14, and 15.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11(0Bh) 0001011 Interface Control	3	ADCBCP	0	BCLK Polarity (DSP modes) 0 : normal BCLK polarity 1: inverted BCLK polarity

The WL[1:0] bits are used to control the input word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11(0Bh) 0001011 Interface Control	5:4	ADCWL [1:0]	10	Word Length 00 : 16 bit data 01: 20 bit data 10: 24 bit data 11: 32 bit data

Note:

1. If 32-bit mode is selected in right justified mode, the WM8775 defaults to 24 bits.
2. In 24 bit I^2S mode, any width of 24 bits or less is supported provided that ADCLRC is high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

When operating the ADC digital interface in slave mode, to optimise the performance of the ADC it is recommended that the ADCMCLK and ADCBCLK input signals do not have coinciding rising edges. The ADCMCLK bit provides the option to internally invert the ADCMCLK input signal when the input signals have coinciding rising edges.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11(0Bh) 0001011 Interface Control	6	ADCMCLK	0	ADCMCLK Polarity 0 : non-inverted 1: inverted

ADC MASTER MODE

Control bit MS selects between audio interface Master and Slave Modes. In Master mode ADCLRC and BCLK are outputs and are generated by the WM8775. In Slave mode ADCLRC and BCLK are inputs to WM8775.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12(0Ch) 0001100 Interface Control	8	ADCMS	0	Audio Interface Master/Slave Mode select: 0 : Slave Mode 1: Master Mode

MASTER MODE ADCLRC FREQUENCY SELECT

In Master mode the WM8775 generates ADCLRC and BCLK. These clocks are derived from the master clock. The ratio of MCLK to ADCLRC is set by ADCRATE.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12(0Ch) 0001100 ADCLRC Frequency Select	2:0	ADCRATE[2:0]	010	Master Mode MCLK:ADCLRC ratio select: 010: 256fs 011: 384fs 100: 512fs 101: 768fs

ADC OVERSAMPLING RATE SELECT

For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12(0Ch) 0001100 ADC Oversampling Rate	3	ADCOSR	0	ADC oversampling rate select 0: 128x oversampling 1: 64x oversampling

POWERDOWN MODE AND ADC DISABLE

Setting the PDWN register bit immediately powers down the WM8775, including the references, overriding all other powerdown control bits. All trace of the previous input samples is removed, but all control register settings are preserved. When PDWN is cleared, the digital filters will be re-initialised. It is recommended that the 4-channel input mux and buffer, and ADC are powered down before setting PDWN.

The ADC may also be powered down by setting the ADCPD disable bit. Setting ADCPD will disable the ADC and select a low power mode. The ADC digital filters will be reset and will reinitialise when ADCPD is reset.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R13(0Dh) 0001101 Powerdown Control	0	PDWN	0	Power Down Mode Select: 0 : Normal Mode 1: Power Down Mode
	1	ADCPD	0	ADC Disable: 0 : Normal Mode 1: Power Down Mode
	6	AINPD	0	Analogue Input Disable: 0 : Normal Mode 1 : Power Down Mode

ADC GAIN CONTROL

The ADC has an analogue input PGA and digital gain control for each stereo channel. Both the analogue and digital gains are adjusted by the same register, LAG for the left and RAG for the right. The analogue PGA has a range of +24dB to -21dB in 0.5dB steps. The digital gain control allows further attenuation (after the ADC) from -21.5dB to -103dB in 0.5dB steps. Table 11 shows how the register maps the analogue and digital gains.

LAG/RAG[7:0]	ATTENUATION LEVEL	ANALOGUE PGA	DIGITAL ATTENTUATION
00(hex)	-∞ dB (mute)	-21dB	Digital mute
01(hex)	-103dB	-21dB	-82dB
:	:	:	:
A4(hex)	-21.5dB	-21dB	-0.5dB
A5(hex)	-21dB	-21dB	0dB
:	:	:	:
CF(hex)	0dB	0dB	0dB
:	:	:	:
FE(hex)	+23.5dB	+23.5dB	0dB
FF(hex)	+24dB	+24dB	0dB

Table 11 Analogue and Digital Gain Mapping for ADC

Left and right inputs may also be independently muted. The LRBOTH control bit allows the user to write the same attenuation value to both left and right volume control registers, saving on software writes. The ADC volume and mute also applies to the bypass signal path.

In addition a zero cross detect circuit is provided for the input PGA. When ZCLA/ZCRA is set with a write, the gain will update only when the input signal approaches zero (midrail). This minimises audible clicks and 'zipper' noise as the gain values change. A timeout clock is also provided which will generate an update after a minimum of 131072 master clocks (= ~10.5ms with a master clock of 12.288MHz). The timeout clock may be disabled by setting TOD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) 0000111 Timeout Clock Disable	3	TOD	0	Analogue PGA Zero cross detect timeout disable 0 : Timeout enabled 1: Timeout disabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14(0Eh) 0001110 Attenuation ADCL	7:0	LAG[7:0]	11001111 (0dB)	Attenuation data for Left channel ADC gain in 0.5dB steps. See Table 11.
	8	ZCLA	0	Left channel ADC zero cross enable: 0: Zero cross disabled 1: Zero cross enabled
R15(0Fh) 0001111 Attenuation ADCR	7:0	RAG[7:0]	11001111 (0dB)	Attenuation data for right channel ADC gain in 0.5dB steps. See Table 11.
	8	ZCRA	0	Right channel ADC zero cross enable: 0: Zero cross disabled 1: Zero cross enabled
R21(15h) 0010101 ADC Input Mux	8	LRBOTH	0	Right channel input PGA controlled by left channel register 0 : Right channel uses RAG. 1 : Right channel uses LAG.
R21(15h) 0010101 ADC Mute	7	MUTELA	0	Mute for left channel ADC 0: Normal Operation 1: Mute ADC left
	6	MUTERA	0	Mute for right channel ADC 0: Normal operation 1: Mute ADC right

ADC HIGHPASS FILTER DISABLE

The ADC digital filters contain a digital high pass filter. This defaults to enabled and can be disabled using software control bit ADCHPD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11(0Bh) 0001011 ADC Control	8	ADCHPD	0	ADC High pass filter disable: 0: High pass filter enabled 1: High pass filter disabled

LIMITER / AUTOMATIC LEVEL CONTROL (ALC)

The WM8775 has an automatic pga gain control circuit, which can function as a peak limiter or as an automatic level control (ALC). In peak limiter mode, a digital peak detector detects when the input signal goes above a predefined level and will ramp the pga gain down to prevent the signal becoming too large for the input range of the ADC. When the signal returns to a level below the threshold, the pga gain is slowly returned to its starting level. The peak limiter cannot increase the pga gain above its static level.

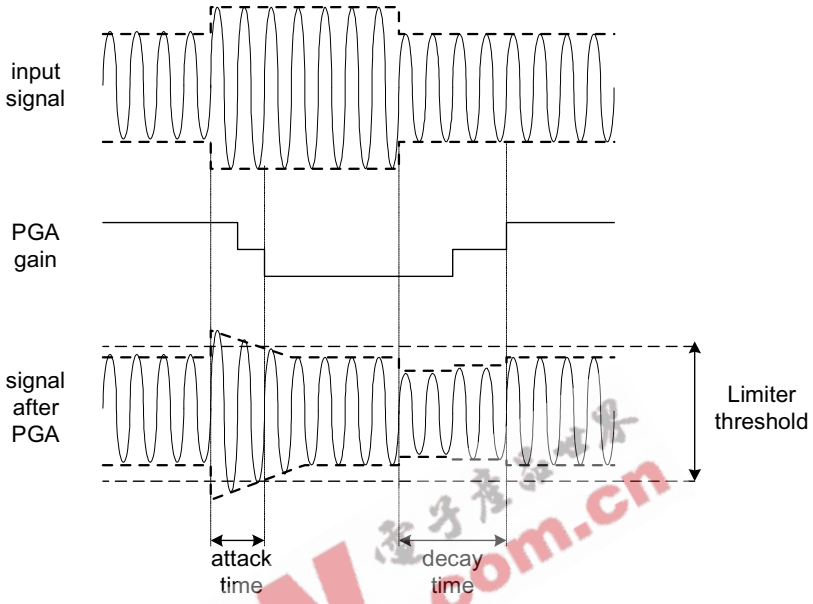


Figure 22 Limiter Operation

In ALC mode, the circuit aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary.

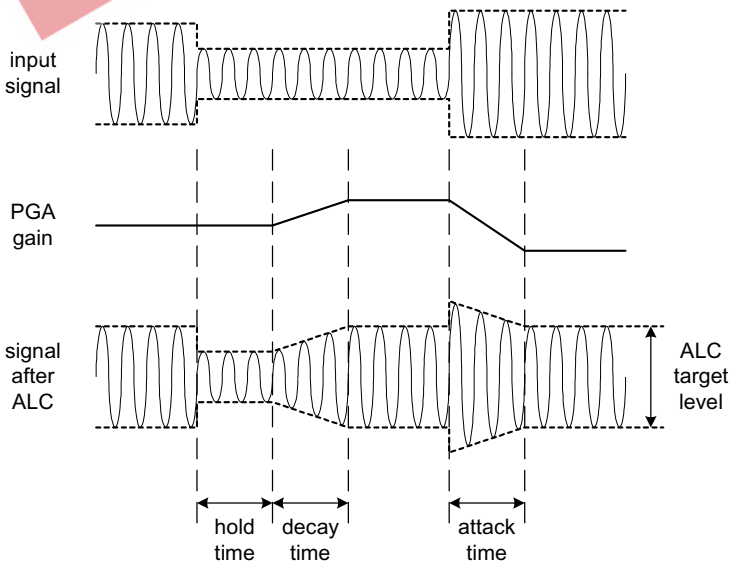


Figure 23 ALC Operation

The gain control circuit is enabled by setting the LCEN control bit. The user can select between Limiter mode and three different ALC modes using the LCSEL control bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17(11h) 0010001 ALC Control 2	8	LCEN	0	Enable the PGA gain control circuit. 0 = Disabled 1 = Enabled
R16(10h) 0010000 ALC Control 1	8:7	LCSEL	00	LC function select 00 = Limiter 01 = ALC Right channel only 10 = ALC Left channel only 11 = ALC Stereo

The limiter function only operates in stereo, which means that the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When enabled, the threshold for the limiter or target level for the ALC is programmed using the LCT control bits. This allows the threshold/target level to be programmed between -1dB and -16dB in 1dB steps. Note that for the ALC, target levels of -1dB and -2dB give a threshold of -3dB. This is because the ALC can give erroneous operation if the target level is set too high.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16(10h) 0010000 ALC Control 1	3:0	LCT[3:0]	1011 (-5dB)	Limiter Threshold/ALC target level in 1dB steps. 0000: -16dB FS 0001: -15dB FS … 1101: -3dB FS 1110: -2dB FS 1111: -1dB FS

ATTACK AND DECAY TIMES

The limiter and ALC have different attack and decay times which determine their operation. However, the attack and decay times are defined slightly differently for the limiter and for the ALC. DCY and ATK control the decay and attack times, respectively.

Decay time (Gain Ramp-Up). When in ALC mode, this is defined as the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –21dB up to +20 dB). When in limiter mode, it is defined as the time it takes for the gain to ramp up by 6dB.

The decay time can be programmed in power-of-two (2^n) steps. For the ALC this gives times from 33.6ms, 67.2ms, 134.4ms etc. to 34.41s. For the limiter this gives times from 1.2ms, 2.4ms etc., up to 1.2288s.

Attack time (Gain Ramp-Down) When in ALC mode, this is defined as the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from +20dB down to -21dB gain). When in limiter mode, it is defined as the time it takes for the gain to ramp down by 6dB.

The attack time can be programmed in power-of-two (2^n) steps, from 8.4ms, 16.8ms, 33.6ms etc. to 8.6s for the ALC and from 250us, 500us, etc. up to 256ms.

The time it takes for the recording level to return to its target value or static gain value therefore depends on both the attack/decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack/decay time.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R18(12h) 0010010 ALC Control 3	3:0	ATK[3:0]	0010	LC attack (gain ramp-down) time	
				ALC mode 0000: 8.4ms 0001: 16.8ms 0010: 33.6ms… (time doubles with every step) 1010 or higher: 8.6s	Limiter Mode 0000: 250us 0001: 500us… 0010: 1ms (time doubles with every step) 1010 or higher: 256ms
	7:4	DCY [3:0]	0011	LC decay (gain ramp-up) time	
				ALC mode 0000: 33.5ms 0001: 67.2ms 0010: 134.4ms ….(time doubles for every step) 1010 or higher: 34.3ms	Limiter mode 0000: 1.2ms 0001: 2.4ms 0010: 4.8ms ….(time doubles for every step) 1010 or higher: 1.2288s

TRANSIENT WINDOW (LIMITER ONLY)

To prevent the limiter responding to to short duration high ampitude signals (such as hand-claps in a live performance), the limiter has a programmable transient window preventing it responding to signals above the threshold until their duration exceeds the window period. The Transient window is set in register TRANWIN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20(14h) 0010100 Limiter Control	6:4	TRANWIN [2:0]	010	Length of Transient Window 000: 0us (disabled) 001: 62.5us 010: 125us ….. 111: 4ms

ZERO CROSS

The PGA has a zero cross detector to prevent gain changes introducing noise to the signal. In ALC mode the register bit ALCZC allows this to be turned off if desired.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17(11h) 0010001 ALC Control 2	7	ALCZC	0 (disabled)	PGA zero cross enable 0 : disabled 1: enabled

MAXIMUM GAIN (ALC ONLY) AND MAXIMUM ATTENUATION

To prevent low level signals being amplified too much by the ALC, the MAXGAIN register sets the upper limit for the gain. This prevents low level noise being over-amplified. The MAXGAIN register has no effect on the limiter operation.

The MAXATTEN register has different operation for the limiter and for the ALC. For the limiter it defines the maximum attenuation below the static (user programmed) gain. For the ALC, it defines the lower limit for the gain.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
R16(10h) 0010000 ALC Control 1	6:4	MAXGAIN	111 (+24dB)	Set maximum gain for the PGA (ALC only) 111 : +24dB 110 : +20dB …..(-4dB steps) 010 : +4dB 001 : 0dB 000 : 0dB	
R20(14h) 0010100 Limiter Control	3:0	MAXATTEN	0110	Maximum attenuation of PGA	
				Limiter (attenuation below static) 0011 or lower: -3dB 0100: -4dB …. (-1dB steps) 1100: -12dB	ALC (lower PGA gain limit) 1010 or lower : -1dB 1011 : -5dB ….. (-4dB steps) 1110 : -17dB 1111 : -21dB

HOLD TIME (ALC ONLY)

The ALC also has a hold time, which is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7ms. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17(11h) 0010001 ALC Control 2	3:0	HLD[3:0]	0000	ALC hold time before gain is increased. 0000: 0ms 0001: 2.67ms 0010: 5.33ms … (time doubles with every step) 1111: 43.691s

OVERLOAD DETECTOR (ALC ONLY)

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes an overload detector. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

(Note: If ATK = 0000, then the overload detector makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used).

NOISE GATE (ALC ONLY)

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM8775 has a noise gate function that prevents noise pumping by comparing the signal level at the AINL1/2/3/4 and/or AINR1/2/3/4 pins against a noise gate threshold, NGTH. The noise gate cuts in when:

- Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

- Signal level at input pin [dB] < NGTH [dB]

When the noise gate is triggered, the PGA gain is held constant (preventing it from ramping up as it would normally when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 6dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19(13h) 0010011 Noise Gate Control	0	NGAT	0	Noise gate function enable 1 = enable 0 = disable
	4:2	NGTH[2:0]	000	Noise gate threshold (with respect to analogue input level) 000: -78dBFS 001: -72dBfs … 6 dB steps 110: -42dBFS 111: -36dBFS

ADC INPUT MUX AND POWERDOWN CONTROL

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21(15h) 0010101 ADC Mux and Powerdown Control	3:0	AMX[3:0]	0001	ADC input mixer control bits (see Table 12)

Register bits AMX[3:0] control the left and right channel inputs into the stereo ADC. The default is AIN1. One bit of AMX is allocated to each stereo input pair to allow the signals to be mixed before being digitised by the ADC. For example, if AMX[3:0] is 0101, the input signal to the ADC will be (AIN1L+AIN3L) on the left channel and (AIN1R+AIN3R) on the right channel.

However if the analogue input buffer is powered down, by setting AINPD, then all 4-channel mux inputs are switched to buffered VMIDADC.

AMX[3:0]	LEFT ADC INPUT	RIGHT ADC INPUT
0001	AIN1L	AIN1R
0010	AIN2L	AIN2R
0100	AIN3L	AIN3R
1000	AIN4L	AIN4R

Table 12 ADC Input Mixer Control

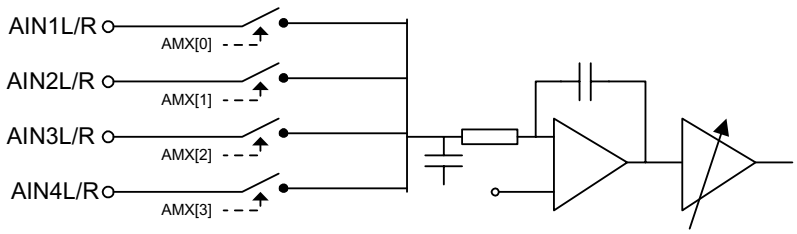


Figure 24 ADC Input Mixer

SOFTWARE REGISTER RESET

Writing to register 0010111 will cause a register reset, resetting all register bits to their default values.

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8775 can be configured using the Control Interface. All unused bits should be set to '0'.

REGISTER	B 15	B 14	B 13	B 12	B 11	B 10	B 9	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT (HEX)
R7 (07h)	0	0	0	0	1	1	1	0	0	0	0	0	TOD	0	0	0	000
R11 (0Bh)	0	0	0	1	0	1	1	ADCHPD	0	ADCMCLK	ADCWL[1:0]		ADCBCP	ADCLRP	ADCFMT[1:0]		022
R12 (OCh)	0	0	0	1	1	0	0	ADCMS	0	0	1	0	ADCOSR	ADCRATE[2:0]			022
R13 (0Dh)	0	0	0	1	1	0	1	0	0	AINPD	0	0	1	0	ADCPD	PWDN	008
R14 (0Eh)	0	0	0	1	1	1	0	ZCLA	LAG[7:0]								0CF
R15 (0Fh)	0	0	0	1	1	1	1	ZCRA	RAG[7:0]								0CF
R16 (10h)	0	0	1	0	0	0	0	LCSEL[1:0]		MAXGAIN[2:0]			LCT[3:0]				07B
R17 (11h)	0	0	1	0	0	0	1	LCEN	ALCZC	0	0	0	HLD[3:0]				000
R18 (12h)	0	0	1	0	0	1	0	0	DCY[3:0]				ATK[3:0]				032
R19 (13h)	0	0	1	0	0	1	1	0	0	0	0	NGTH[2:0]			0	NGAT	000
R20 (14h)	0	0	1	0	1	0	0	0	1	TRANWIN [2:0]			MAXATTEN [3:0]				0A6
R21 (15h)	0	0	1	0	1	0	1	LRBOTH	MUTELA	MUTERA	0		AMX[3:0]				001
R23 (17h)	0	0	1	0	1	1	1	SOFTWARE RESET									not reset

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 (07h) 0000111 Timeout Clock Disable	3	TOD	0	ADC Analogue PGA Zero cross detect timeout disable 0 : Timeout enabled 1: Timeout disabled
R11 (0Bh) 0001011 Interface Control	1:0	ADCFMT[1:0]	10	Interface format select 00: right justified mode 01: left justified mode 10: I²S mode 11: DSP mode
	2	ADCLRP	0	ADCLRC Polarity or DSP mode A/B select In left/right/ I²S modes: ADCLRC Polarity (normal) 0 : normal ADCLRC polarity 1: inverted ADCLRC polarity DSP Mode 0: DSP mode A 1: DSP mode B
	3	ADCBCP	0	BITCLK Polarity 0: Normal - ADCLRC sampled on rising edge of BCLK; DOUT changes on falling edge of BCLK. 1: Inverted - ADCLRC sampled on falling edge of BCLK; DOUT changes on rising edge of BCLK.
	5:4	ADCWL[1:0]	10	Input Word Length 00: 16-bit Mode 01: 20-bit Mode 10: 24-bit Mode 11: 32-bit Mode (not supported in right justified mode)
	6	ADCMCLK	0	ADCMCLK Polarity 0 : non-inverted 1: inverted
	8	ADCHPD	0	ADC High pass Filter Disable: 0: High pass Filter enabled 1: High pass Filter disabled
12 (0Ch) 0001100 Master Mode Control	2:0	ADCRATE[2:0]	010	Master Mode MCLK:ADCLRC ratio select: 010: 256fs 011: 384fs 100: 512fs 101: 768fs
	3	ADCOSR	0	ADC oversample rate select 0: 128x oversampling 1: 64x oversampling
	8	ADCMS	0	Maser/Slave interface mode select 0: Slave Mode – ADCLRC and BCLK are inputs 1: Master Mode – ADCLRC and BCLK are outputs
R13 (0Dh) 0001101 Powerdown Control	0	PWDN	0	Chip Powerdown Control (works together with ADCD): 0: All circuits running, outputs are active 1: All circuits in power save mode, outputs muted
	1	ADCPD	0	ADC powerdown: 0: ADC enabled 1: ADC disabled
	6	AINPD	0	Input mux and buffer powerdown 0: Input mux and buffer enabled 1: Input mux and buffer powered down

R14 (0Eh) 0001110 Attenuation ADCL	7:0	LAG[7:0]	11001111 (0dB)	Attenuation data for left channel ADC gain in 0.5dB steps	
	8	ZCLA	0	Left channel ADC zero cross enable: 0: Zero cross disabled 1: Zero cross enabled	
R15 (0Fh) 0001111 Attenuation ADCR	7:0	RAG[7:0]	11001111 (0dB)	Attenuation data for right channel ADC gain in 0.5dB steps	
	8	ZCRA	0	Right channel ADC zero cross enable: 0: Zero cross disabled 1: Zero cross enabled	
R16 (10h) 0010000 ALC Control 1	3:0	LCT[3:0]	1011 (-5dB)	Limiter Threshold/ALC target level in 1dB steps. 0000: -16dB FS 0001: -15dB FS … 1101: -3dB FS 1110: -2dB FS 1111: -1dB FS	
	6:4	MAXGAIN[2:0]	111 (+24dB)	Set Maximum Gain of PGA 111 : +24dB 110 : +20dB ….(-4dB steps) 010 : +4dB 001 : 0dB 000 : 0dB	
	8:7	LCSEL[1:0]	00	ALC/Limiter function select 00 = Limiter 01 = ALC Right channel only 10 = ALC Left channel only 11 = ALC Stereo (PGA registers unused)	
R17 (11h) 0010001 ALC Control 2	3:0	HLD[3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000: 0ms 0001: 2.67ms 0010: 5.33ms … (time doubles with every step) 1111: 43.691s	
	7	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit.	
	8	LCEN	0	Enable Gain control circuit. 0 = Disable 1 = Enable	
R18 (12h) 0010010 ALC Control 3	3:0	ATK[3:0]	0010 (24ms)	ALC/Limiter attack (gain ramp-down) time	
				ALC mode 0000: 8.4ms 0001: 16.8ms 0010: 33.6ms… (time doubles with every step) 1010 or higher: 8.6s	Limiter Mode 0000: 250us 0001: 500us… 0010: 1ms (time doubles with every step) 1010 or higher: 256ms
	7:4	DCY[3:0]	0011 (268ms/ 9.6ms)	ALC/Limiter decay (gain ramp up) time	
				ALC mode 0000: 33.5ms 0001: 67.2ms 0010: 134.4ms ….(time doubles for every step) 1010 or higher: 34.3ms	Limiter mode 0000: 1.2ms 0001: 2.4ms 0010: 4.8ms ….(time doubles for every step) 1010 or higher: 1.2288s

R19 (13h) 0010011 Noise Gate Control	0	NGAT	0	Noise gate enable (ALC only) 0 : disabled 1 : enabled	
	4:2	NGTH	000	Noise gate threshold 000: -78dBFS 001: -72dBfs … 6 dB steps 110: -42dBFS 111: -36dBFS	
R20 (14h) 0010100 Limiter Control	3:0	MAXATTEN [3:0]	0110	Maximum attenuation of PGA	
				Limiter (attenuation below static) 0011 or lower: -3dB 0100: -4dB …. (-1dB steps) 1100 or higher: -12dB	ALC (lower PGA gain limit) 1010 or lower: -1dB 1011 : -5dB ….. (-4dB steps) 1110 : -17dB 1111 : -21dB
	6:4	TRANWIN [2:0]	010	Length of Transient Window 000: 0us (disabled) 001: 62.5us 010: 125us ….. 111: 4ms	
R21 (15h) 0010101 ADC Mixer Control	3:0	AMX[3:0]	0001	ADC left channel input mixer control bits AMX[3:0] ADC LEFT IN ADC RIGHT IN 0001 AIN1L AIN1R 0010 AIN2L AIN2L 0100 AIN3L AIN3R 1000 AIN4L AIN4R	
	6	MUTERA	0	Mute for right channel ADC 0: Mute off 1: Mute on	
	7	MUTELA	0	Mute for left channel ADC 0: Mute off 1: Mute on	
	8	LRBOTH	0	Setting LRBOTH will write the same gain value to RAG[7:0] and LAG[7:0].	
R23 (17h) 0010111 Software Reset	[8:0]	RESET	Not reset	Writing to this register will apply a reset to the device registers.	

Table 13 Register Map Description

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	±0.01 dB	0		0.4535fs	
	-6dB		0.4892fs		
Passband ripple				±0.01	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-65			dB
Group Delay			22		fs

Table 14 Digital Filter Characteristics

ADC FILTER RESPONSES

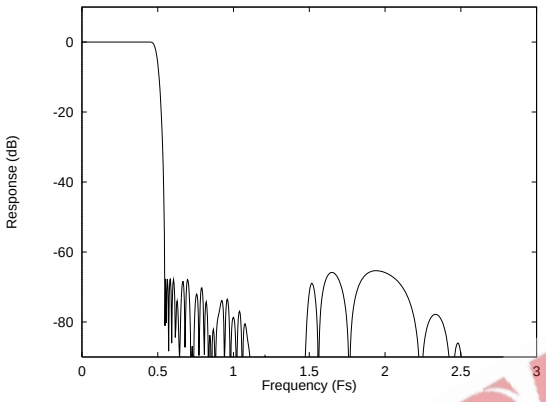


Figure 25 ADC Digital Filter Frequency Response

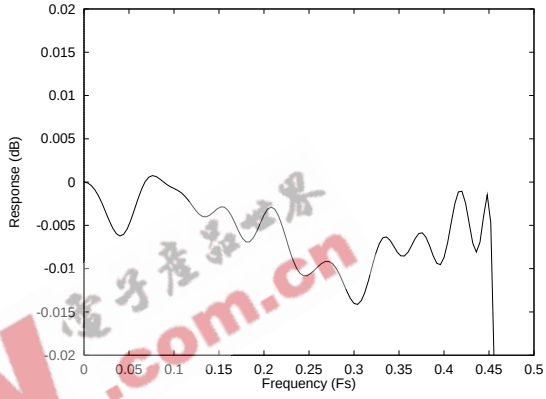


Figure 26 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8775 has a selectable digital highpass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

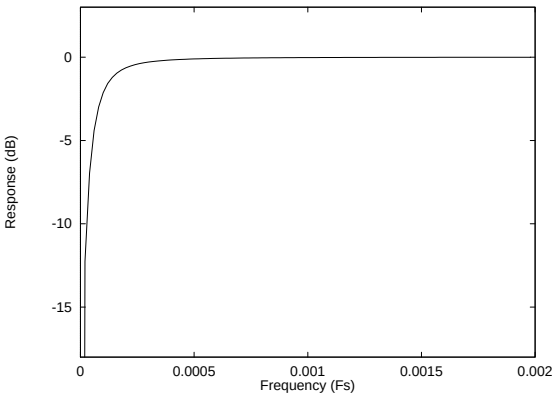


Figure 27 ADC Highpass Filter Response

APPLICATIONS INFORMATION

EXTERNAL CIRCUIT CONFIGURATION

In order to allow the use of 2V rms and larger inputs to the ADC inputs, a structure is used that uses external resistors to drop these larger voltages. This also increases the robustness of the circuit to external abuse such as ESD pulse. Figure 28 shows the ADC input multiplexor circuit with external components allowing 2Vrms inputs to be applied.

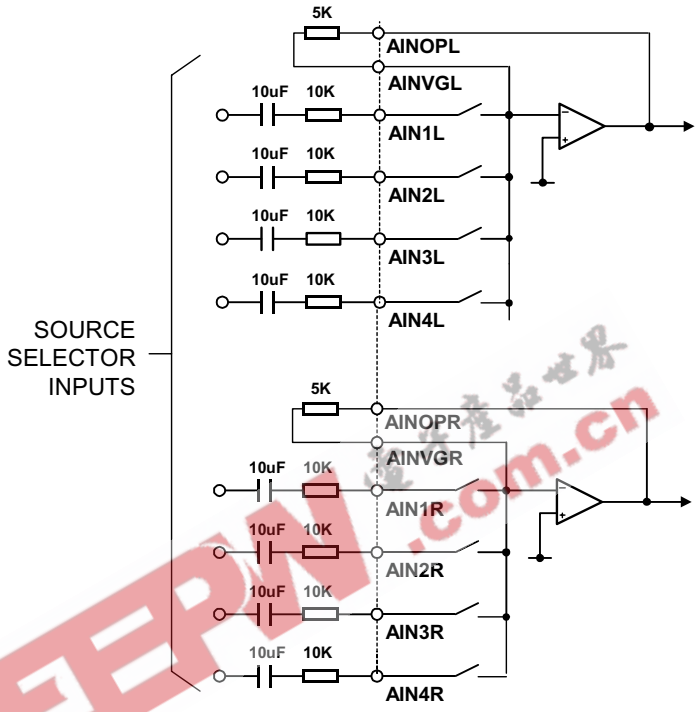
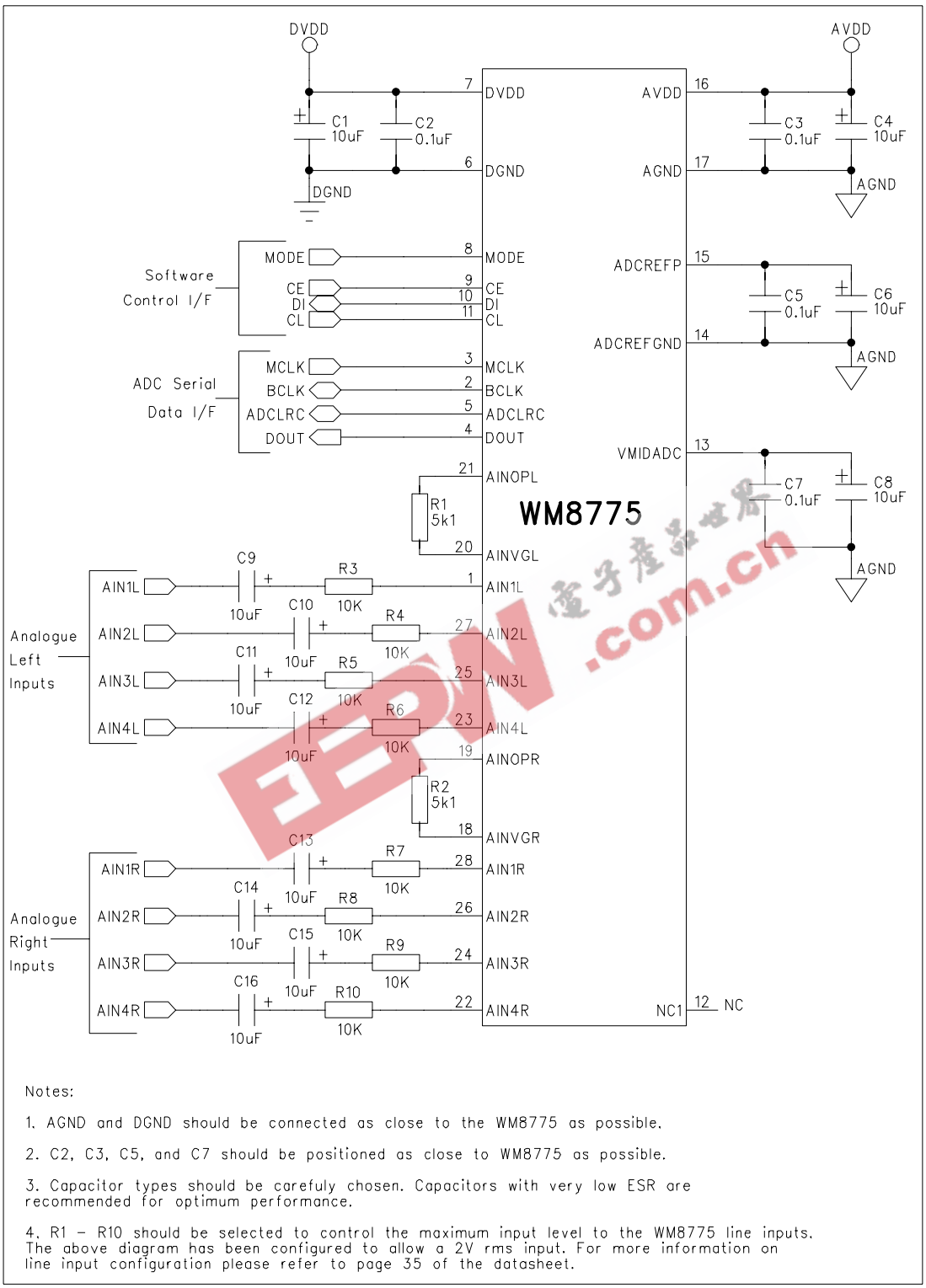


Figure 28 ADC Input Multiplexor Configuration

RECOMMENDED EXTERNAL COMPONENTS



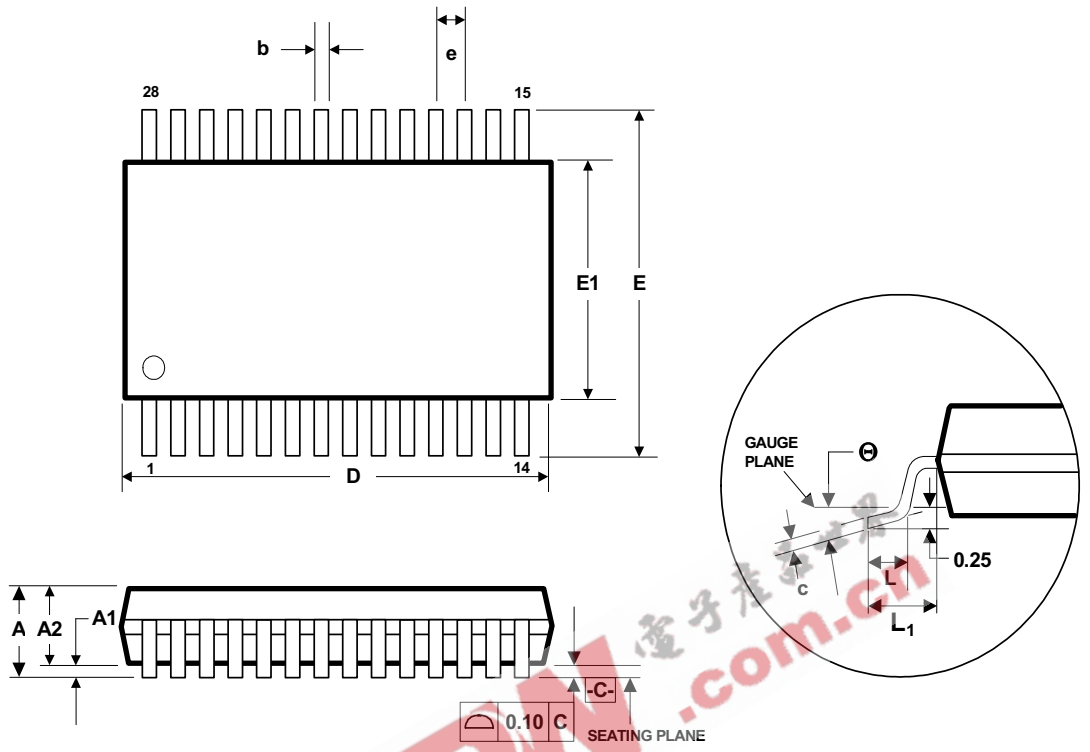
Notes:

1. AGND and DGND should be connected as close to the WM8775 as possible.
2. C2, C3, C5, and C7 should be positioned as close to WM8775 as possible.
3. Capacitor types should be carefuly chosen. Capacitors with very low ESR are recommended for optimum performance.
4. R1 – R10 should be selected to control the maximum input level to the WM8775 line inputs. The above diagram has been configured to allow a 2V rms input. For more information on line input configuration please refer to page 35 of the datasheet.

Figure 29 Recommended External Component Diagram

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.E**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	0.25
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		1.25 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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