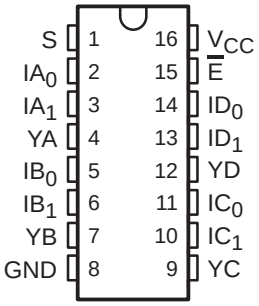
# TS3L110
# QUAD SPDT HIGH-BANDWIDTH 10/100 BASE-T LAN SWITCH
# DIFFERENTIAL 8-CHANNEL TO 4-CHANNEL MULTIPLEXER/DEMULTIPLEXER

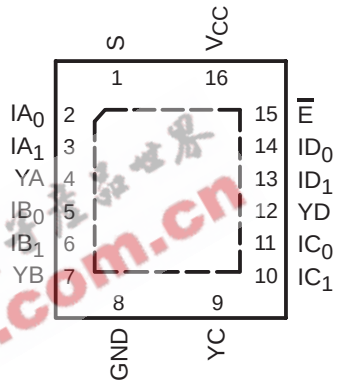
SCDS176 – SEPTEMBER 2004

- Wide Bandwidth (BW = 500 MHz Typ)
- Low Crosstalk ($X_{TALK}$ = −30 dB Typ)
- Bidirectional Data Flow, With Near-Zero Propagation Delay
- Low and Flat ON-State Resistance ($r_{on}$ = 4 Ω Typ, $r_{on(flat)}$ = 1 Ω)
- Switching on Data I/O Ports (0 to 5 V)
- $V_{CC}$ Operating Range From 3 V to 3.6 V
- $I_{off}$ Supports Partial-Power-Down Mode Operation
- Data and Control Inputs Have Undershoot Clamp Diodes
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)
- Suitable for Both 10 Base-T/100 Base-T Signaling

**D, DBQ, DGV, OR PW PACKAGE**
**(TOP VIEW)**




**RGY PACKAGE**
**(TOP VIEW)**




## description/ordering information

The TI TS3L110 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ($\overline{E}$) input. When $\overline{E}$ is low, the switch is enabled, and the I port is connected to the Y port. When $\overline{E}$ is high, the switch is disabled, and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | QFN − RGY | Tape and reel | TS3L110RGYR | TK110 |
| | SOIC − D | Tube | TS3L110D | TS3L110 |
| | | Tape and reel | TS3L110DR | |
| | SSOP (QSOP) − DBQ | Tape and reel | TS3L110DBQR | TK110 |
| | TSSOP − PW | Tube | TS3L110PW | TK110 |
| | | Tape and reel | TS3L110PWR | |
| | TVSOP − DGV | Tape and reel | TS3L110DGVR | TK110 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## description/ordering information (continued)

This device can be used to replace mechanical relays in LAN applications. This device has low and flat $r_{on}$, wide bandwidth, and low crosstalk, making it suitable for 10 Base-T, 100 Base-T, and various other LAN applications. The device can be used to route signals from a 10/100 Base-T ethernet transceiver to the RJ-45 LAN connectors in laptops or in docking stations. The device is designed for low channel-to-channel skew and low crosstalk.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{E}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

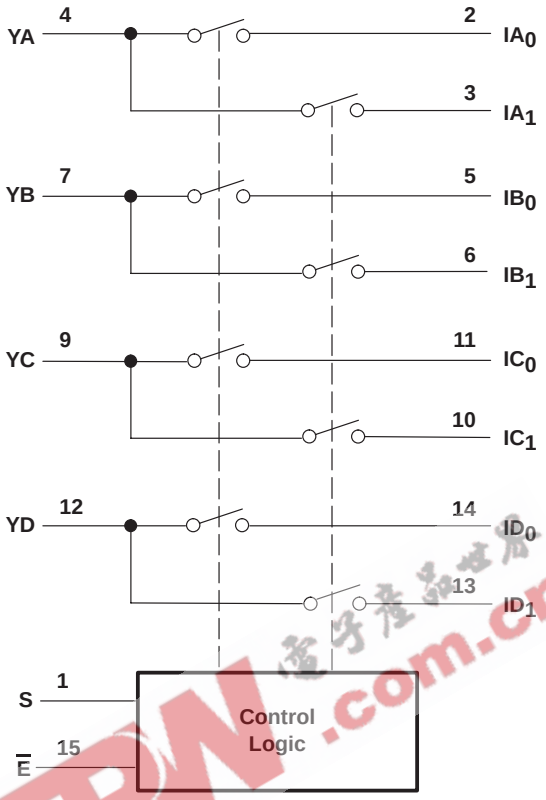
**FUNCTION TABLE**

| INPUTS | | INPUT/OUTPUT YX | FUNCTION |
|---|---|---|---|
| $\overline{E}$ | S | | |
| L | L | $IX_0$ | $YX = IX_0$ |
| L | H | $IX_1$ | $YX = IX_1$ |
| H | X | Z | Disconnect |

**PIN DESCRIPTIONS**

| PIN NAME | DESCRIPTION |
|---|---|
| IAn−IDn | Data I/Os |
| S | Select input |
| $\overline{E}$ | Enable input |
| YA−YD | Data I/Os |

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Control input voltage range, $V_{IN}$ (see Notes 1 and 2) . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 7 V
Control input clamp current, $I_{IK}$ ($V_{IN}$ < 0) . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±128 mA
Continuous current through $V_{CC}$ or GND terminals . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 5): D package . . . . . 73°C/W
(see Note 5): DBQ package . . . . . 90°C/W
(see Note 5): DGV package . . . . . 120°C/W
(see Note 5): PW package . . . . . 108°C/W
(see Note 6): RGY package . . . . . 39°C/W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. $V_I$ and $V_O$ are used to denote specific conditions for $V_{I/O}$.
4. $I_I$ and $I_O$ are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

## recommended operating conditions (see Note 7)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 3.6 | V |
| $V_{IH}$ | High-level control input voltage ($\overline{E}$, S) | 2 | 5.5 | V |
| $V_{IL}$ | Low-level control input voltage ($\overline{E}$, S) | 0 | 0.8 | V |
| $V_{I/O}$ | Input/output voltage | 0 | 5.5 | V |
| $T_A$ | Operating free-air temperature | −40 | 85 | °C |

NOTE 7: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $\overline{E}$, S | $V_{CC}$ = 3.6 V, | $I_{IN}$ = −18 mA | | | | −1.8 | V |
| $I_{IH}$ | $\overline{E}$, S | $V_{CC}$ = 3.6 V, | $V_{IN}$ = 5.5 V | | | | ±1 | µA |
| $I_{IL}$ | $\overline{E}$, S | $V_{CC}$ = 3.6 V, | $V_{IN}$ = GND | | | | ±1 | µA |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_O$ = 0 to 5.5 V , | $V_I$ = 0 | | | 1 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, | $I_{I/O}$ = 0, | Switch ON or OFF | | 0.7 | 1.5 | mA |
| $C_{in}$ | $\overline{E}$, S | f = 1 MHz, | $V_{IN}$ = 0 | | | 2.5 | 3.5 | pF |
| $C_{io(OFF)}$ | I port | $V_I$ = 0, | f = 1 MHz, Outputs open, | Switch OFF | | 3.5 | 5 | pF |
| | Y port | $V_I$ = 0, | f = 1 MHz, Outputs open, | Switch OFF | | 5.5 | 7 | |
| $C_{io(ON)}$ | I or Y port | $V_I$ = 0, | f = 1 MHz, Outputs open, | Switch ON | | 10.5 | 13 | pF |
| $r_{on}$ | | $V_{CC}$ = 3 V | 1.25 V ≤ $V_I$ ≤ $V_{CC}$, | $I_I$ = −10 mA to −30 mA | | 4 | 8 | Ω |
| $r_{on(flat)}$‡ | | $V_{CC}$ = 3 V | $V_I$ = 1.25 V and $V_{CC}$, | $I_I$ = −10 mA to −30 mA | | 1 | | Ω |
| $\Delta r_{on}$§ | | $V_{CC}$ = 3 V, | 1.25 V ≤ $V_I$ ≤ $V_{CC}$, | $I_I$ = −10 mA to −30 mA | | 0.9 | 2 | Ω |

$V_I$, $V_O$, $I_I$, and $I_O$ refer to I/O pins. $V_{IN}$ refers to the control inputs.
† All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
‡ $r_{on(flat)}$ is the difference of $r_{on}$ in a given channel at specified voltages.
§ $\Delta r_{on}$ is the difference of $r_{on}$ in a given device.

## switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V, $R_L$ = 200 Ω, $C_L$ = 10 pF (unless otherwise noted) (see Figures 5 and 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pd}$¶ | I or Y | Y or I | | 0.25 | | ns |
| $t_{PZH}$, $t_{PZL}$ | $\overline{E}$ or S | I or Y | 0.5 | | 7 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | $\overline{E}$ or S | I or Y | 0.5 | | 5 | ns |
| $t_{sk(p)}$# | I or Y | Y or I | | 0.1 | 0.2 | ns |

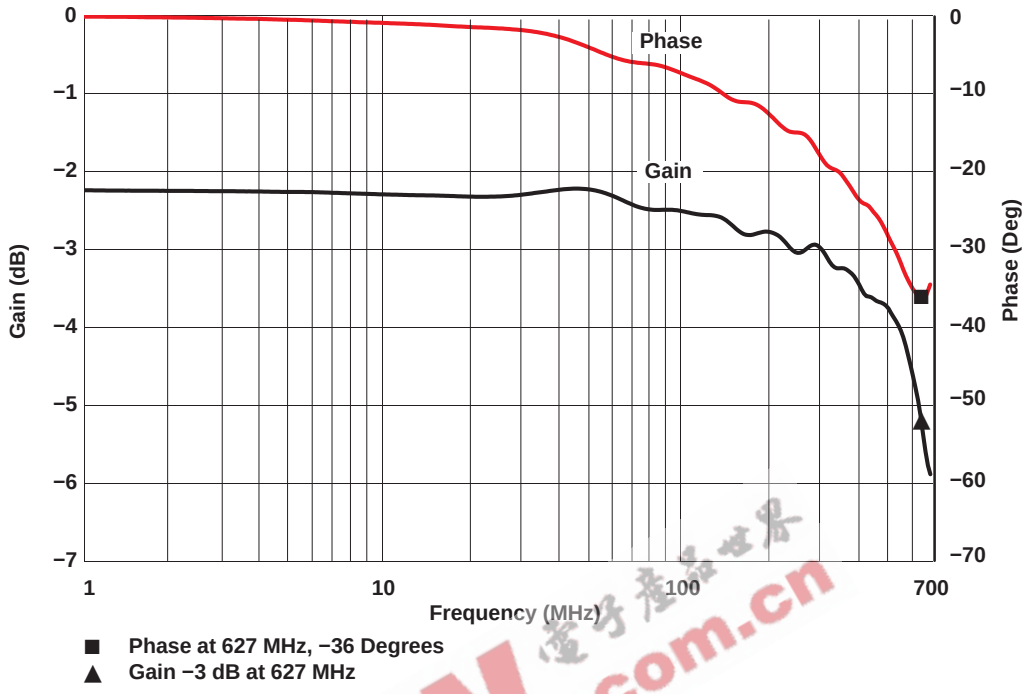
† All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.
¶ The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
# Skew between opposite transitions of the same output $|t_{PHL} - t_{PLH}|$. This parameter is not production tested.

## dynamic characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|
| $X_{TALK}$ | $R_L$ = 100 Ω, | f = 250 MHz, see Figure 7 | | −26 | | dB |
| $O_{IRR}$ | $R_L$ = 100 Ω, | f = 250 MHz, see Figure 8 | | −28 | | dB |
| BW | $R_L$ = 100 Ω, see Figure 6 | | | 500 | | MHz |

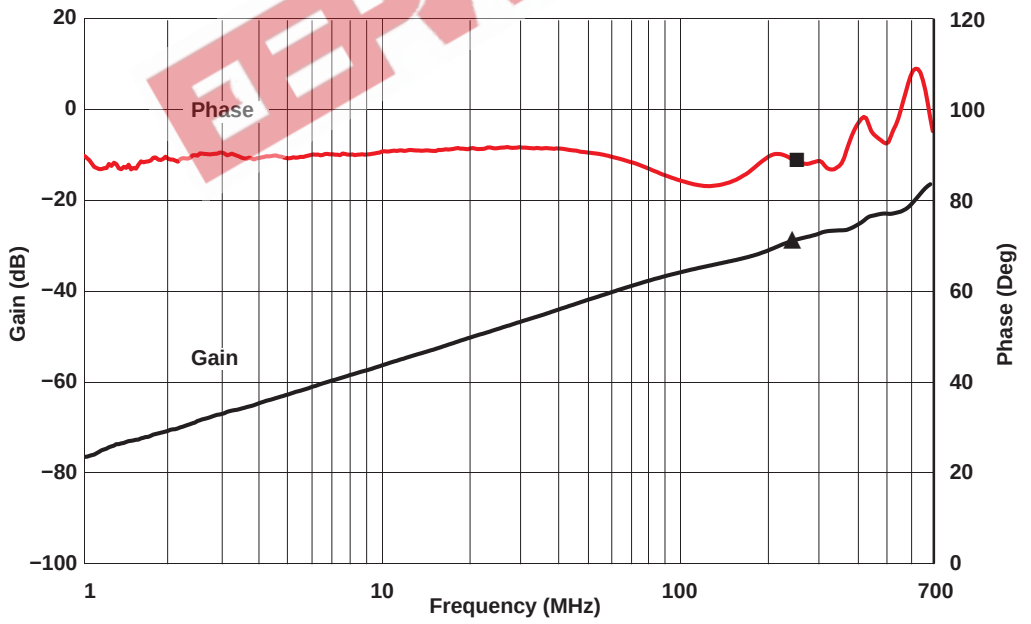
† All typical values are at $V_{CC}$ = 3.3 V (unless otherwise noted), $T_A$ = 25°C.

## OPERATING CHARACTERISTICS




■ Phase at 627 MHz, −36 Degrees
▲ Gain −3 dB at 627 MHz

**Figure 1. Gain/Phase vs Frequency**




■ Phase at 250 MHz, 88.2 Degrees
▲ Gain −28.5 dB at 250 MHz

**Figure 2. OFF Isolation vs Frequency**

## OPERATING CHARACTERISTICS

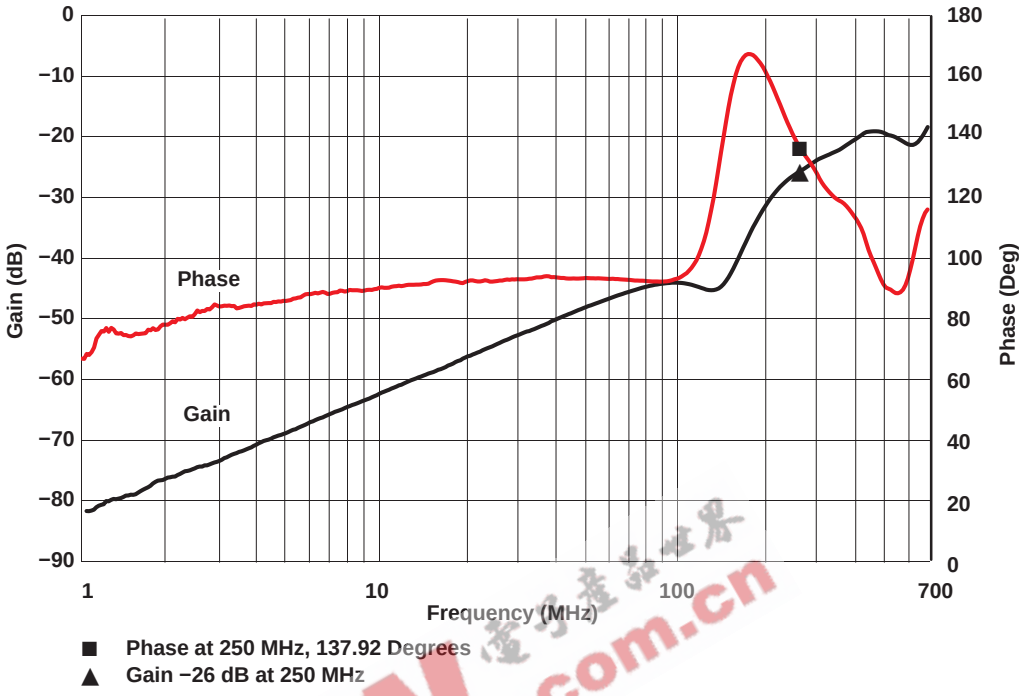



Figure 3. Crosstalk vs Frequency

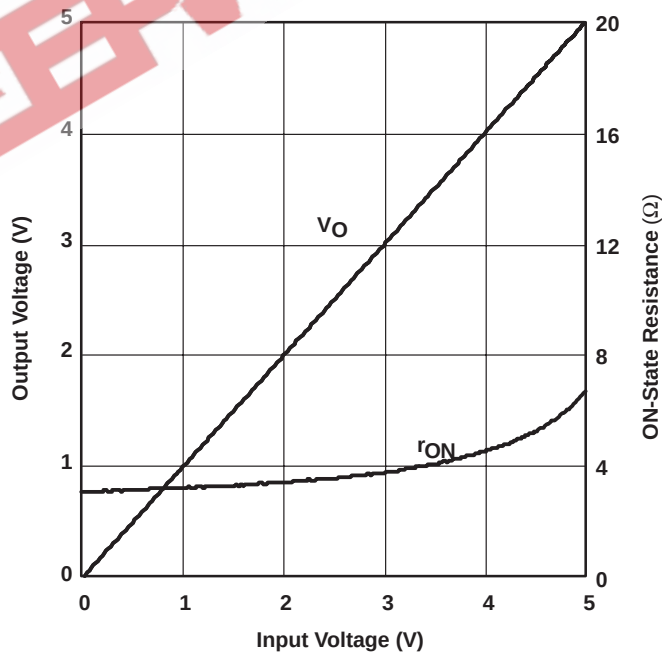
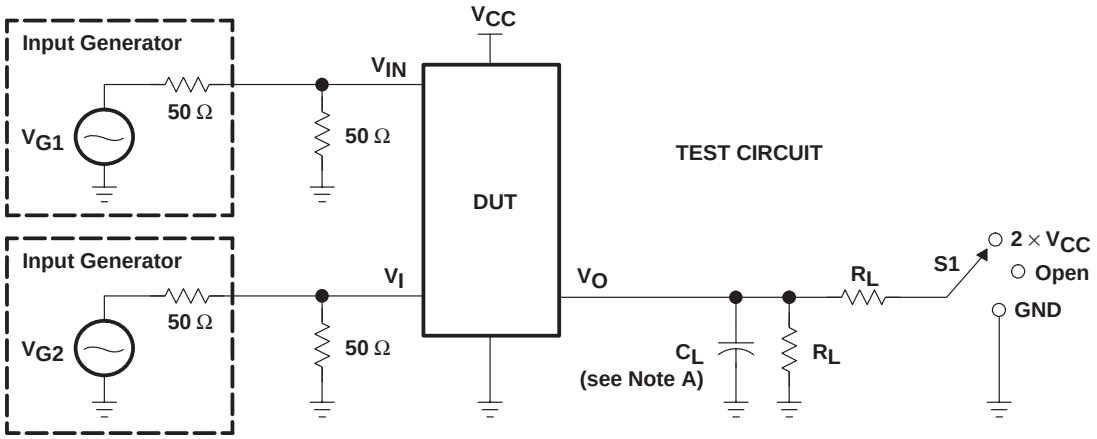
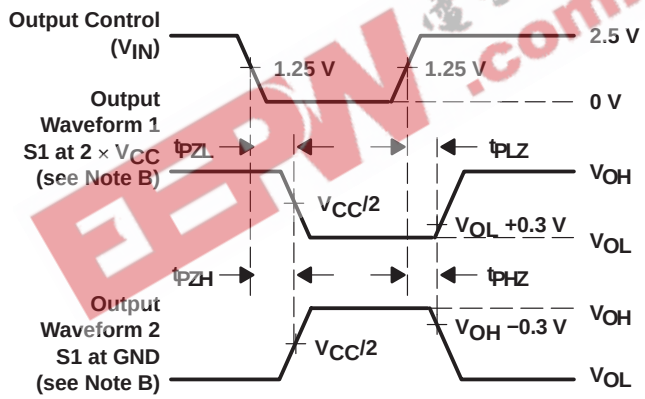



Figure 4. Output Voltage/ON-State Resistance vs Input Voltage

## PARAMETER MEASUREMENT INFORMATION FOR ENABLE AND DISABLE TIMES




| TEST | $V_{CC}$ | S1 | $R_L$ | $V_I$ | $C_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|
| $t_{PLZ}/t_{PZL}$ | 3.3 V ± 0.3 V | 2 × $V_{CC}$ | 200 Ω | GND | 10 pF | 0.3 V |
| $t_{PHZ}/t_{PZH}$ | 3.3 V ± 0.3 V | GND | 200 Ω | $V_{CC}$ | 10 pF | 0.3 V |

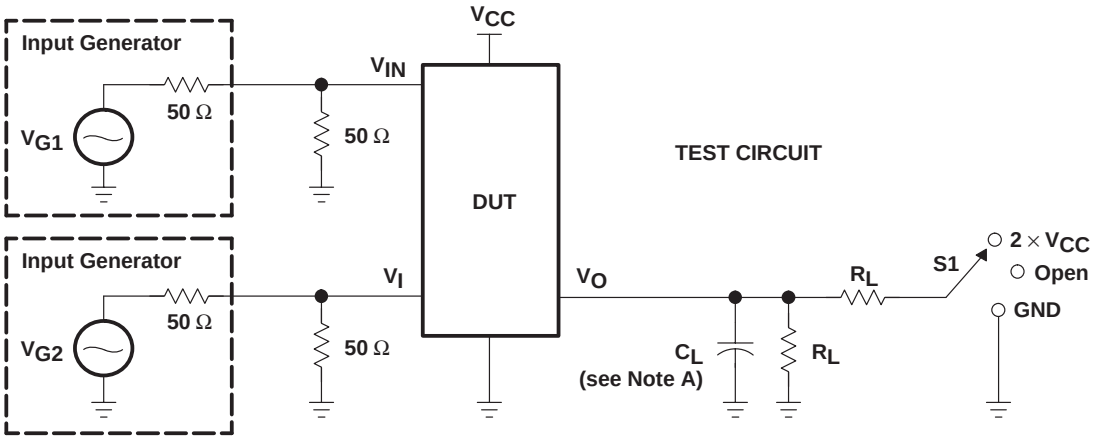



**VOLTAGE WAVEFORMS**
**ENABLE AND DISABLE TIMES**

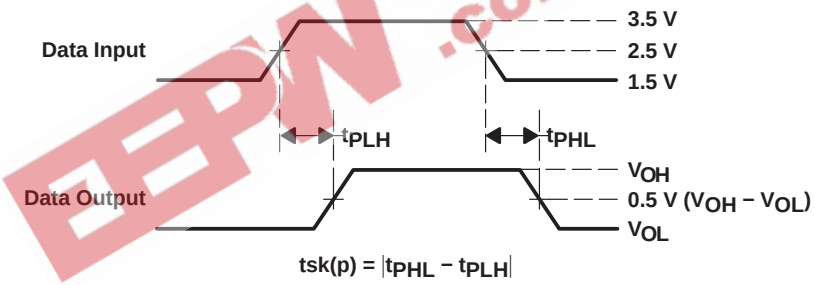
NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.

**Figure 5. Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION FOR SKEW




| TEST | $V_{CC}$ | S1 | $R_L$ | $V_{IN}$ (see Note B) | $C_L$ |
|---|---|---|---|---|---|
| $t_{sk(p)}$ | 3.3 V ± 0.3 V | GND | 200 Ω | $V_{CC}$ or GND | 10 pF |

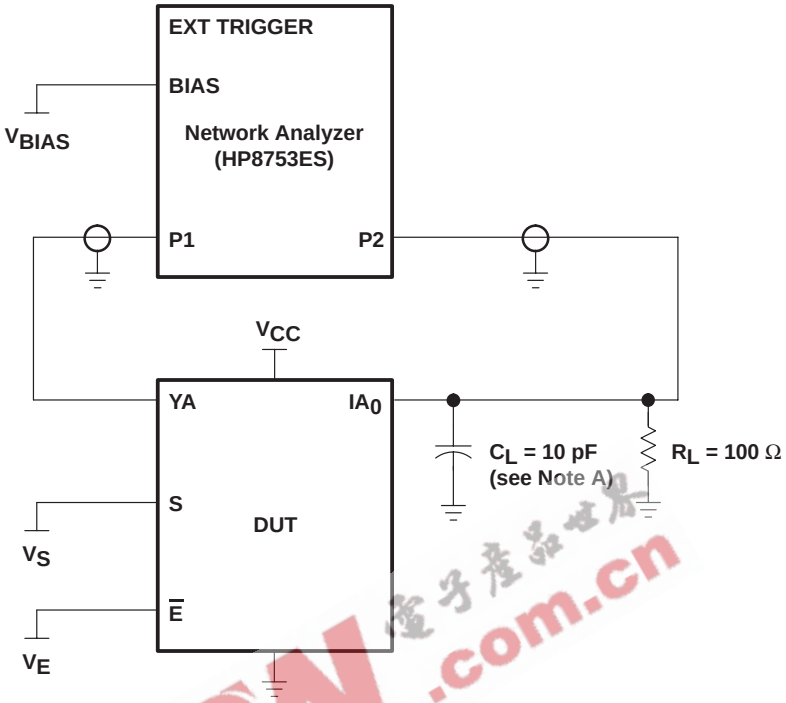



VOLTAGE WAVEFORMS
PULSE SKEW ($t_{sk(p)}$)

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Switch is ON during the measurement of $t_{sk(p)}$, i.e., voltage at $\overline{E}$ = 0 and S = $V_{CC}$ or GND

**Figure 6. Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION




NOTE A: $C_L$ includes probe and jig capacitance.

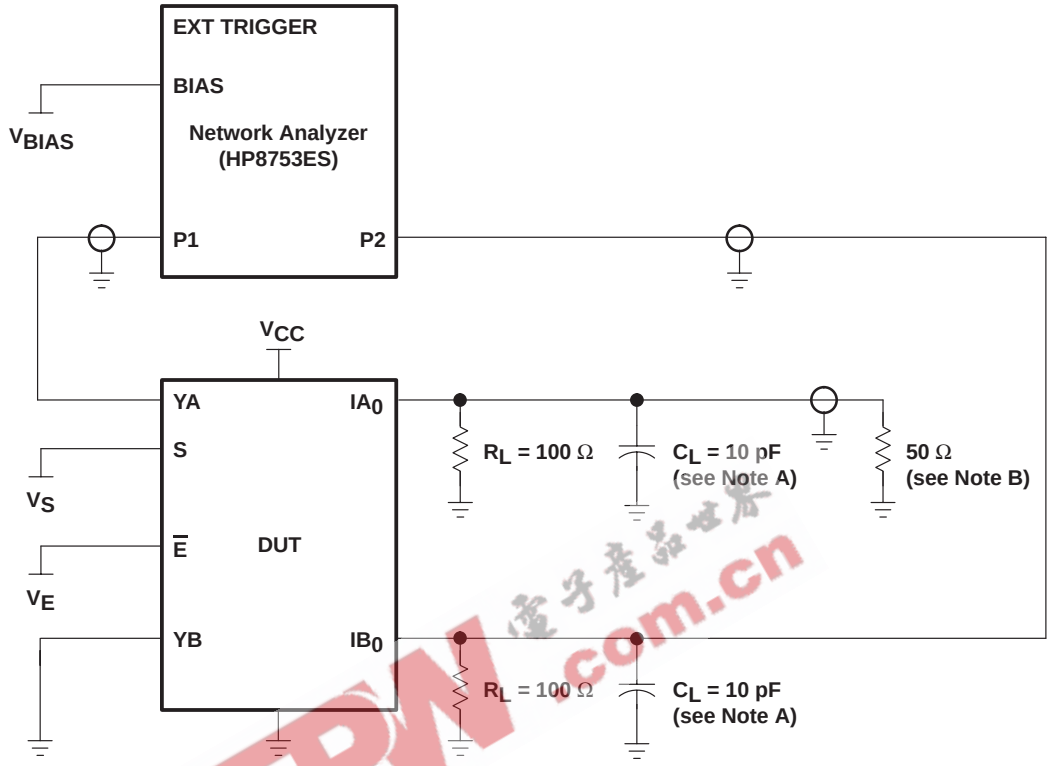
**Figure 7. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when $V_S$ = 0, $V_E$ = 0, and YA is the input, the output is measured at $IA_0$. All unused analog I/O ports are left open.

### HP8753ES setup

Average = 4
RBW = 3 kHz
$V_{BIAS}$ = 0.35 V
ST = 2 s
P1 = 0 dBm

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

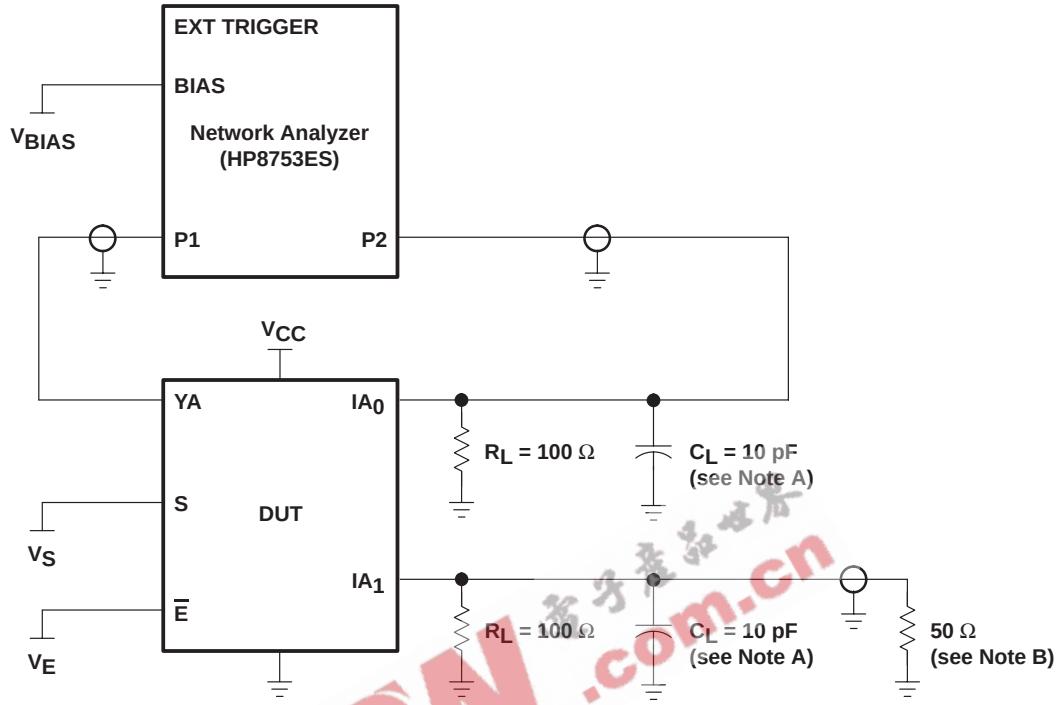
**Figure 8. Test Circuit for Crosstalk ($X_{TALK}$)**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when $V_S$ = 0, $V_E$ = 0, and YA is the input, the output is measured at $IB_0$. All unused analog input (Y) ports are connected to GND, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

### HP8753ES setup

Average = 4
RBW = 3 kHz
$V_{BIAS}$ = 0.35 V
ST = 2 s
P1 = 0 dBm

## PARAMETER MEASUREMENT INFORMATION




NOTES: A. $C_L$ includes probe and jig capacitance.
B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

**Figure 9. Test Circuit for OFF Isolation ($O_{IRR}$)**

OFF isolation is measured at the output of the OFF channel. For example, when $V_S = V_{CC}$, $V_E = 0$, and YA is the input, the output is measured at $IA_0$. All unused analog input (Y) ports are left open, and output (I) ports are connected to GND through 50-Ω pulldown resistors.

### HP8753ES setup

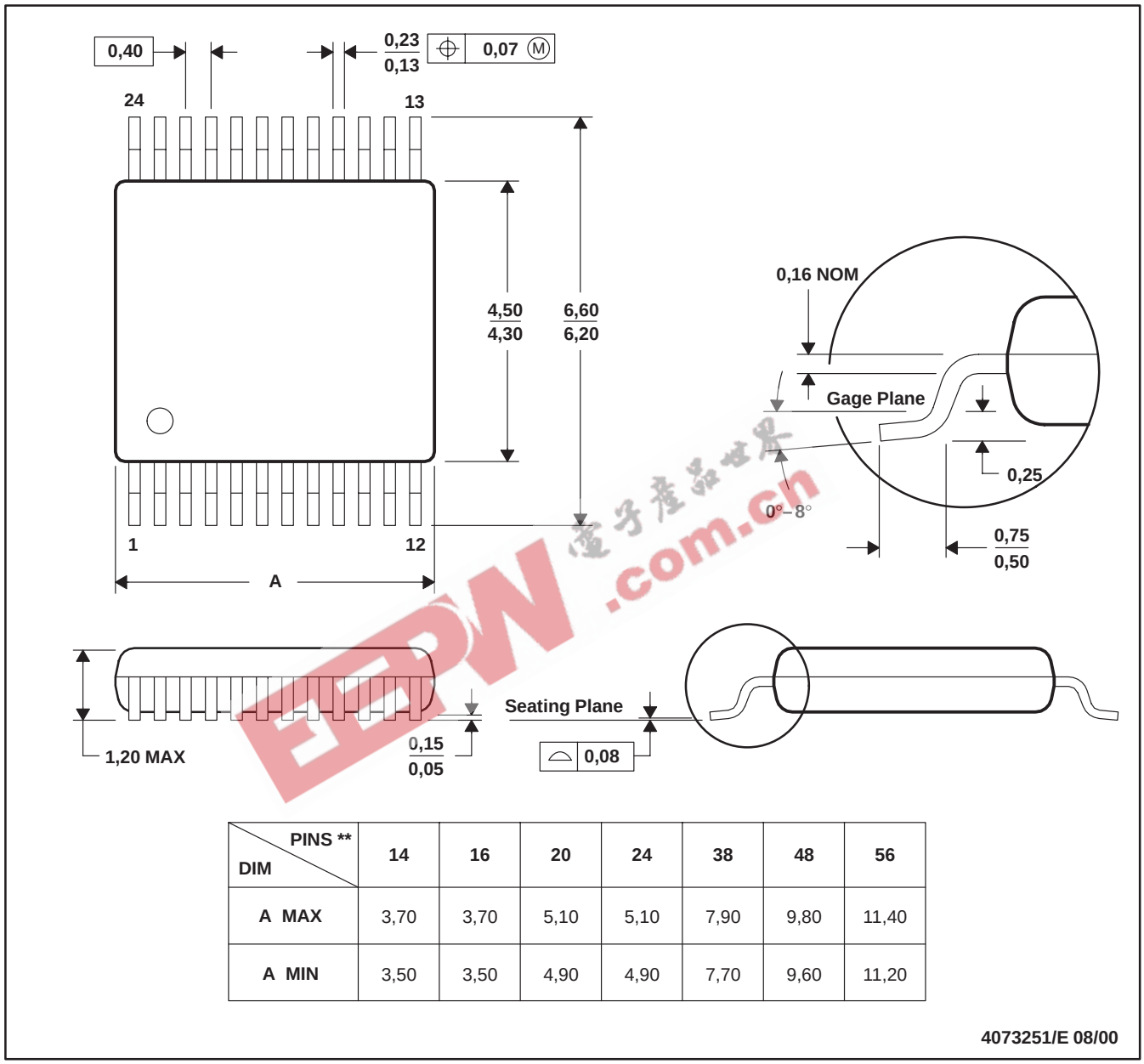
Average = 4
RBW = 3 kHz
$V_{BIAS}$ = 0.35 V
ST = 2 s
P1 = 0 dBm

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

## DGV (R-PDSO-G**)

## PLASTIC SMALL-OUTLINE

**24 PINS SHOWN**

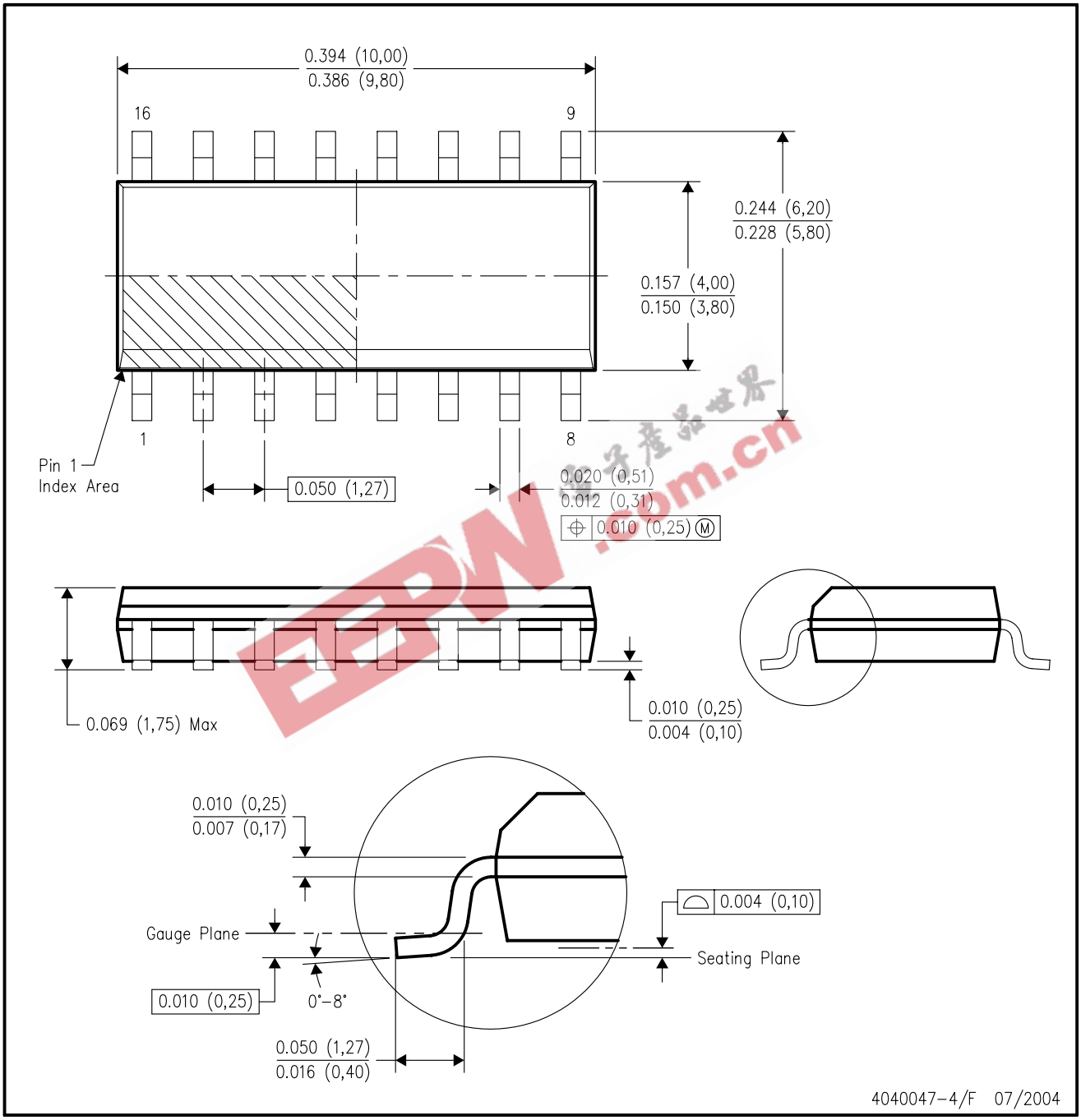



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

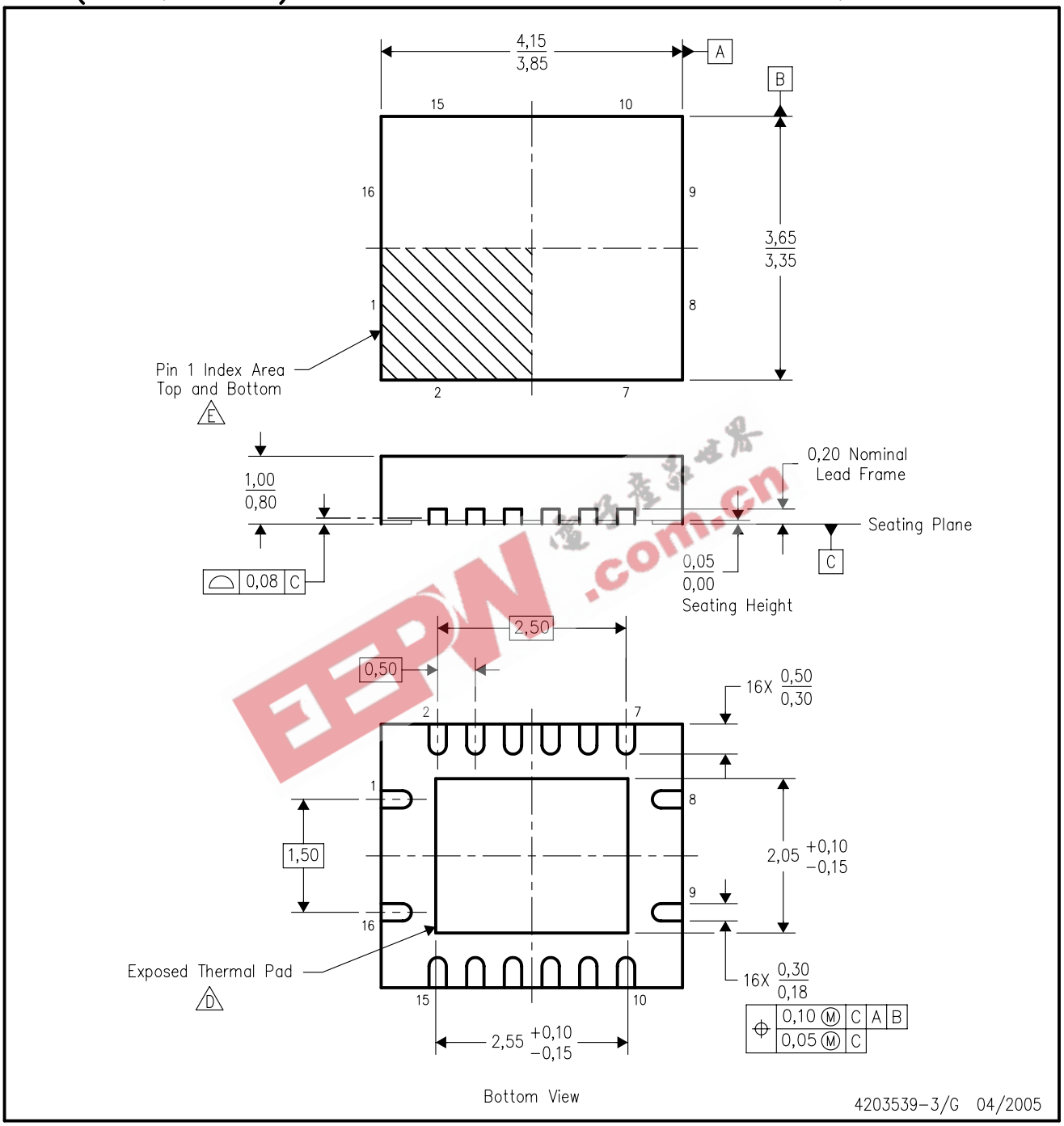
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



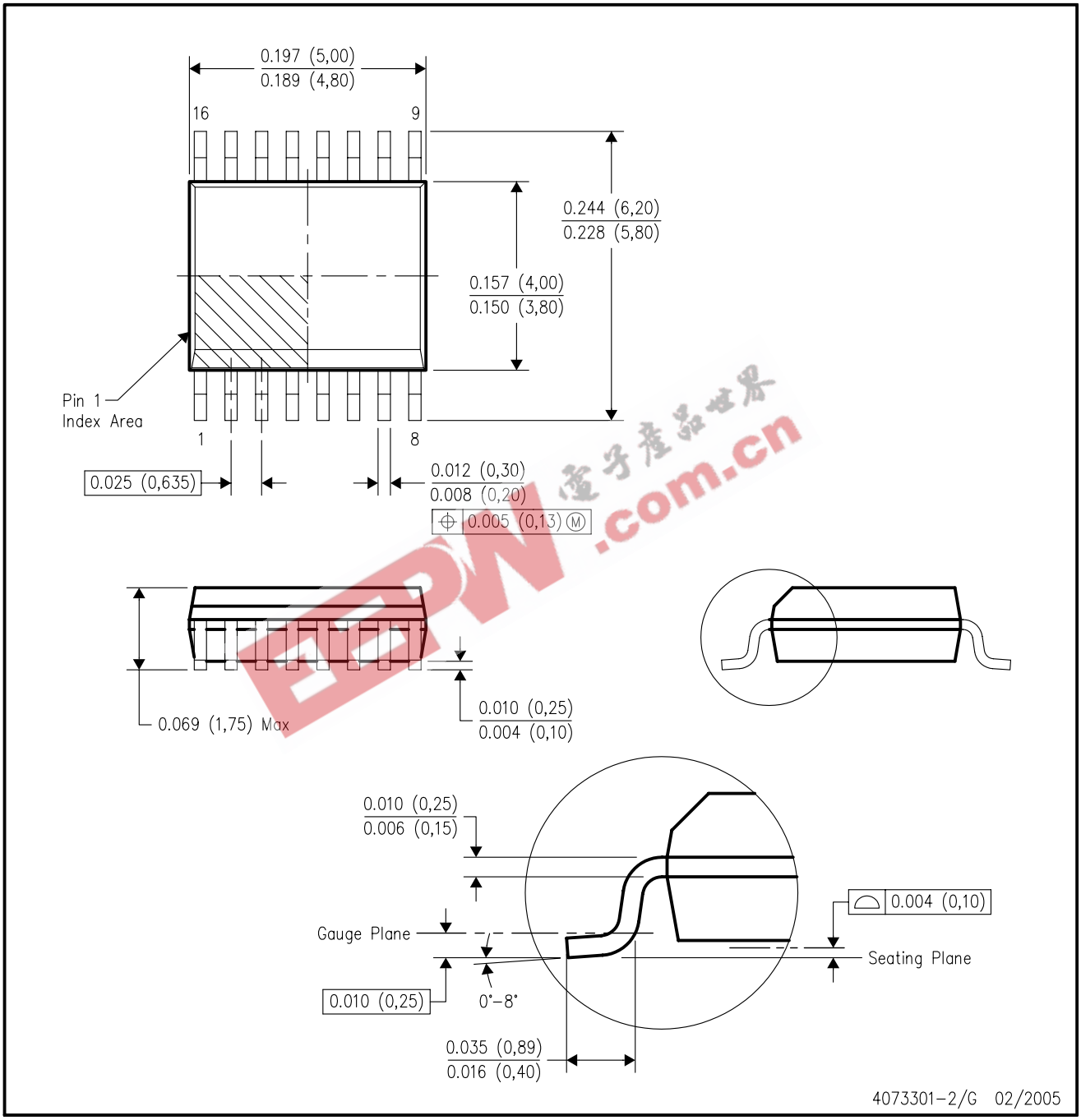

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AC.

RGY (R–PQFP–N16) PLASTIC QUAD FLATPACK




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BB.

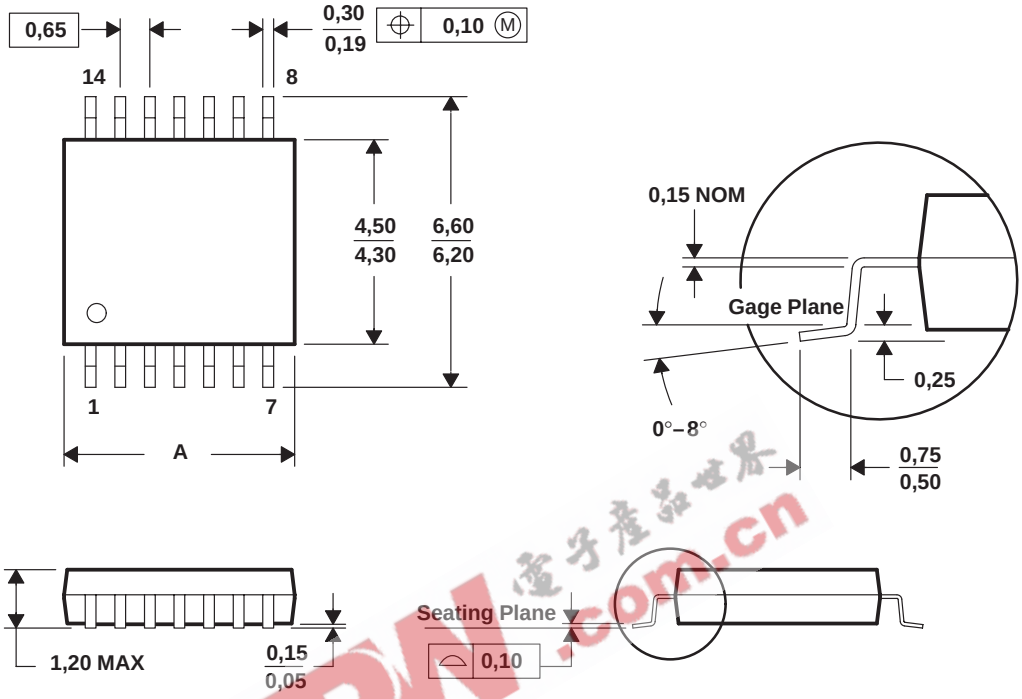
## DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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