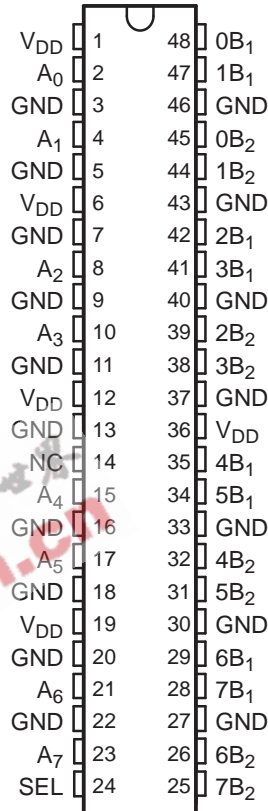


## FEATURES

- **Compatible With HDMI v1.2a (Type A) DVI 1.0 High-Speed Digital Interface**
  - Wide Bandwidth of Over 1.65 Gbps (Bandwidth 1.8 Gbps Typ)
  - 165-MHz Speed Operation
  - Serial Data Stream at 10× Pixel Clock Rate
  - Supports All Video Formats up to 1080p and SXGA (1280 × 1024 at 75 Hz)
  - Total Raw Capacity 4.95 Gbps (Single Link)
  - HDCP Compatible
- **Low Crosstalk ( $X_{TALK} = -41$  dB Typ)**
- **Low Bit-to-Bit Skew ( $t_{sk(o)} = 0.2$  ns Max)**
- **Low and Flat ON-State Resistance ( $r_{on} = 4 \Omega$  Typ,  $r_{on(flat)} = 0.7 \Omega$  Typ)**
- **Low Input/Output Capacitance ( $C_{ON} = 10$  pF Typ)**
- **Rail-to-Rail Switching on Data I/O Ports (0 to 5 V)**
- **$V_{DD}$  Operating Range From 3 V to 3.6 V**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE  
(TOP VIEW)



NC – No internal connection

## APPLICATIONS

- Digital Video Signal Switching
- Differential DVI, HDMI Signal Multiplexing for Audio/Video Receivers and High-Definition Television (HDTV)

## DESCRIPTION/ORDERING INFORMATION

The TS3DV416 is a 16-bit to 8-bit multiplexer/demultiplexer digital video switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer.

The device provides a low and flat ON-state resistance ( $r_{on}$ ) and an excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various digital video applications, such as DVI and HDMI.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# TS3DV416 4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

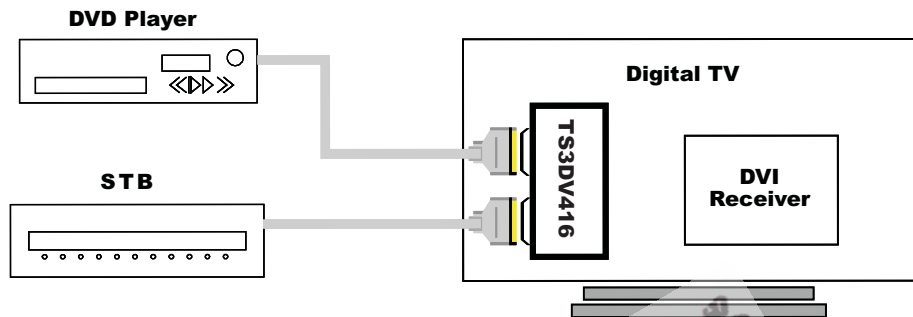
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## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	TS3DV416DGGR	TS3DV416
	TVSOP – DGV	Tape and reel	TS3DV416DGVR	SD416

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

## TYPICAL APPLICATION



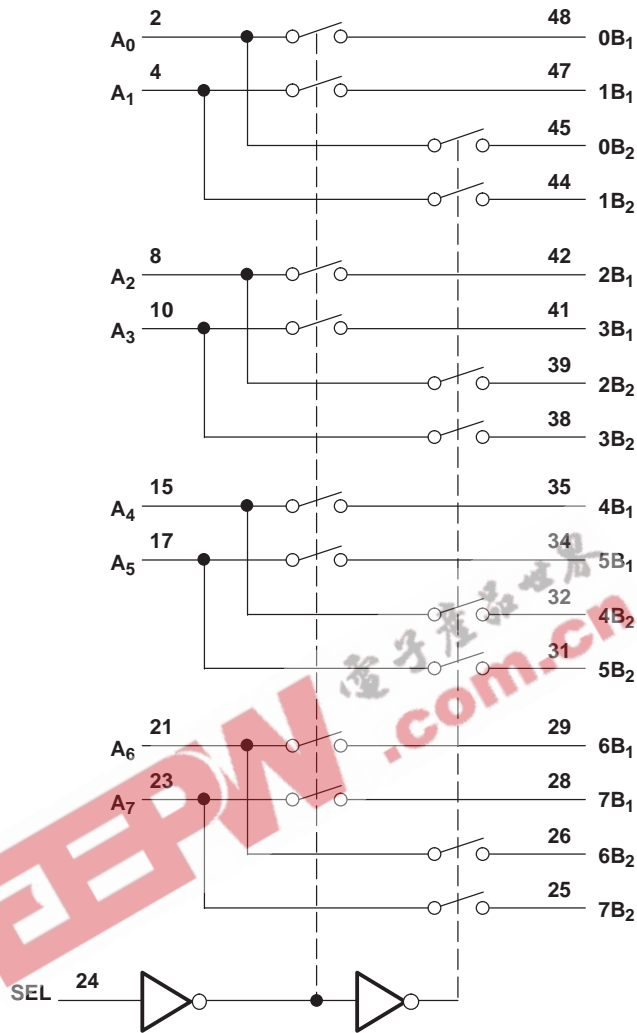
## FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT A <sub>n</sub>	FUNCTION	
L	nB <sub>1</sub>	A <sub>n</sub> = nB <sub>1</sub>	nB <sub>2</sub> high-impedance mode
H	nB <sub>2</sub>	A <sub>n</sub> = nB <sub>2</sub>	nB <sub>1</sub> high-impedance mode

## PIN DESCRIPTION

NAME	DESCRIPTION
A <sub>n</sub>	Data I/O
nB <sub>m</sub>	Data I/O
SEL	Select input

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# TS3DV416

## 4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

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### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage range	-0.5	4.6	V
V <sub>IN</sub>	Control input voltage range <sup>(2)(3)</sup>	-0.5	7	V
V <sub>I/O</sub>	Switch I/O voltage range <sup>(2)(3)(4)</sup>	-0.5	7	V
I <sub>IK</sub>	Control input clamp current		-50	mA
			V <sub>IN</sub> < 0	
I <sub>I/O</sub> K	I/O port clamp current		-50	mA
			V <sub>I/O</sub> < 0	
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>		±128	mA
	Continuous current through V <sub>DD</sub> or GND		±100	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(6)</sup>		70	°C/W
		DGG package		
	DGV package		58	
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage	3	3.6	V
V <sub>IH</sub>	High-level control input voltage (SEL)	2	5.5	V
V <sub>IL</sub>	Low-level control input voltage (SEL)	0	0.8	V
V <sub>I/O</sub>	Input/output voltage	0	5.5	V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>DD</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### Electrical Characteristics<sup>(1)</sup>

for high-frequency switching over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
$V_{IK}$	SEL	$V_{DD} = 3.6 \text{ V}$ , $I_{IN} = -18 \text{ mA}$		-0.7	-1.2	V
$I_{IH}$	SEL	$V_{DD} = 3.6 \text{ V}$ , $V_{IN} = V_{DD}$			$\pm 1$	$\mu\text{A}$
$I_{IL}$	SEL	$V_{DD} = 3.6 \text{ V}$ , $V_{IN} = \text{GND}$			$\pm 1$	$\mu\text{A}$
$I_{off}$		$V_{DD} = 0$ , $V_O = 0 \text{ to } 3.6 \text{ V}$ , $V_I = 0$			1	$\mu\text{A}$
$I_{DD}$		$V_{DD} = 3.6 \text{ V}$ , $I_{I/O} = 0$ , Switch ON or OFF		250	600	$\mu\text{A}$
$C_{IN}$	SEL	$f = 1 \text{ MHz}$ , $V_{IN} = 0$		2.5	3	pF
$C_{OFF}$	B port	$V_I = 0$ , $f = 1 \text{ MHz}$ , Outputs open, Switch OFF		3.5	4	pF
$C_{ON}$		$V_I = 0$ , $f = 1 \text{ MHz}$ , Outputs open, Switch ON		10	10.9	pF
$r_{on}$		$V_{DD} = 3 \text{ V}$ , $1.5 \text{ V} \leq V_I \leq V_{DD}$ , $I_O = -40 \text{ mA}$		4	8	$\Omega$
$r_{on(\text{flat})}$ <sup>(3)</sup>		$V_{DD} = 3 \text{ V}$ , $V_I = 1.5 \text{ V}$ and $V_{DD}$ , $I_O = -40 \text{ mA}$		0.7		$\Omega$
$\Delta r_{on}$ <sup>(4)</sup>		$V_{DD} = 3 \text{ V}$ , $1.5 \text{ V} \leq V_I \leq V_{DD}$ , $I_O = -40 \text{ mA}$		0.2	1.2	$\Omega$

- (1)  $V_I$ ,  $V_O$ ,  $I_I$ , and  $I_O$  refer to I/O pins.  $V_{IN}$  refers to the control inputs.  
 (2) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
 (3)  $r_{on(\text{flat})}$  is the difference of  $r_{on}$  in a given channel at specified voltages.  
 (4)  $\Delta r_{on}$  is the difference of  $r_{on}$  from center ( $A_4$ ,  $A_5$ ) ports to any other port.

### Switching Characteristics

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $R_L = 200 \Omega$ ,  $C_L = 10 \text{ pF}$  (unless otherwise noted) (see [Figure 4](#) and [Figure 5](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP <sup>(1)</sup>	MAX	UNIT
$t_{pd}$ <sup>(2)</sup>	A or B	B or A		0.04		ns
$t_{PZH}$ , $t_{PZL}$	SEL	A or B	1.5		11.5	ns
$t_{PHZ}$ , $t_{PLZ}$	SEL	A or B	1		8.5	ns
$t_{sk(o)}$ <sup>(3)</sup>	A or B	B or A		0.1	0.2	ns
$t_{sk(p)}$ <sup>(4)</sup>				0.1	0.2	ns

- (1) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .  
 (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).  
 (3) Output skew between center port ( $A_4$  to  $A_5$ ) to any other port  
 (4) Skew between opposite transitions of the same output in a given device  $|t_{PHL} - t_{PLH}|$

### Dynamic Characteristics

over recommended operating free-air temperature range,  $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS		TYP <sup>(1)</sup>	UNIT
$X_{TALK}$	$R_L = 100 \Omega$ , $f = 250 \text{ MHz}$ ,	See <a href="#">Figure 7</a>	-41	dB
$O_{IRR}$	$R_L = 100 \Omega$ , $f = 250 \text{ MHz}$ ,	See <a href="#">Figure 8</a>	-39	dB
BW	See <a href="#">Figure 6</a>		900	MHz

- (1) All typical values are at  $V_{DD} = 3.3 \text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

TS3DV416  
4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH  
FOR DVI/HDMI APPLICATIONS

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OPERATING CHARACTERISTICS

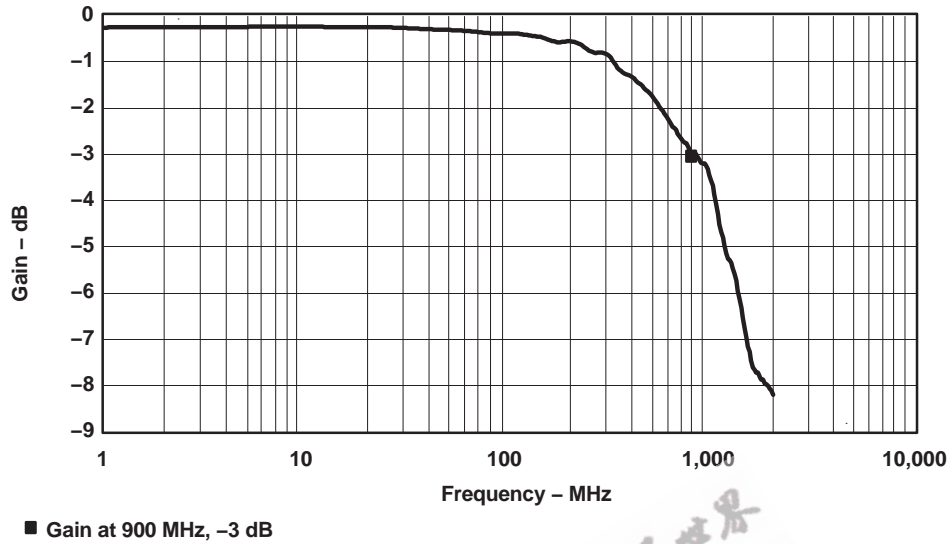


Figure 1. Gain vs Frequency

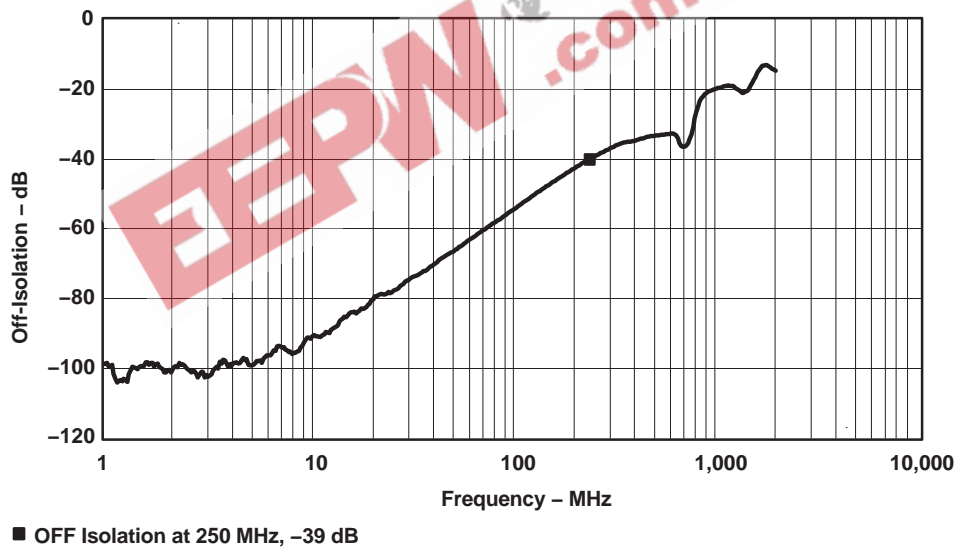


Figure 2. OFF Isolation vs Frequency

OPERATING CHARACTERISTICS (continued)

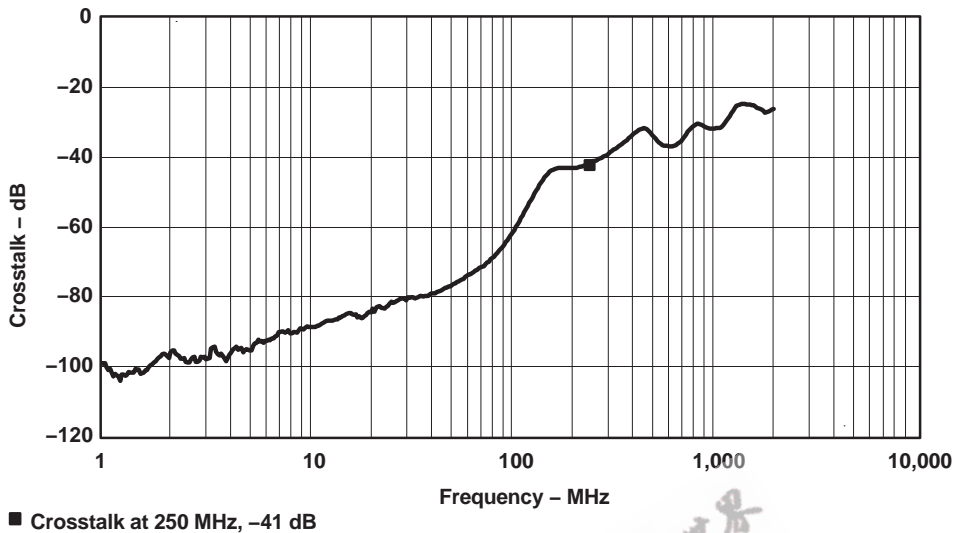


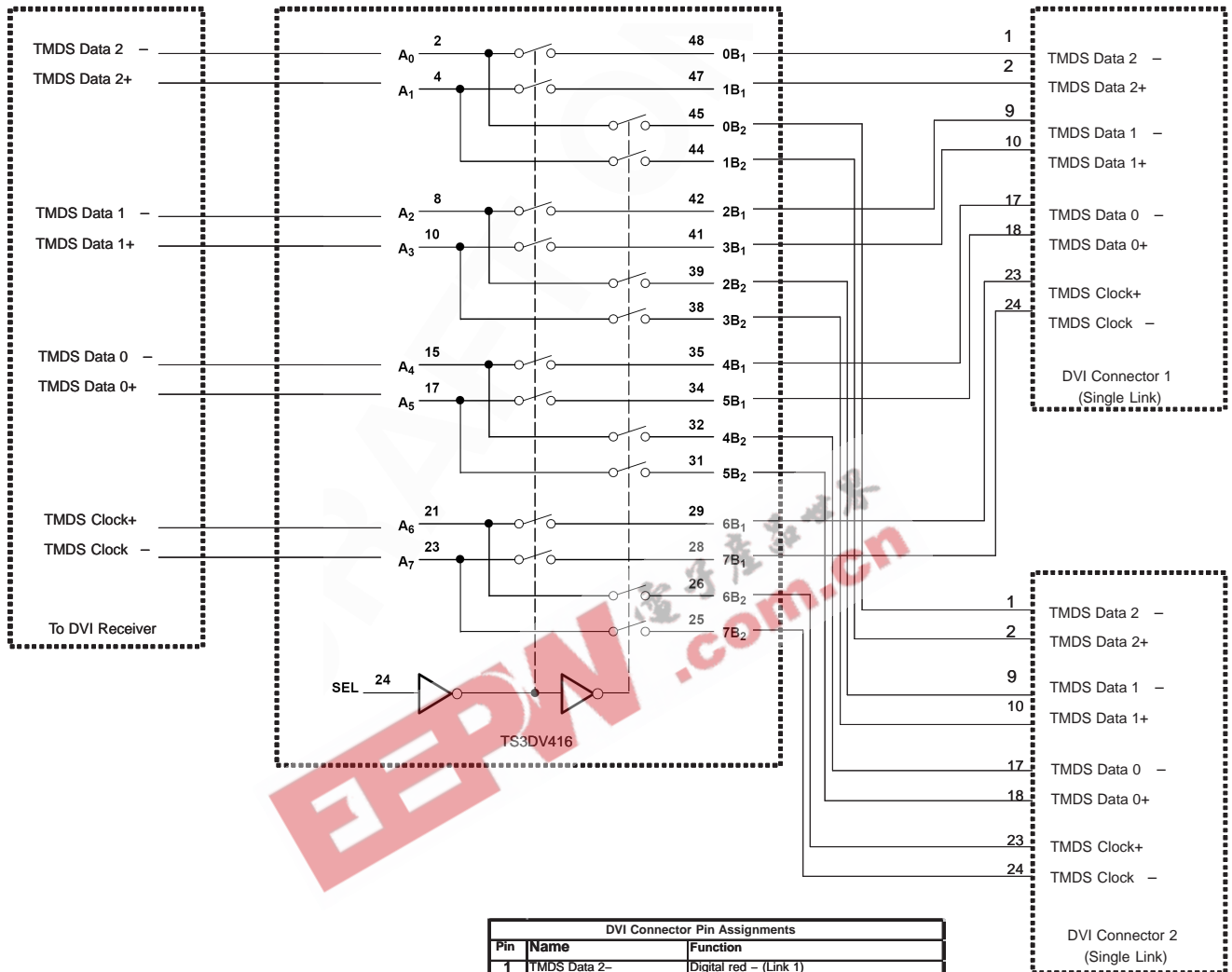
Figure 3. Crosstalk vs Frequency

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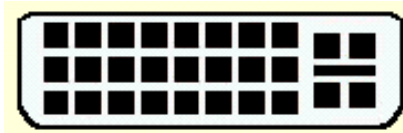
# TS3DV416 4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

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## APPLICATION INFORMATION



Typical DVI Connector



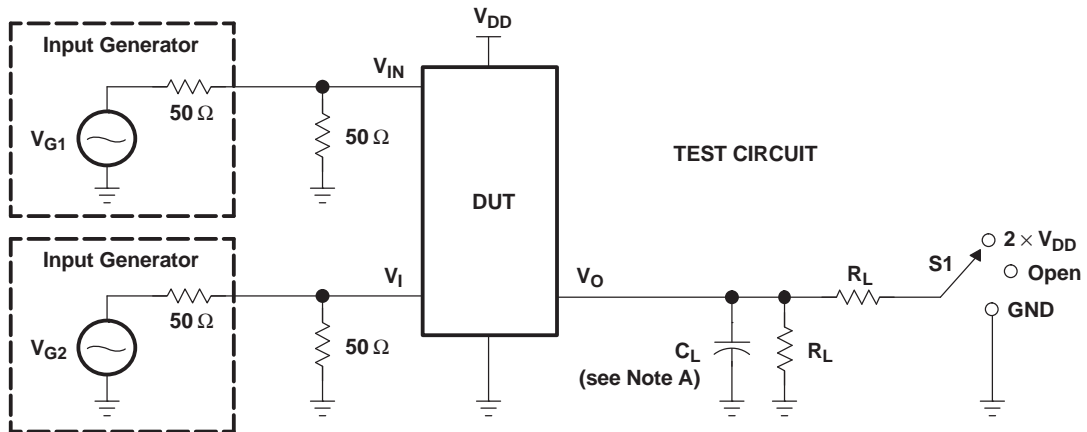
1	2	3	4	5	6	7	8	C1	C2
9	10	11	12	13	14	15	16	C5	
17	18	19	20	21	22	23	24	C3	C4

The TS3DV416 can be used to switch between two digital video ports.

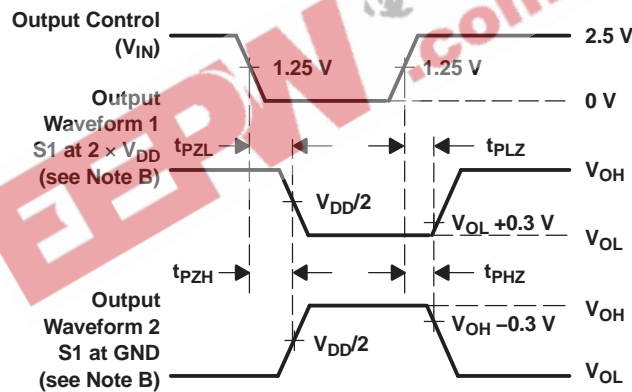
DVI Connector Pin Assignments		
Pin	Name	Function
1	TMDS Data 2-	Digital red - (Link 1)
2	TMDS Data 2+	Digital red + (Link 1)
3	TMDS Data 2/4 shield	
4	TMDS Data 4-	Digital green - (Link 2)
5	TMDS Data 4+	Digital green + (Link 2)
6	DDC clock	
7	DDC data	
8	Analog Vertical Sync	
9	TMDS Data 1-	Digital green - (Link 1)
10	TMDS Data 1+	Digital green + (Link 1)
11	TMDS Data 1/3 shield	
12	TMDS Data 3-	Digital blue - (Link 2)
13	TMDS Data 3+	Digital blue + (Link 2)
14	+5V	Power for monitor when in standby
15	Ground	Return for pin 14 and analog sync
16	Hot Plug Detect	
17	TMDS data 0-	Digital blue - (Link 1) and digital sync
18	TMDS data 0+	Digital blue + (Link 1) and digital sync
19	TMDS data 0/5 shield	
20	TMDS data 5-	Digital red - (Link 2)
21	TMDS data 5+	Digital red + (Link 2)
22	TMDS clock shield	
23	TMDS clock+	Digital clock + (Links 1 and 2)
24	TMDS clock-	Digital clock - (Links 1 and 2)
C1	Analog Red	
C2	Analog Green	
C3	Analog Blue	
C4	Analog Horizontal Sync	
C5	Analog Ground	Return for R, G and B signals



PARAMETER MEASUREMENT INFORMATION  
(Enable and Disable Times)



TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V ± 0.3 V	2 × V <sub>DD</sub>	200 Ω	GND	10 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V ± 0.3 V	GND	200 Ω	V <sub>DD</sub>	10 pF	0.3 V



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

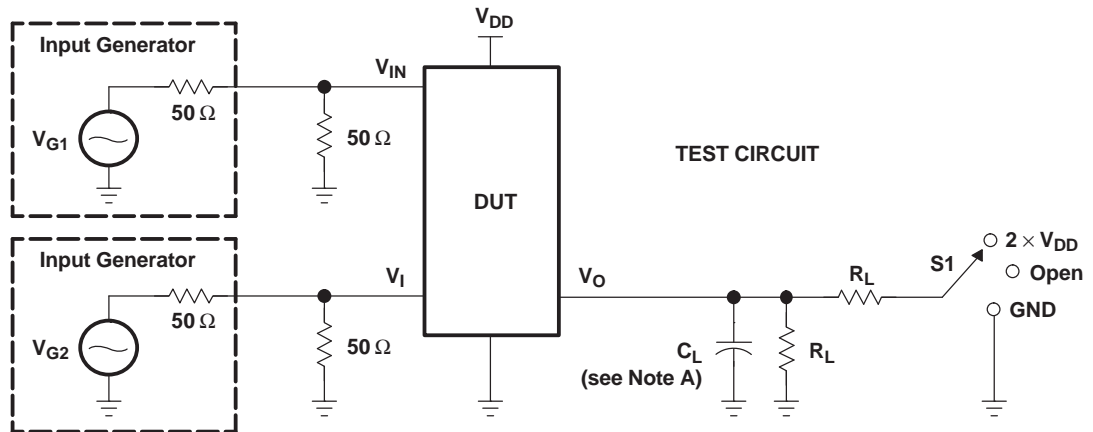
- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. t<sub>PLZ</sub> and t<sub>PHZ</sub> are the same as t<sub>dis</sub>.  
 F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

Figure 4. Test Circuit and Voltage Waveforms

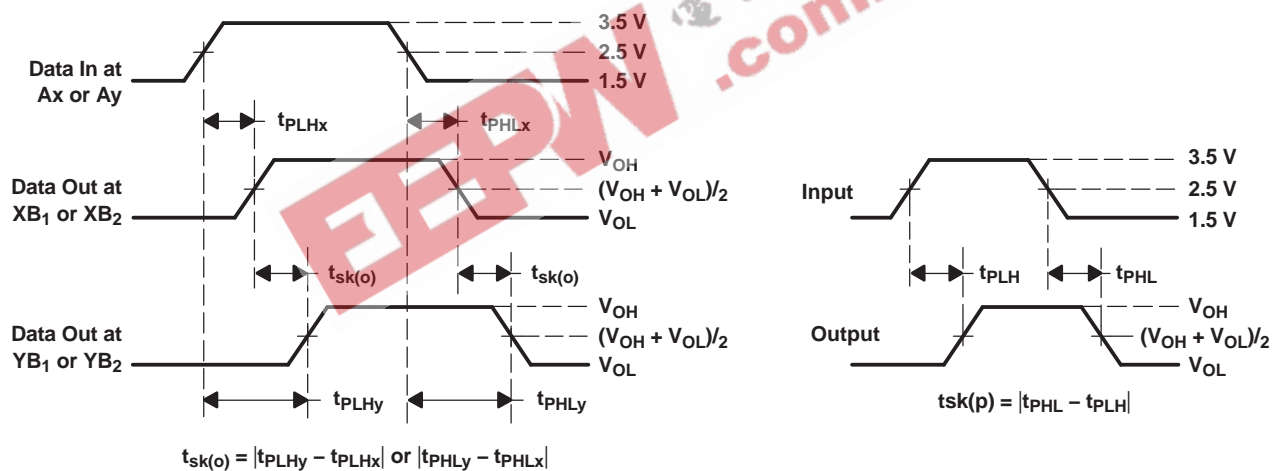
# TS3DV416 4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH FOR DVI/HDMI APPLICATIONS

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## PARAMETER MEASUREMENT INFORMATION (Skew)



TEST	V <sub>DD</sub>	S1	R <sub>L</sub>	V <sub>I</sub>	C <sub>L</sub>	V <sub>Δ</sub>
t <sub>sk(o)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>DD</sub> or GND	10 pF	
t <sub>sk(p)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>DD</sub> or GND	10 pF	



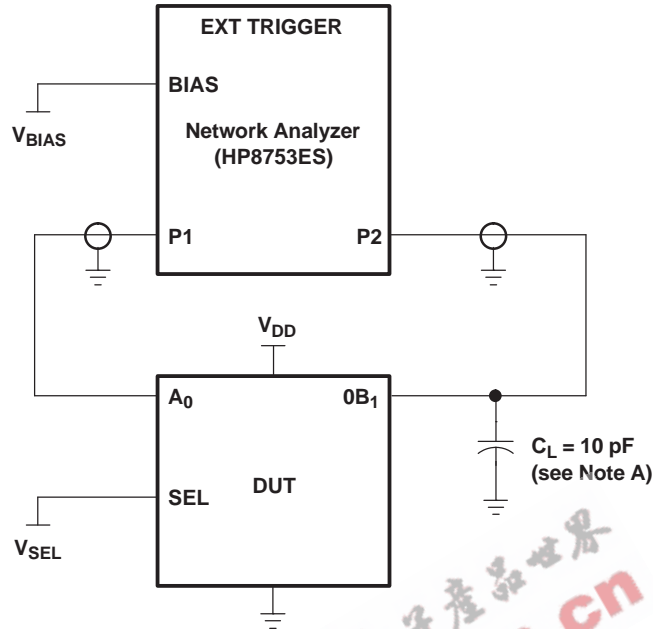
VOLTAGE WAVEFORMS  
OUTPUT SKEW (t<sub>sk(o)</sub>)

VOLTAGE WAVEFORMS  
PULSE SKEW (t<sub>sk(p)</sub>)

- NOTES: A. C<sub>L</sub> includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z<sub>O</sub> = 50 Ω, t<sub>r</sub> ≤ 2.5 ns, t<sub>f</sub> ≤ 2.5 ns.  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 5. Test Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**



NOTE A:  $C_L$  includes probe and jig capacitance.

**Figure 6. Test Circuit for Frequency Response (BW)**

Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL} = 0$  and  $A_0$  is the input, the output is measured at  $0B_1$ . All unused analog I/O ports are left open.

**HP8753ES Setup**

Average = 4

RBW = 3 kHz

$V_{BIAS} = 0.35$  V

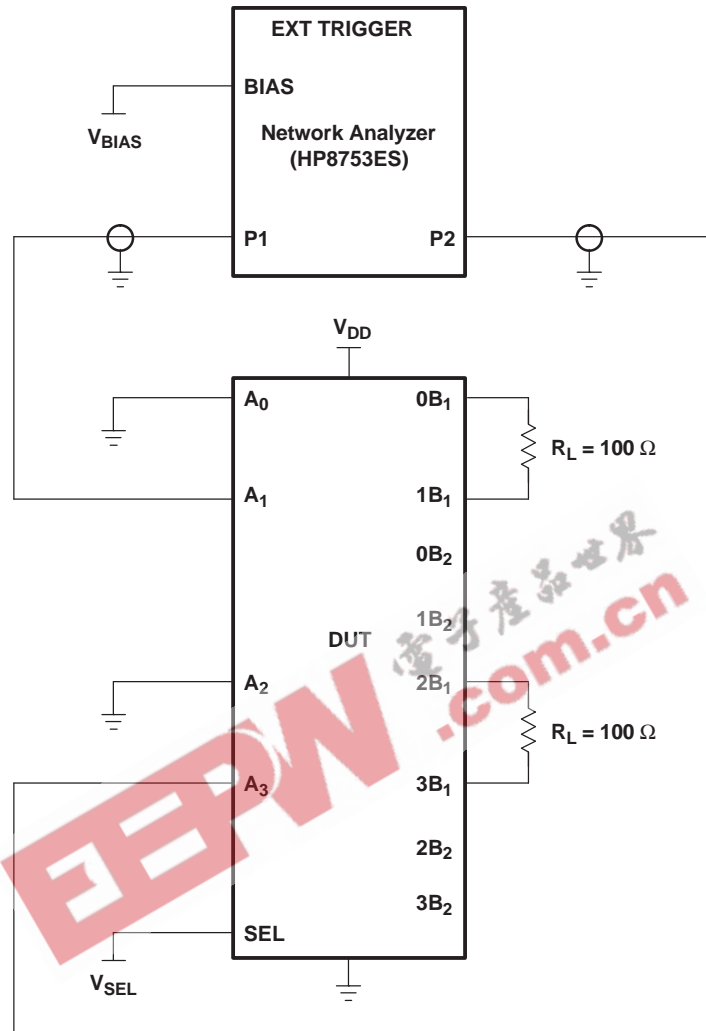
ST = 2 s

P1 = 0 dBm

**TS3DV416**  
**4-CHANNEL DIFFERENTIAL 8:16 MULTIPLEXER SWITCH**  
**FOR DVI/HDMI APPLICATIONS**

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**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

**Figure 7. Test Circuit for Crosstalk ( $X_{TALK}$ )**

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{SEL} = 0$  and  $A_1$  is the input, the output is measured at  $A_3$ . All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

**HP8753ES Setup**

Average = 4

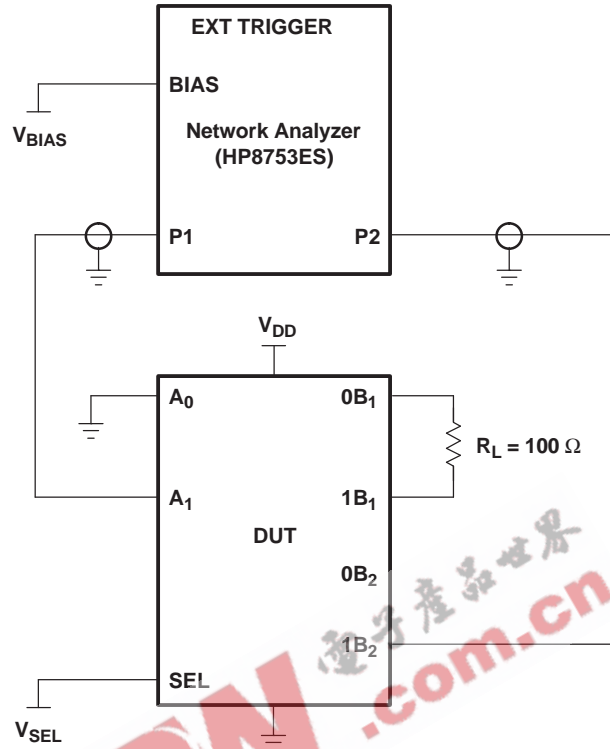
RBW = 3 kHz

$V_{BIAS} = 0.35$  V

ST = 2 s

P1 = 0 dBm

**PARAMETER MEASUREMENT INFORMATION**



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

**Figure 8. Test Circuit for OFF Isolation ( $O_{IRR}$ )**

OFF isolation is measured at the output of the OFF channel. For example, when  $V_{SEL} = GND$  and  $A_1$  is the input, the output is measured at  $1B_2$ . All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

**HP8753ES Setup**

Average = 4

RBW = 3 kHz

$V_{BIAS} = 0.35\text{ V}$

ST = 2 s

P1 = 0 dBm

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TS3DV416DGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3DV416DGGRE4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS3DV416DGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

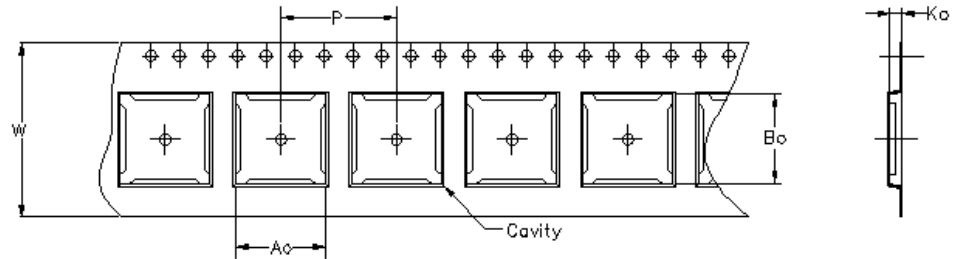
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

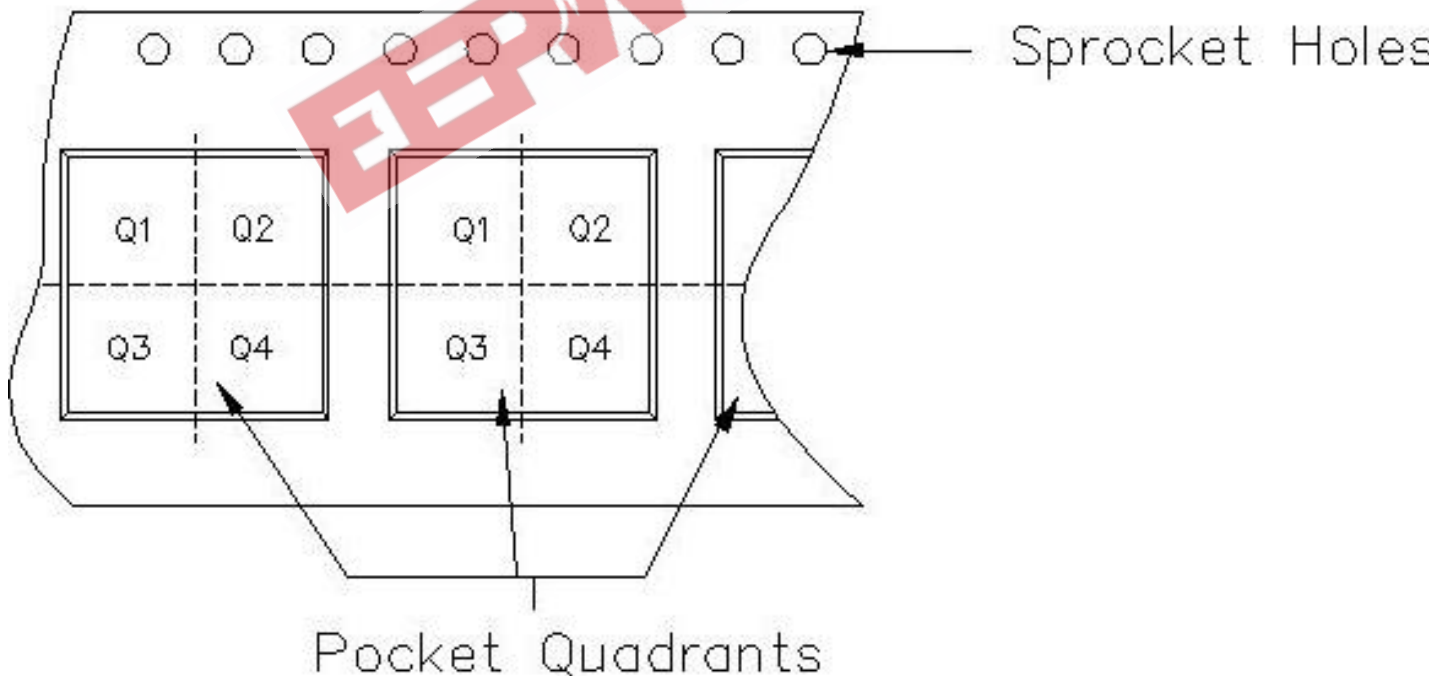
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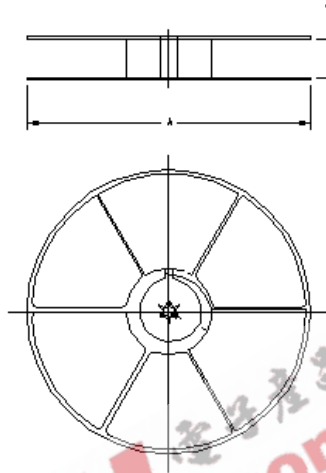
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



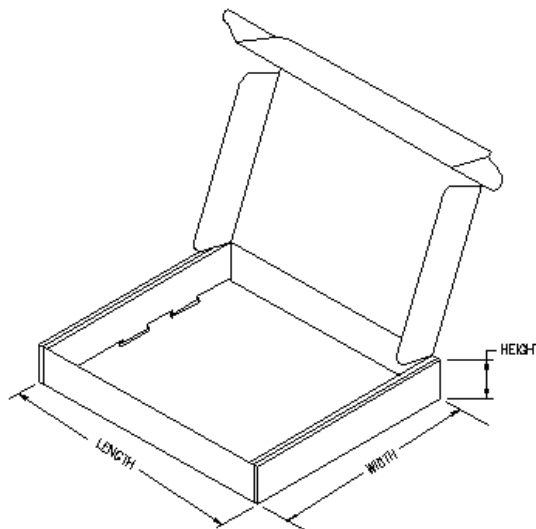
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV416DGGR	DGG	48	MLA	330	24	8.6	15.8	1.8	12	24	Q1
TS3DV416DGVR	DGV	48	MLA	330	24	6.8	10.1	1.6	12	24	Q1



**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TS3DV416DGGR	DGG	48	MLA	333.2	333.2	31.75
TS3DV416DGVR	DGV	48	MLA	333.2	333.2	31.75





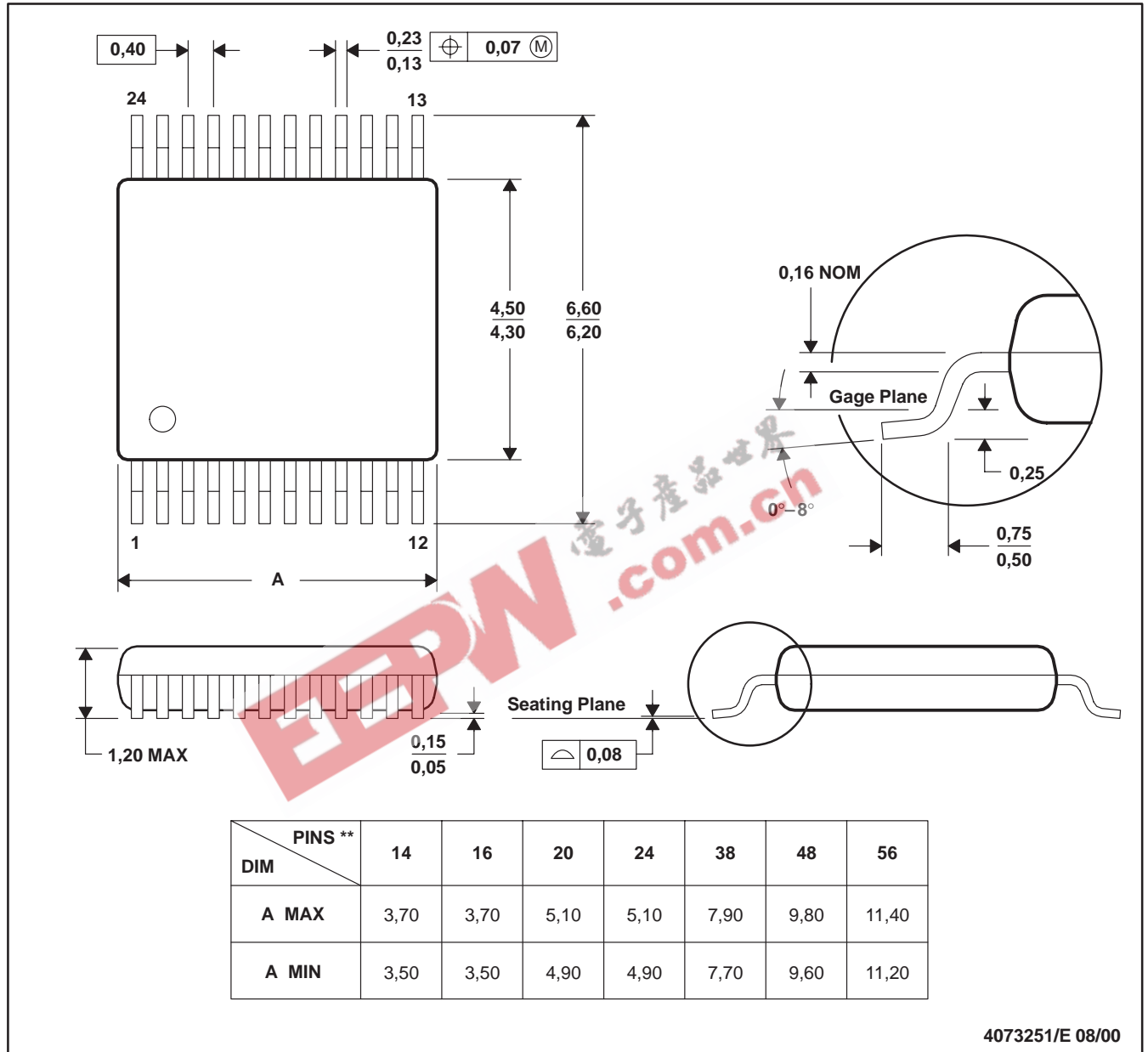
# MECHANICAL DATA

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

**DGV (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



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