4-ch MOTOR DRIVER FOR PORTABLE CD PLAYERS —YD5901

DESCRIPTION

This driver IC contains a 4ch H bridge driver and DC-DC converter control circuit on one chip, and was developed for use in portable CD players. QFP-44 is used for the package, making it ideal for smaller sets.

FEATURES

*Built-in 4ch H Bridge Driver, and PWM Control of Load Drive Voltage is Made Possible by External Components.

*DC-DC Converter Control Circuit on Chip.

* With Reset Output Inversion Output Pin.

*Empty Detection Level Can be Switched Between Rechargeable Battery and Dry Battery.

*Constant Current Charging; Current Value Can be Varied Using External Resistor.

*Built-in Power Transistor For Charging.

*Built-in Independent Thermal Shutdown Circuit.

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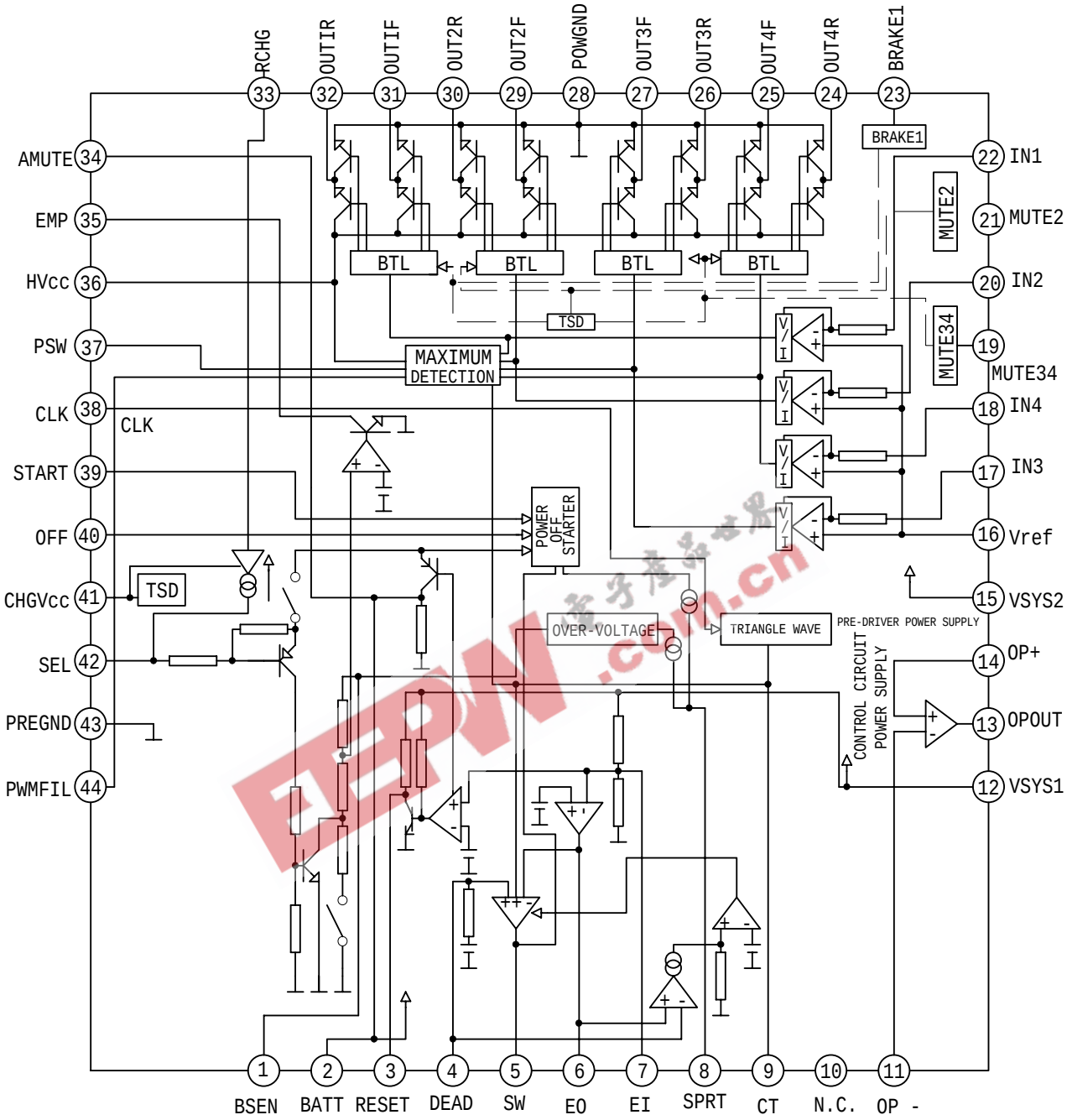
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25℃)

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc*1	13.5	V
Driver Output Current	Io	500	mA
Power Dissipation	P_D	625*2	mW
Operating Temperature	Topr	-30 to +85	℃
Storage Temperature	Tstg	-55 to +150	℃

*1 Vcc shows input voltage of VSYS1, VSYS3, HVcc, BATT, and CHGVcc.

*2 Reduced by 5mW for each increase in Tamb of 1℃ over 25℃.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Tamb=25℃, BATT=2.4V, VSYS1=VSYS2=3.2V, Vref=1.6V, CHGVcc=0V, fCLK=88.2kHz)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common Section						
BATT Stand-by Current	I_{ST}	BATT=9.0V, VSYS1=VSYS2=Vref=0V		0	3	μA
BATT Supply Current (No Load)	I_{BAT}	HVcc=0.45V, MUTE34=3.2V		2.5	4.0	mA
VSYS1 Supply Current (No Load)	I_{SYS1}	HVcc=0.45V, MUTE34=3.2, EI=0V		4.7	6.4	mA
VSYS2 Supply Current (No Load)	I_{SYS2}	HVcc=0.45V, MUTE34=3.2V		4.1	5.5	mA
CHGVcc Supply Current (No Load)	I_{CGVCC}	CHGVcc=4.5V, R_{OUT}=OPEN		0.65	2.00	mA
H-Bridge Driver Part						
Voltage Gain ch1, ch3, ch4	G_{VC134}		12	14	16	dB
Voltage Gain ch2	G_{VC2}		21.5	23.5	24.5	dB
Gain Error By Polarity	ΔG_{VC}		-2	0	2	dB
Input Pin Resistance ch1, ch3, ch4	R_{IN134}	IN=1.7Vand 1.8V	9	11	13	kΩ
Input Pin Resistance ch2	R_{IN2}	IN=1.7V and 1.8V	6	7.5	9	kΩ
Maximum Output Voltage	V_{OUT}	RL=8Ω, HVcc=BATT=4.0V, IN=0-3.2V	1.9	2.1		V
Saturation Voltage (Lower)	VsatL	I_O=-300mA, IN=0 和 3.2V		240	400	mV

Saturation Voltage (Upper)	VsatU	I_O=-300mA, IN=0 和 3.2V		240	400	mV
Input Offset Voltage	V_{OI}		-8	0	8	mV
Output Offset Voltage ch1, ch3, ch4	V_{OO134}	Vref=IN=1.6V	-50	0	50	mV
Output Offset Voltage ch2	V_{OO2}	Vref=IN=1.6V	-130	0	130	mV
Dead Zone	V_{DB}		-10	0	10	mV
BRAKE1 ON Threshold Voltage	V_{BRON}	IN1=1.8V	2.0			V
BRAKE1 OFF Threshold Voltage	V_{BROFF}	IN1=1.8V			0.8	V
MUTE2 ON Threshold Voltage	V_{M20N}	IN2=1.8V	2.0			V
H-Bridge Driver Part						
MUTE2 OFF Threshold Voltage	V_{M2OFF}	IN2=1.8V			0.8	V
MUTE34 ON Threshold Voltage	V_{M34ON}	IN3=IN4=1.8V			0.8	V
MUTE34 OFF Threshold Voltage	V_{M34OFF}	IN3=IN4=1.8V	2.0			V
Vref ON Threshold Voltage	V_{refON}	IN1=IN2=IN3=IN4=1.8V	1.2			V
Vref OFF Threshold Voltage	V_{refOFF}	IN1=IN2=IN3=IN4=1.8V			0.8	V
BRAKE1 Brake Current	I_{BRAKE1}	Current difference between BRAKE pin “H” time and “L” time.	4	7	10	mA
PWM Power Supply Driving						
PSW Sink Current	I_{PSW}	IN1=2.1V	10	13	17	mA
HVcc Level Shift Voltage	V_{SHIF}	IN1=1.8V, HVcc-OUT1F	0.35	0.45	0.55	V
HVcc Leak Current	I_{HLK}	HVcc=9.0V, VSYS1=VSYS2=BATT =0V		0	5	μA
PWM Amp Transfer Gain		HVcc=1.8V, HVcc=1.2～1.4V	1/60	1/50	1/40	1/kΩ
DC-DC Converter						
Error Amp						
VSYS1 Threshold Voltage	V_{SITH}		3.05	3.20	3.35	V

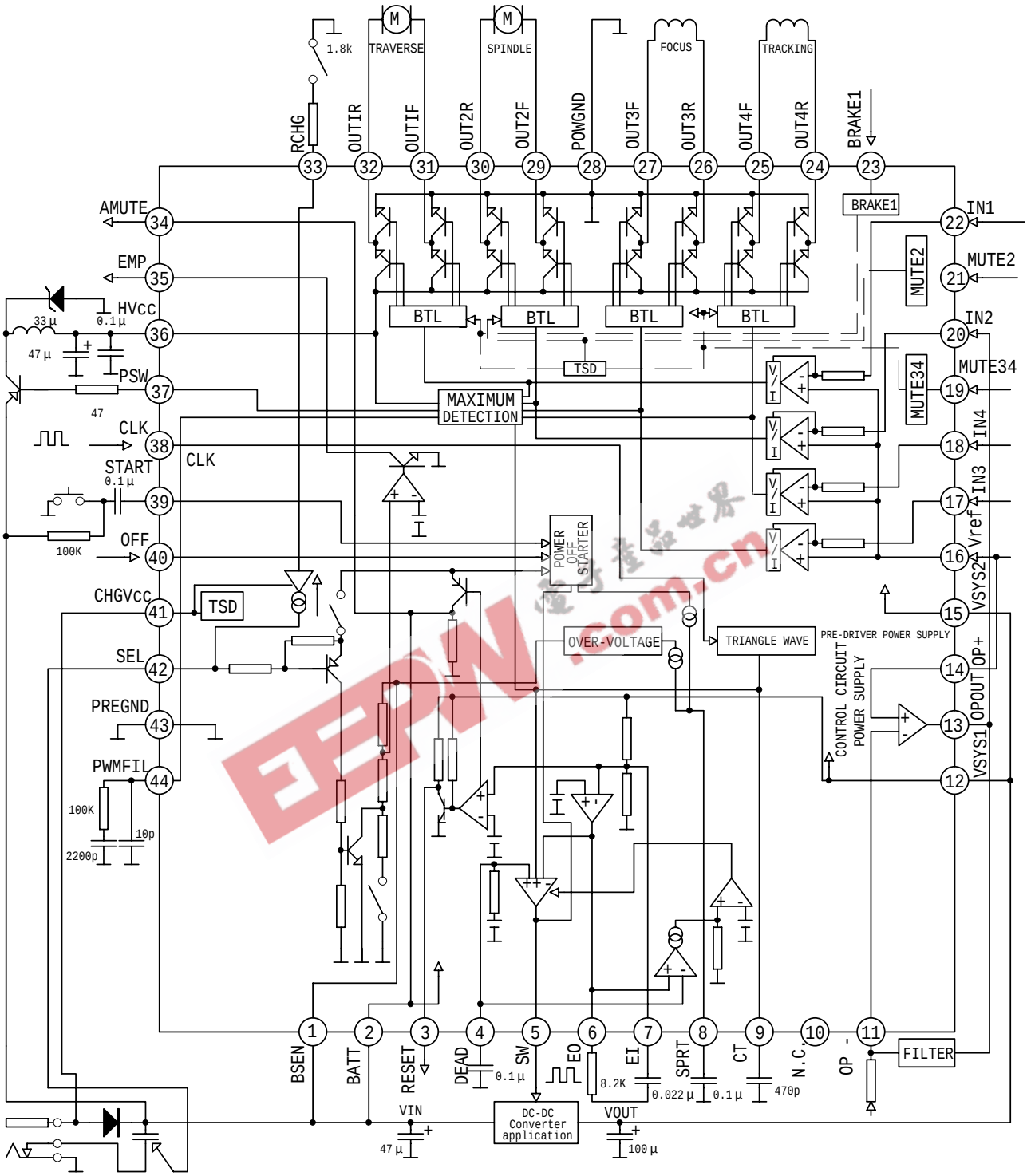
EO Pin Output Voltage "H"	V_{EOH}	EI=0.7V, Io=-100μA	1.4	1.6		V
EO Pin Output Voltage "L"	V_{EOL}	EI=1.3V, Io=100μA			0.3	V
Short Circuit Protection						
SPRT Pin Voltage	V_{SPR}	EI=1.3V		0	0.1	V
EO=H SPRT Pin Current1	I_{SPR1}	EI=0.7V	6	10	16	μA
OFF=L SPRT Pin Current2	I_{SPR2}	EI=1.3V, OFF=0V	12	20	32	μA
SPRT Pin Current3 Over-Voltage	I_{SPR3}	EI=1.3V, BATT=9.5V	12	20	32	μA
SPRT Pin Impedance	R_{SPR}		175	220	265	kΩ
SPRT Pin Threshold Voltage	V_{SPTH}	EI=0.7V, C_T=0V	1.10	1.20	1.30	V
Over-Voltage Protection Detect	V_{HVPR}	BSEN Pin Voltage	8.0	8.4	9.0	V
Transistor Driving						
SW Pin Output Voltage1 "H"	V_{SW1H}	BATT=C_T=1.5V, S1=VSYS2=0V, Io=-2mA Starting Time	0.78	0.98	1.13	V
SW Pin Output Voltage 2 "H"	V_{SW2H}	CT=0V, Io=-10mA, EI=0.7V, SPRT=0V	1.00	1.50		V
SW Pin Output Voltage 2 "L"	V_{SW2L}	CT=20V, I_O=-10mA		0.30	0.45	V
SW Pin Oscillating Frequency1	f_{sw1}	C_T=470pF, VSYS1=YSYS2=0V Starting time	65	80	95	kHz
SW Pin Oscillating Frequency 2	f_{sw2}	CT=470pF, CLK=0V	60	70	82	kHz
SW Pin Oscillating Frequency 3	f_{sw3}	CT=470pF		88.2		kHz
SW Pin Minimum Pulse Width	T_{SWMIN}	C_T=470pF, EO=0.5V→0.7V Sweep	0.01		0.60	ms
Pulse Duty Start	D_{SW1}	C_T=470pF, VSYS1=VSYS2=0V	40	50	60	%
Max. Pulse Duty At Self-Running	D_{SW2}	C_T=470pF, EI=0.7V, CLK=0V	70	80	90	%
Max. Pulse Duty At CLK Synchronization	D_{SW3}	C_T=470pF, EI=0.7V	65	75	85	%

Interface						
OFF Pin Threshold Voltage	V_{OFIH}	EI=1.3V			VSYS1 -2.0	V
OFF Pin Bias Current	I_{OFF}	OFF=0V	75	95	115	μA
START Pin ON Threshold Voltage	V_{STATH1}	VSYS1=VSYS2=0V, C_T=2.0V			BATT-1.0	V
START Pin OFF Threshold Voltage	V_{STATH2}	VSYS1=VSYS2=0V, C_T=2.0V	BATT-0.3			V
START Pin Bias Current	I_{START}	START=OV	10	20	30	μA
CLK Pin Threshold Voltage “H”	V_{CLKTHH}		2.0			V
CLK Pin Threshold Voltage “L”	V_{CLKTHL}				0.8	V
CLK Pin Bias Current	I_{CLK}	CLK=3.2V			10	μA
Dead Time						
DEAD Pin Impedance	R_{DEAD}		52	65	78	kΩ
DEAD Pin Output Voltage	V_{DEAD}		0.78	0.88	0.98	V
Starter Circuit						
Starter Switching Voltage	V_{STNM}	VSYS1=VSYS2=0V→ 3.2V, START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	V_{SNHS}	START=0V	130	200	300	mV
Discharge Release	V_{DIS}		1.63	1.83	2.03	V
Empty Detection						
EMP Detection Voltage1	V_{EMPT1}	VSEL=0V	2.1	2.2	2.3	V
EMP Detection Voltage2	V_{EMPT2}	ISEL=-2μA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	V_{EMHS1}	VSEL=0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	V_{EMHS2}	ISEL=-2μA	25	50	100	mV
EMP Pin Output Voltage	V_{EMP}	I_O=1mA,BSEN=1V			0.5	V
EMP Pin Output Leak Current	I_{EMPL}	BSEN=2.4V			1.0	μA
BSEN Pin Input Resistance	R_{BSEN}	VSEL=0V	17	23	27	kΩ

BSEN Pin Leak Current	I_{BSENL}	VSYS1=VSYS2=0V, BSEN=4.5V			1.0	mA
SEL Pin Detection Voltage	V_{SELTH}	VSELTH=BATT-SEL, BSEN=2.0V	1.5			V
SEL Pin Detection Current	I_{SELT}		-2			μA
Reset Circuit						
VSYS1RESET Threshold Voltage Ratio	H_{SRT}	Comparison with error amplifier threshold voltage	85	90	95	%
RESET Detection Hysteresis Width	V_{RSTHS}		25	50	100	mV
RESET Pin Output Voltage	V_{RST}	I_O=1mA, VSYS1=VSYS2=2.8V			0.5	V
RESET Pin PULL UP Resistance	R_{RST}		72	90	108	kΩ
AMUTE Pin Output Voltage1	V_{AMT1}	I_O=-1mA, VSYS1=VSYS2=2.8V	BATT-0.4		BATT	V
AMUTE Pin Output Voltage2	V_{AMT2}	I_O=-1mA, START=0V, VSYS1=VSYS2=0V	BATT-0.4		BATT	V
AMUTE Pin PULL DOWN Resistance	R_{AMT}		77	95	113	kΩ
Op Amp						
Input Bias Current	I_{BIAS}	OP+=1.6V			300	nA
Input Offset Voltage	V_{OIOP}		-5.5	0	5.5	mV
High Level Offset Voltage	V_{OHOP}	RL=OPEN	2.8			V
Low Level Offset Voltage	V_{OLOP}	RL=OPEN			0.2	V
Output Drive Current（Source）	I_{SOU}	50Ω GND		-6.5	-3.0	mA
Output Drive Current（Sink）	I_{SIN}	50Ω GND	0.4	0.7		mA
Open Loop Voltage Gain	GVO	V_{IN}=-7.5dBV, f=1kHz		70		dB
Slew Rate	SR			0.5		V/μs
Battery Charging Circuit						
RCHG Pin Bias Voltage	V_{RCHG}	CHGVcc=4.5V, RCHG=1.8kΩ	0.71	0.81	0.91	V
RCHG Pin Output Resistance	R_{RCHG}	CHGVcc=4.5V, RCHG=0.5V 和 0.6V	0.75	0.95	1.2	kΩ

SEL Pin Leak Current 1	I_{SELLK1}	CHGVcc=4.5V, RCHG=OPEN, BATT=4.5V			1.0	mA
SEL Pin Leak Current 2	I_{SELLK2}	CHGVcc=0.6V, RCHG=1.8kΩ, BATT=4.5V			1.0	μA
SEL Pin Saturation Voltage	V_{SELCG}	CHGVcc=4.5V, I_O=300mA, RCHG=0Ω		0.45	1.00	V

APPLICATION CIRCUIT



OUTLINE DRAWING