

54F/74F378 Parallel D Register with Enable

General Description

The 'F378 is a 6-bit register with a buffered common Enable. This device is similar to the 'F174, but with common Enable rather than common Master Reset.

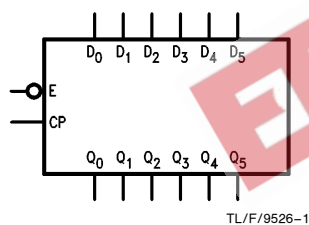
Features

- 6-bit high-speed parallel register
- Positive edge-triggered D-type inputs
- Fully buffered common clock and enable inputs
- Input clamp diodes limit high-speed termination effects
- Full TTL and CMOS compatible

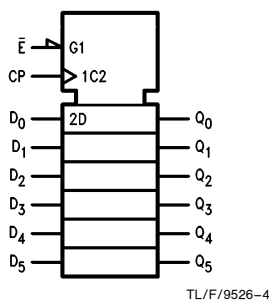
Commercial	Military	Package Number	Package Description
74F378PC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F378DM (QB)	J16A	16-Lead Ceramic Dual-In-Line
74F378SC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F378SJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F378FM (QB)	W16A	16-Lead Cerpack
	54F378LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols

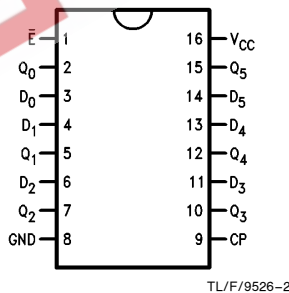


IEEE/IEC

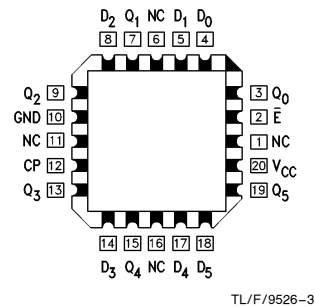


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\bar{E}$	Enable Input (Active LOW)	1.0/1.0	20 μA / -0.6 mA
D_0-D_5	Data Inputs	1.0/1.0	20 μA / -0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA / -0.6 mA
Q_0-Q_5	Outputs	50/33.3	-1 mA/20 mA

Functional Description

The 'F378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\bar{E}$) inputs are common to all flip-flops.

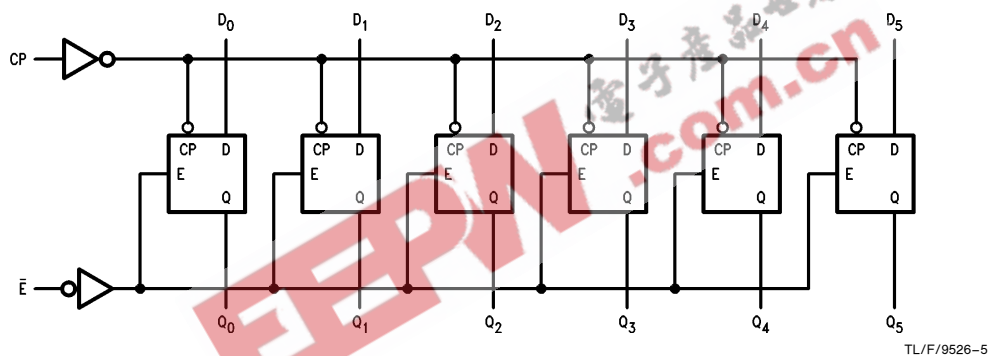
When the $\bar{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\bar{E}$ input is HIGH the register will retain the present data independent of the CP input.

Truth Table

Inputs			Output
$\bar{E}$	CP	D_n	Q_n
H	—	X	No Change
L	—	H	H
L	—	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
— = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE® Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.5 2.7		V	Min	I _{OH} = −1 mA I _{OH} = −1 mA I _{OH} = −1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 20 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current		−60	−150	mA	Max	V _{OUT} = 0V
I _{CCL}	Power Supply Current		30	45	mA	Max	V _O = LOW

AC Electrical Characteristics

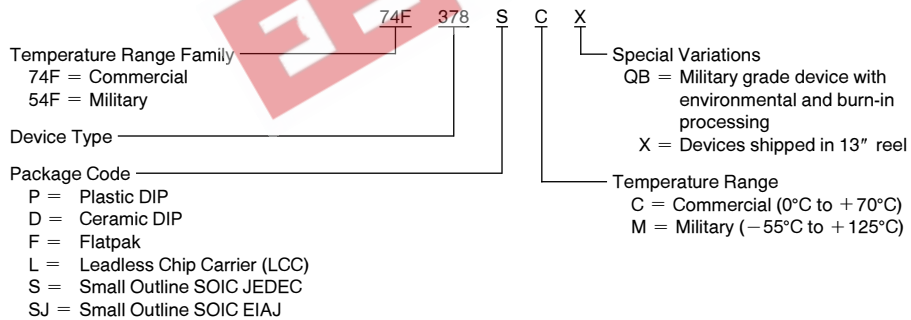
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Input Frequency	80	100		70		80		MHz
t_{PLH}	Propagation Delay	3.0	5.5	7.5	3.0	10.0	3.0	8.5	ns
t_{PHL}	CP to Q_n	3.5	6.0	8.5	3.5	10.5	3.5	9.5	

AC Operating Requirements

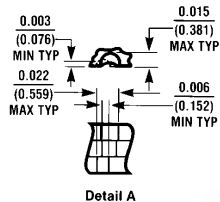
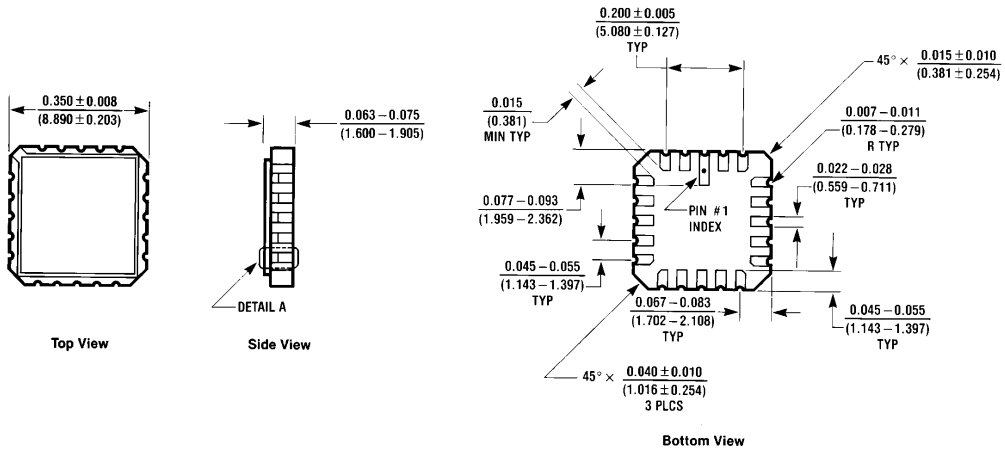
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.0		5.0		4.0		ns
$t_s(\text{L})$	D_n to CP	4.0		5.0		4.0		
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		2.0		0		ns
$t_h(\text{L})$	D_n to CP	0		2.0		0		
$t_s(\text{H})$	Setup Time, HIGH or LOW	6.0		4.5		6.0		ns
$t_s(\text{L})$	$\bar{E}$ to CP	10.0		13.0		10.0		
$t_h(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns
$t_h(\text{L})$	$\bar{E}$ to CP	0		0		0		
$t_w(\text{H})$	CP Pulse Width	4.0		5.0		4.0		ns
$t_w(\text{L})$	HIGH or LOW	6.0		7.5		6.0		

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

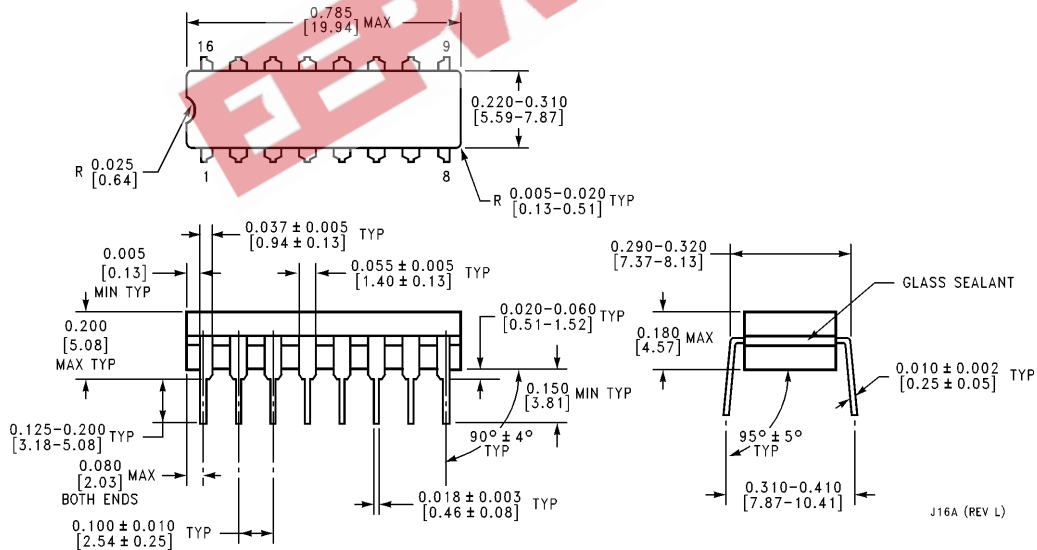


Physical Dimensions inches (millimeters)



**20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A**

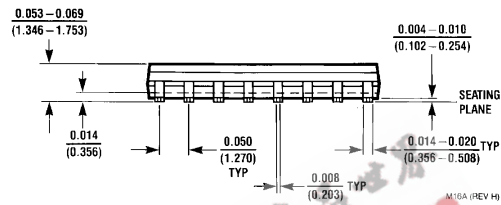
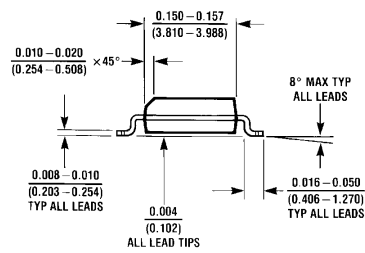
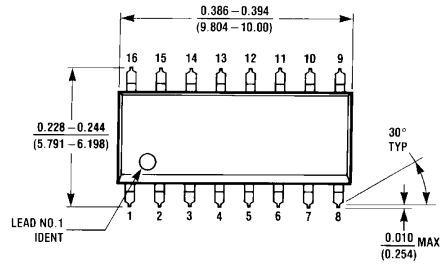
E20A (REV D)



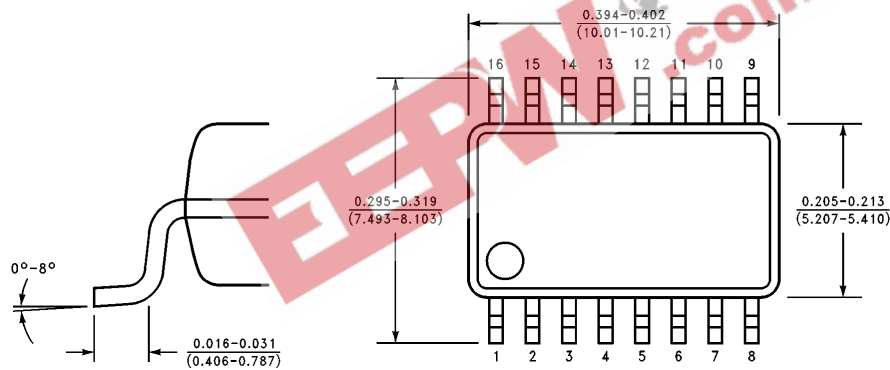
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

J16A (REV L)

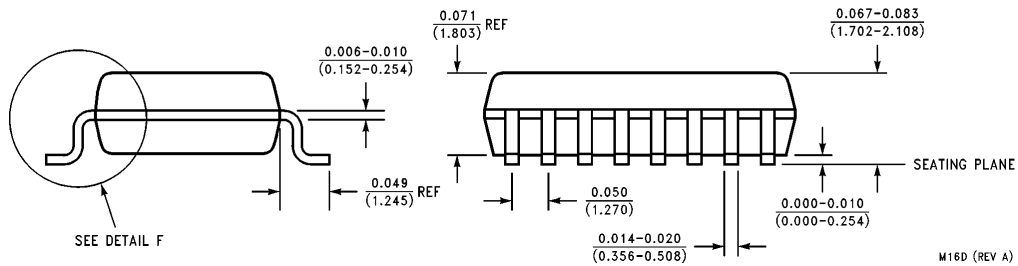
Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC
NS Package Number M16A



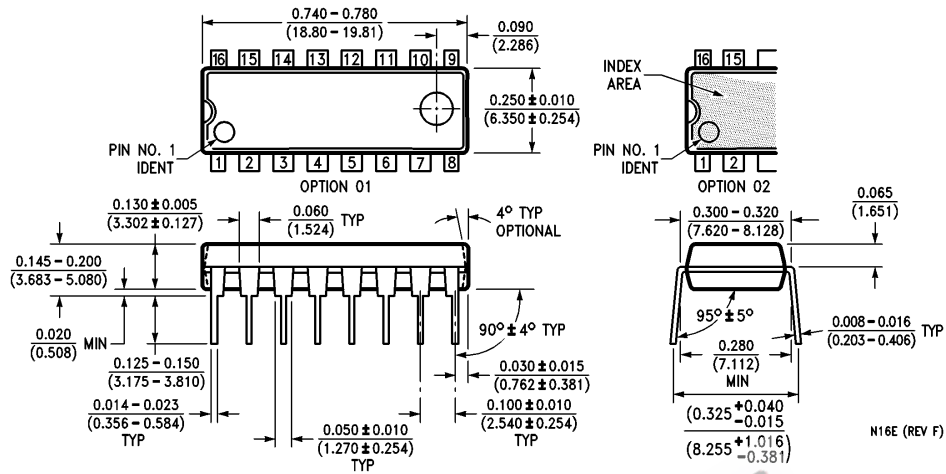
DETAIL F



16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

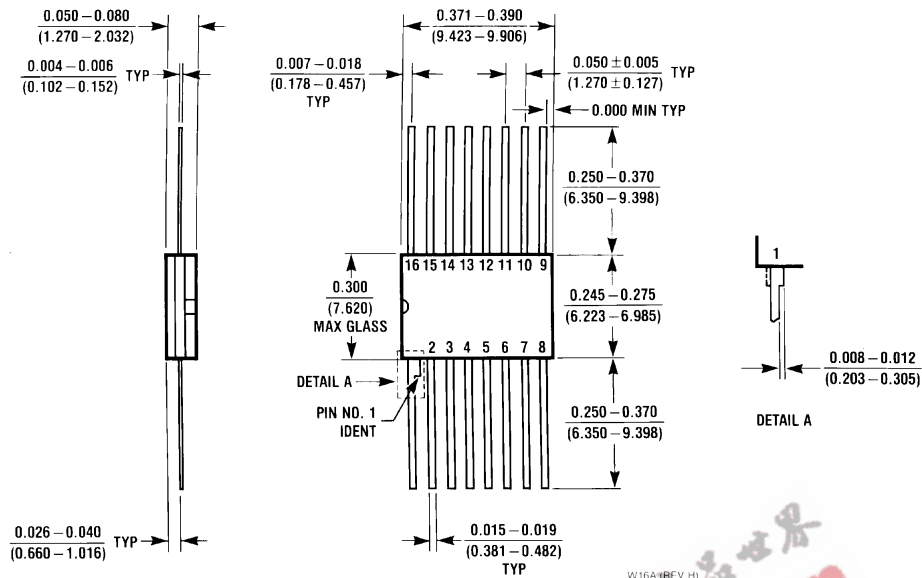
M16D (REV A)

Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

N16E (REV F)

Physical Dimensions inches (millimeters) (Continued)

16-Lead Ceramic Flatpak (F)
NS Package Number W16A

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National Semiconductor Corporation
 2900 Semiconductor Drive
 P.O. Box 58090
 Santa Clara, CA 95052-8090
 Tel: (800) 272-9959
 TWX: (910) 339-9240

National Semiconductor GmbH
 Livry-Gargan-Str. 10
 D-82256 Fürstentfeldbruck
 Germany
 Tel: (81-41) 35-0
 Telex: 527649
 Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
 Sumitomo Chemical
 Engineering Center
 Bldg. 7F
 1-7-1, Nakase, Mihama-Ku
 Chiba-City,
 Chiba Prefecture 261
 Tel: (043) 299-2300
 Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
 13th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
 Rue Deputado Lacorda Franco
 120-3A
 Sao Paulo-SP
 Brazil 05418-000
 Tel: (55-11) 212-5066
 Telex: 391-1131931 NSBR BR
 Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
 Building 16
 Business Park Drive
 Monash Business Park
 Nottingham, Melbourne
 Victoria 3168 Australia
 Tel: (3) 558-9889
 Fax: (3) 558-9998

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